A 7-bit 300-MS/s Subranging ADC with Embedded Threshold & Gain-Loss Calibration

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Abstract— **This paper reports a 7-bit 300-MS/s subranging ADC fabricated in standard 65nm CMOS, which utilizes embedded reference and gain loss error calibration techniques. A shared passive capacitive DAC array performs the input sampling in quantization mode and reference generation in calibration mode, providing a linear, accurate and compact calibration implementation. As a consequence of the developed calibration techniques, uniform-sized dynamic comparators are employed to reduce the process-mismatch variation and nonlinearity error, when compared with the conventional structures. The ADC achieves peak SNDR of 40.5dB at 300MS/s and 39dB at 400MS/s, with ERBW of 300MHz and 350MHz, respectively. The power consumption is 2.3mW only from 1.2-V supply at 300MS/s.**

I. INTRODUCTION

In order to satisfy the low power requirements of most of modern electronic systems, the conventional full flash converter structure has been replaced by subranging or two-step architectures [1]-[3] which provide an option to trade off between speed and exponential growth in the number of comparators. However, the large amount of preamplifiers [2] [3] for suppressing the comparator offset variations in the parallel path of the sub-flash ADCs leads to large static power consumption and is still unavoidable. Removing the static preamplifiers and employing dynamic built-in threshold comparators [1] [4] can enhance the power efficiency of the flash ADC, but it causes larger kickback noise and offset mismatch from the unbalanced-size dynamic comparators [1] [4] which are especially sensitive in medium (6 to 8 bit) to high (9+ bit) resolution ADC designs.

This paper presents a compact and power-efficient medium-resolution subranging ADC architecture which employs uniform-sized dynamic latch-type comparators with a proposed on-chip digital calibration scheme. Reference voltages of the ADC are embedded as built-in thresholds of the comparators to save the reference charging power during quantization, whose accuracies are guaranteed by the parasitic gain loss and comparator offset calibration. On the other hand, the comparators' dimensions are uniform to reduce the sensitivity to process variation, diminish the signal dependent error from kickback noise and enhance the compactness of the layout. Besides, a precise capacitive DAC array is reused in the ADC conversion and calibration modes to achieve a compact implementation. To verify performance boundary, the prototype ADC is implemented with an 8-bit scheme, and the measurement result shows that the best achievement is attained at the resolution of 7-bit level.

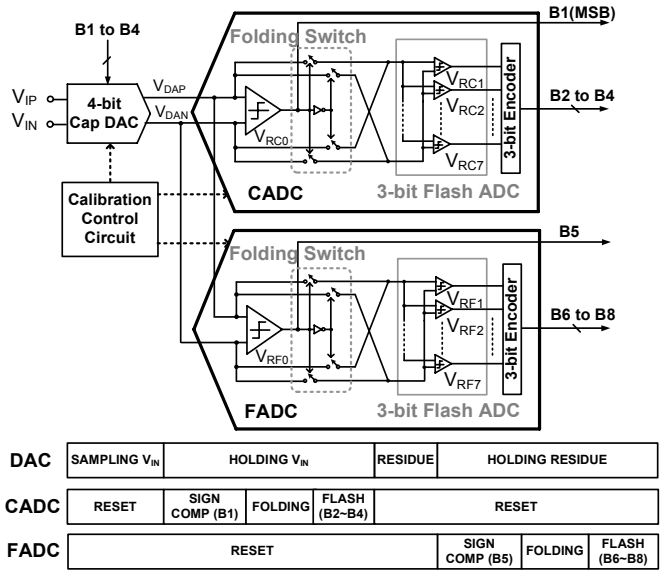

Fig. 1. The overall ADC architecture.

II. THE PROPOSED ADC ARCHITECTURE

Fig. 1 shows the architecture of the proposed subranging ADC. The CADC and the FADC with similar structure

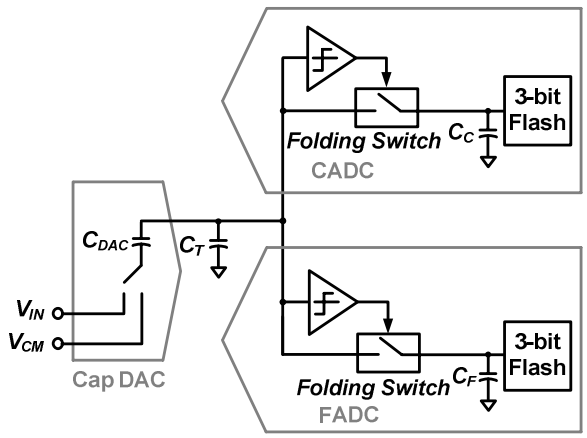

Fig. 2. Parasitic capacitances at inter-stages.

consist of a 1-bit sign comparator, folding switches and a 3-bit flash with 7 embedded threshold comparators. A capacitive DAC works as a passive track-and-hold while the proposed ADC is quantizing. The sign comparator with the threshold at mid-supply quantizes the B1 (MSB) which determines the connection of folding switches [4] between the DAC and the 3-bit flash in the CADC. After the charge in the DAC has been shared with the input capacitance of the flash, the remaining 3 bits (B2 to B4) of the coarse code can be quantized. A residue is generated in the same DAC with the coarse code by the switching with supply V_{DD} and ground V_{SS}, in order not to consume any static power. Then, FADC quantizes the residue to a fine code (B5 to B8) similarly to the CADC.

III. NONLINEARITY CONSIDERATION

A. Gain-loss error

The non-linearity of the subranging ADC results mainly from the inter-stage gain error due to the different parasitic capacitance of two quantization steps. Fig. 2 shows the main parasitic capacitances C_T, C_C and C_F affecting the inter-stage conversion, which include the parasitic capacitance at the top plate of the DAC (C_T) and the inputs of coarse (C_C) and fine (C_F) stages. Since bottom-plate sampling is applied to reduce the charge injection in the DAC array, the held signal suffers a gain loss from the charge sharing of the C_{DAC} and C_T at the top-plate of the DAC. Once the folding switch in the CADC turns on, the gain is changed to

$$A_C = \frac{C_{DAC}}{C_{DAC} + C_T + C_C} \tag{1}$$

by the charge-sharing effect between the DAC and the parasitic capacitance at the 3-bit flash sub-ADC in the coarse stage. In the fine-step quantization, the gain is altered to

$$A_F = \frac{C_{DAC}}{C_{DAC} + C_T + C_C + C_F} \tag{2}$$

From equations (1) and (2), the input sampled signal magnitude always suffers different gain losses with different processing steps.

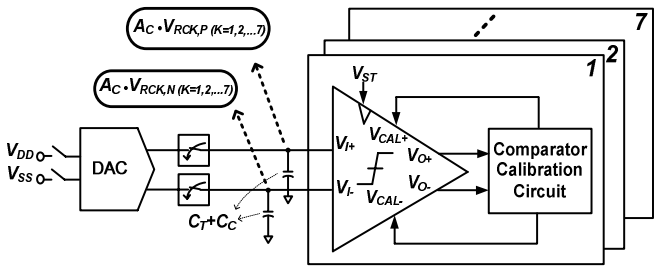

Fig. 3. Embedded threshold with gain-loss calibration in CADC.

B. kickback noise

As the comparator input signal is corrupted by the kickback noise through the comparator input pair at the instant of the trigging phase, the amount of kickback is directly related to the size of the input pair as well as the number of the dynamic comparators. The strategy for reducing the kickback noise implies the minimization of the number of activating comparators in each phase, as well as the dynamic comparators size reduction, to minimize chip area and power consumption. Therefore, the folding flash structure is utilized to form CADC and FADC in which half number of comparators are reduced through the alternative connections of folding switches between the DAC, CADC and FADC. In the proposed design the folding switches are connected in an NMOS bootstrapping scheme to reduce the turn-on resistance and enhance the charge sharing speed.

Unbalanced-size comparators [1] [4] are widely utilized in conventional dynamic-comparator-based flash structures, where the input pair dimensions of the comparators are designed with a proportional relationship to implement the different built-in thresholds. However, the signal dependent kickback noise effect becomes more complex and serious. Thus, to overcome this problem, an embedded threshold calibration technique with gain loss compensation is proposed here, where the uniform-sized dynamic comparator can be employed in the sub-flash ADCs to reduce the kickback noise and the process mismatch variation.

IV. EMBEDDED THRESHOLD AND GAIN LOSS CALIBRATION

Fig. 3 shows the comparator threshold calibration scheme of the CADC with gain loss compensation. The input sampling capacitive DAC is also used as reference generator in the calibration mode. During the calibration, the thresholds of CADC comparators, i.e., $V_{RC1,P,N}$ to $V_{RC7,P,N}$, are generated by bottom-plate switching with supply V_{DD} and ground V_{SS} in the 4-bit capacitive DAC array, and they are embedded as the thresholds of the comparators through the calibration circuit one by one. Since the top-plate voltage of the DAC suffers from parasitic gain ratio A_C, the embedded gain ratio of the CADC comparator thresholds is related with the gain loss of the input signal during ADC quantization and thus the gain loss is compensated.

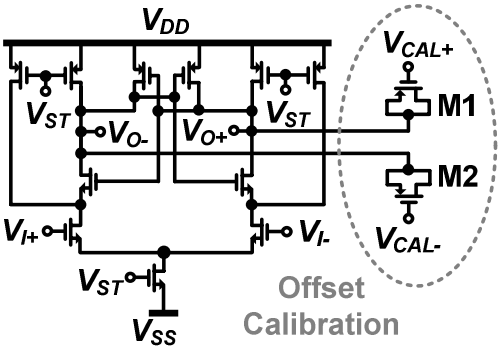

Fig. 4. Uniform-sized dynamic latch-type comparator.

Since the capacitive DAC is reused this leads to a very compact hardware design. The matching of the DAC is designed to be above 8-bit for the resolution requirement, and the capacitance C_{DAC} is designed as 400fF in order to tolerate the layout parasitic gain loss and comparator kickback noise. Similar to CADC, reference voltages of FADC are generated in the DAC with the gain ratio A_F, which are embedded as the thresholds of fine comparators. Besides, there is a 4-bit reference ladder to co-work with the 4-bit DAC to generate the fine thresholds of the FADC, which are powered off after the calibration.

Fig. 4 shows the schematic of the uniform-sized dynamic latch-type comparator. To reduce kickback noise and achieve higher power efficiency, the transistors' sizes of the comparator's input pairs are uniform and minimized but attaining the requirements of speed and thermal noise. Furthermore, the offset of the comparator is seen as a deviation in the threshold, which is also calibrated to the specified reference voltage, simultaneously, through the embedded threshold calibration scheme mentioned above. The offset and reference embedding is adjusted by the capacitive loading [1] at the output of the comparator, where the gate voltage V_{CAL+} and V_{CAL-} of PMOS M1 and M2 are addressed with a monotonic resistive ladder to change the loading capacitance of the comparator. Since the total parasitic capacitance at the top-plate of the DAC is approximated to 50% of C_{DAC}, after the layout routing, the signal swing is decreased by 33%. Thus, the resolution of the calibrated comparators must be over 8-bit. Monte Carlo simulations show that the maximum comparator offset before calibration is up to 35mV and after calibration it is reduced to 0.5mV, which is small enough to meet the requirement.

When compared with transistors, the passive elements such as the resistor and the capacitor are more reliable to achieve better matching properties due to their linear characteristics. In this design, the reference voltages are generated from the capacitor DAC array to be embedded as the thresholds of the comparators. Moreover, and different from the gate-weight [1] and imbalanced [4] comparator

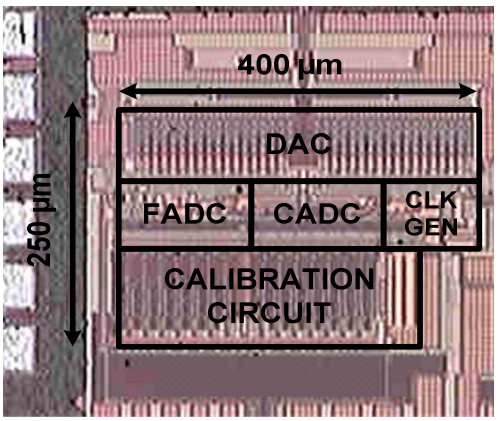

Fig. 5: Chip micrograph.

techniques, the size of all comparators is uniform, hence the kickback noise effect can be reduced, the trip points of comparators can be less sensitive to the process variation, and the layout can be more compact.

V. Measurement Results

The prototype ADC was implemented in a 65nm standard CMOS process. Fig. 5 shows the die photograph. The active area is $0.1mm^2$ counting with the calibration circuit. The ADC has a full-scale input range of 1.2Vpp differential. During the measurement, the B8 of FADC is regarded as an additional bit to reduce the quantization noise power by a factor of 4. Fig. 6 shows the measured static performance. Before activating the calibration, DNL is -1.0/+12.5 LSB and INL is -10.0/+12.7 LSB. After calibration, DNL and INL become -0.63/+0.63 LSB and -0.95/+0.76 LSB, respectively. Fig. 7 shows the measured FFT plot with 27MHz input and 300MHz sampling frequency. Fig. 8 and Fig. 9 illustrate the SNDR and SFDR of the ADC versus input and sampling frequencies. At the speed of 300MS/s, the ADC achieves peak SNDR of 40.5dB, peak SFDR of 51dB, and ERBW of 300MHz. At the maximum conversion rate of 400MS/s, the SNDR is 39dB, consuming 2.7mW under 1.2-V supply. The power dissipation is 2.3mW at the sampling rate of 300MS/s. The analog power, including the comparators, calibration reference ladders and capacitive DAC array is around 0.8mW and the digital power is 1.5mW. Table I compares the present design with the state-of-the-art 7b+ 200M+S/s ADC architectures, previously reported, exhibiting a competitive FOM.

VI. Conclusions

The 7-bit 300MS/s subranging ADC achieves high compactness and power efficiency with the proposed on-chip digital calibration techniques. Uniform-sized dynamic comparator with built-in thresholds presents alternative techniques to realize a low-power flash ADC topology with less nonlinearity, complexity and power consumption. The design achieved a significant FoM of 44fJ/conv. comparable to state-of-the-art ADCs.

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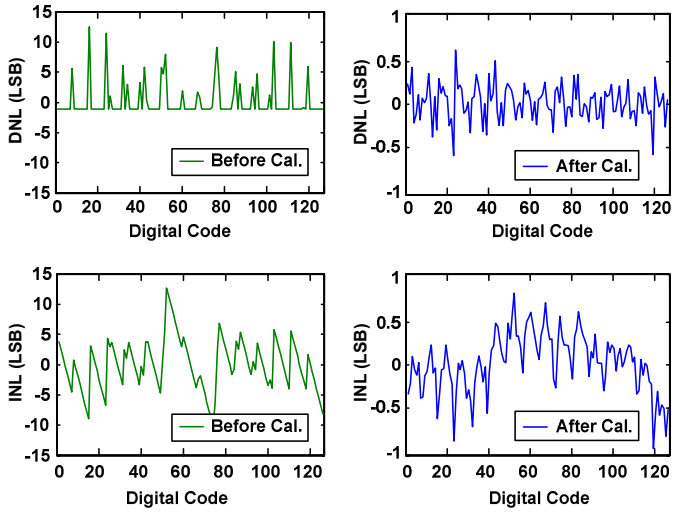

Fig. 6. Measured DNL and INL before and after calibration.

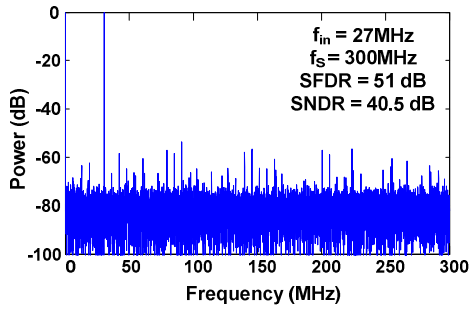

Fig. 7. Measured output spectrum of the ADC with f_S = 300MS/s

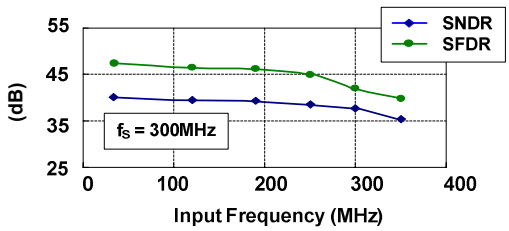

Fig. 8. SNDR & SNFR vs. input frequency.

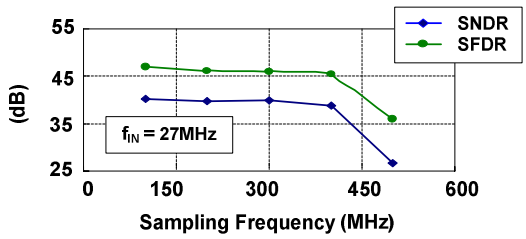

Fig. 9. SNDR & SFDR vs. sampling frequency.

TABLE I: Comparison to the state-of-the-art ADCs.

	ISSCC'08 [2]	JSSC'09 [3]	ISSCC'09 [5]	CICC'10 [6]	ISSCC'11 [7]	This Work	
CMOS Process	90 nm	90 nm	130 nm	65 nm	65 nm	65 nm	
Resolution	8-bit	8-bit	8-bit	10-bit	8-bit	7-bit	
Speed	300 MS/s	770 MS/s	600 MS/s	204 MS/s	400 MS/s	300 MS/s	400 MS/s
ERBW	250 MHz	700 MHz	300 MHz	78 MHz	130 MHz	300 MHz	350 MS/s
Peak SNDR	46.3 dB	43.6 dB	46.7 dB	55.2 dB	44.5 dB	40.5 dB	39 dB
Power	34 mW	70 mW	30 mW	9.15 mW	4 mW	2.3 mW	2.7 mW
$FOM_1 = P/(2^{ENOB} \cdot f_S)$	680 fJ/conv.	940 fJ/conv.	208 fJ/conv.	95 fJ/conv.	73 fJ/conv.	88 fJ/conv.	93 fJ/conv.
$FOM_2 = P/(2^{ENOB} \cdot 2 \cdot ERBW)$	403 fJ/conv.	404 fJ/conv.	340 fJ/conv.	124 fJ/conv.	112 fJ/conv.	44 fJ/conv.	53 fJ/conv.