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AN EXPERIMENTAL 1.8 μm CMOS ANTI-ALIASING SWITCHED-CAPACITOR DECIMATOR WITH HIGH INPUT SAMPLING FREQUENCY

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Abstract: An optimum anti-aliasing switched-capacitor (SC) decimator is capable of achieving a high input sampling ratio while employing operational amplifiers operating at a much lower frequency than what would be needed in conventional SC filtering circuits.This is demonstrated considering the design of a 2nd. order SC decimator building block which has been realised in a 1.8μm CMOS double-poly technology, and achieves a frequency decimation capability from 16.59MHz to 5.53MHz with a total power consumption of only 1.75 mW. The experimental evaluation of the resulting performance behavior has been carried-out not only with respect to the non-ideal characteristics of the amplifiers but also with respect to the errors which may occur associated with the switch timing controlling the operation of the circuit.

1. INTRODUCTION

One of the strategic research goals of analog signal processing technology is the design of high frequency and very high frequency circuits and systems, mainly for applications in video signal processing, mobile communications and high speed data transmission [1]. Significant efforts in this area have been devoted to extend the operation frequency of SC filters towards increasingly higher frequencies, and they have been mainly oriented to either optimize classical circuit techniques and architectures in conventional CMOS technologies [2-4] or to explore new circuit concepts using intrinsically faster technologies such as GaAs and advanced CMOS processes [5, 6]. It has also been suggested in recent work that the development of optimum multirate SC decimating and interpolating techniques could push even further the limits of operation of such circuits. In fact, such techniques make it possible to obtain SC circuits with a sufficiently high ratio between the sampling frequency and the maximum signal frequency of interest without increasing the speed requirements of the amplifiers which can always operate at a frequency compatible with state-of-the-art technologies [7, 8]. Hence, SC decimator and interpolator building blocks have a great potential for high-frequency applications, and, particularly, for those requiring a filtering function together with a sampling rate alteration.

The purpose of this paper is to experimentally characterize and demonstrate the practical feasibility of one such SC decimator building block, and discuss the practical advantages which can be gained with respect to more conventional SC filtering techniques. The SC decimator with optimum implementation that we have considered in this paper corresponds to a 2nd. order building block with a decimating factor of M=3. This is capable of realising a 2nd. order z-transfer function and provide a sampling rate reduction from an input sampling frequency of $3F_S$ to a lower output sampling frequency of F_S together with the appropriate rejection of the unwanted alias frequency components around F_S and $2F_S$. In this work we have chosen a low value of the decimating factor in order to simplify the corresponding IC realization and the subsequent experimental evaluation and characterization of the effects produced by the non-ideal characteristics of the amplifiers and by errors associated with the switch timing controlling the operation of the circuit. Such circuit has been implemented as an experimental IC using a 1.8μm CMOS double-poly process and is shown to achieve a frequency decimation capability from 16.59MHz to 5.53MHz with a total power consumption of only 1.75 mW.

2. CIRCUIT ARCHITECTURE

The architecture of the SC decimator circuit considered in this paper is shown in Fig.1-a and its operation refers to the switch timing indicated in Fig.1-b which, is divided into two sets of time slots corresponding to time frames A and B. Time slots 3, 4, and 5 in time frame A control the sampling of the input signal at a frequency $3F_S$, which can be rather high provided that the width of the resulting time slots can accomodate the charging and settling of the input capacitors. This can usually be achieved without too much difficulty by designing the input SC branches with very low time constants RC, where C is the value of the branch capacitance and R is the value of the ON resistance of the associated switches. Time slots 1 and 2 in time frame B control the transfer of charge from the input capacitors to the feedback capacitors around the amplifiers. Unlike in the previous situation the speed of such a process of charge transfer is now determined primarily by the settling time of the amplifiers. Hence, for a given switching frequency F_S, the wider we make the width of time slots 1 and 2 the slower we can render the speed of the amplifiers in order to save power and even occupy a smaller area of silicon.

When compared with traditional high-frequency SC biquads [4, 5] the above type of SC decimator circuit is capable of achieving an M-fold increase of the input sampling frequency at the expense of a relatively small additional hardware complexity concerning the required number of SC branches and switching waveforms. This can be of the greatest importance for relaxing the burden placed on the anti-aliasing continuous-time filter and reduce the power consumption of the circuit. For clarity, we indicate in Table 1 a brief comparison between the operating limits and characteristics of traditional SC high-frequency biquad circuits and those which can be achieved using the type of SC decimator circuits shown in Fig.1 and which is experimentally demonstrated in this paper.

3. INTEGRATED CIRCUIT IMPLEMENTATION

According to the methodology reported in [8], we have designed the decimator of Fig.1-a with M=3 and a bilinear 2nd. order Tchebyshev lowpass response with passband ripple of 0.01dB and normalized cut-off frequency of f_C/F_S=0.013. The resulting capacitance values obtained after scaling for maximum signal handling capability and reduced capacitor spread are indicated in Fig.1-c yielding a total capacitor area of only 78.87 units.

Two different architectures were adopted for designing the amplifers required in the circuit. One such architecture, shown in Fig.2-a, consists of a rather simple inverter stage which can achieve very high speeds of operation although with relatively modest values of the DC gain [9]. The second architecture, shown in Fig.2-b, belongs to the class of single-stage folded cascode amplifiers which can exhibit a much larger DC gain at the expense of some speed reduction [9]. To increase even further the amplifier gain some additional transistors have been positioned in the cascode stage, and that can then be viewed as a "triple" cascode architecture. For an experimental 1.8μm CMOS technology [10], Table 2 indicates the simulated performance characteristics obtained for three designs of the amplifiers in Fig.2. All these designs were employed to configure the experimental IC with four different versions of the SC decimator circuit , and thus make it possible to characterize its experimental performance behavior with respect to the non-ideal characteristics of the amplifiers. In order to extend such experimental evaluation to the study of the non-ideal effects associated with the switch timing we have further planned the prototype IC in such a way that both the sampling frequency Fs and the complete switch timing can be externally controlled in order to generate different patterns of the time slots and with different pulse widths.

4. EXPERIMENTAL RESULTS

The photomicrograph of the prototype IC is shown in Fig.3. Testing was carried-out on the SC decimator version composed by OA1=Version 1 and OA2=Version 2.A amplifiers, which has better high speed performance. An experimental board containing all the circuitry necessary to generate the bias current and the biasing voltages for the amplifiers has been develloped, whereas the appropriate switching waveforms were generated by a digital pattern generator. For different values of the input sampling frequency $3F_S$ we obtained the experimental amplitude responses shown in Fig.4. While for the lower input sampling frequency of 1.11MHz these results are very close to the nominal amplitude characteristic of the decimator, for the higher input sampling frequency of 16.59MHz we can observe some deviations both with respect to the passband ripple and to the cut-off frequency. For the latter operating condition the pulse widths are 40ns for time slots 1 and 2, and for time slots 3, 4, and 5 we have 20ns corresponding to the minimum value which could be defined by the available instrumentation. Pulse widths of 40ns are already below the minimum width of 82ns necessary to guarantee the correct settling of amplifier 2 (Table 2) and this, according to results obtained by computer simulations, justifies the observed deviations of the amplitude response. Since much faster amplifiers can be comfortably designed for state-of-the-art CMOS technology [11], the results of Fig.4 suggest that this circuit would be capable of achieving a maximum input sampling frequency of the order of 90MHz with a power consumption of only 60mW, and which is significantly lower than what would be required for a traditional circuit design.

Besides the above characterization of the baseband amplitude response of the experimental anti-aliasing SC decimator circuit as a function of the non-ideal characteristics of the amplifiers, we have also investigated the influence of switch timing errors which might arise in association with the multiple switching waveforms controlling the operation of the circuit. The experimental results indicate that the influence of switch timing errors in the baseband below $F_S/2$ is small, as we would have expected for a conventional SC biquad circuit. For example, errors associated with time slot 2 do not produce modifications of the amplitude response whereas errors associated with time slot 4 will change the amplitude response only if there are frequency notches in the baseband [8, 12]. Above $F_S/2$, this SC decimator is relatively sensitive to switch timing errors associated with the sampling of the input signal [8, 12]. This situation is illustrated by the results presented in Fig.5 and which indicate various amplitude responses obtained when the input signal generator varies from 5.552MHz to 5.752MHz (corresponding to the first aliasing band around F_S=5.53MHz) and the output signals are synchronously detected in the baseband from 20KHz to 220KHz. Fig.5-a represents the nominal response obtained by computer simulation and Fig.5-b represents the measured alias response obtained for the nominal switch timing and for a switch timing error (deliberately introduced) of 20ns delay of time slot 2. Our investigations based on computer simulations suggest that the observed error of nearly 25dB maybe due to high frequency effects associated with the input SC branches and which we were not able to adequately characterize in the laboratory. In practice, the observed error may not be too serious since the alias components around F_S and $2F_S$ will always suffer a complementary attenuation due to the front-end continuous-time filter that must remove the alias components around 3Fs and above. The remaining results shown in Fig.5-c indicate the measured anti-aliasing performance for a switch timing error of 20ns advance of time slot 4. As expected from our theoretical analysis [8, 12], such performance is strongly dependent on the accuracy of time slot 4 and which, being responsible for the modification of the frequency zeroes in the aliasing bands, may lead to significant variations of the level of rejection of the alias components. Similar results were obtained for time slots 3 and 5, and which are also responsible for sampling the input signal. The results obtained for the rejection of the alias components in the 2nd. alias band around 2Fs are consistent with the ones shown here for the 1st. alias band and in agreement with our theoretical predictions [12].

5. CONCLUSIONS

We have demonstrated in this paper the practical feasibility of an SC decimator building block which can achieve a high input sampling ratio while employing amplifiers operating at a much lower sampling frequency than would have been needed in more conventional SC filtering circuits. This is of the greatest importance for relaxing the burden placed on the anti-aliasing continuous-time filter and reduce the power consumption of the circuit. The results obtained through the detailed evaluation of an experimental IC realised using a 1.8μm CMOS technology indicate the robustness of the circuit techniques under non-ideal characteristics of both the amplifiers and the switching waveform generators controlling the operation of the circuit.

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Selectivity 2nd. order	Ribner, Copeland [7]	Martins, Franca
Structure	Biquad (Fs, Fs)	Decimator (3Fs, Fs)
Specifications	fp/Fs = 0.091, Qp = 18	fp/Fs = 0.013, Qp = 0.34
Clock frequency	Fs = 5 MHz	3Fs = 16.59 MHz Fs = 5.53 MHz
1st. Aliasing Component	Fs = 5 MHz	Fs = 16.59 MHz
Type of OA's	Single-Ended	Single-Ended
DC-Gain	69 dB	40 dB and 90 dB
Gain-Bandwidth	70 MHz	80 MHz and 20 MHz
Bias Current	135 μA	75 μA and 125 μA
Total Power consumption	1.35 mW	1.75 mW
CMOS technology	1.25 μm	1.8 μm

Table 1 : Comparison between the implementation of a traditional high-frequency biquad and the 2nd. order decimator .

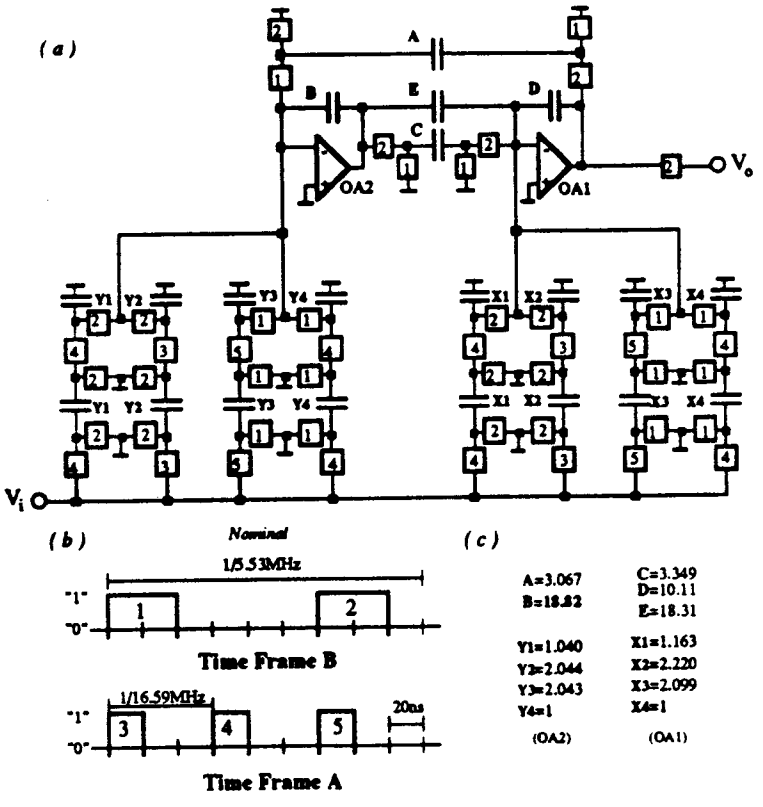

Fig.1 : IIR SC Decimator with M=3.
(a) Circuit. (b) Switching waveforms. (c) Capacitor values.

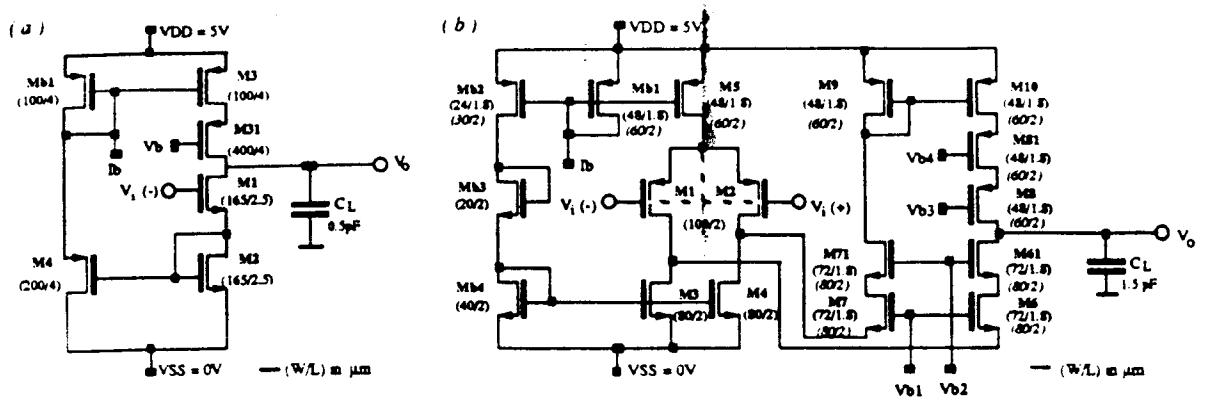

Fig.2 : Architectures of the amplifiers.
(a) Version 1-Single inverter Cascoded.
(b) Version 2.A and 2.B -Folded Cascode.

Characteristics	Version 1	Version2.A (1.8μm)	Version2.B (2μm)
DC-Gain (dB)	40	89	86
GB (MHz)	80	18	15
Phase Margin (CL=1.5pF)	---	65	58
Settling Time (ns)	50	82	87
Input Offset (mV)	---	16	16
Power Cons. (mW)	0.75	0.9	1.1
IC Area (μm) ^{2}	160x140	140x180	150x200

Table 2 : Simulated characteristics of the amplifiers.

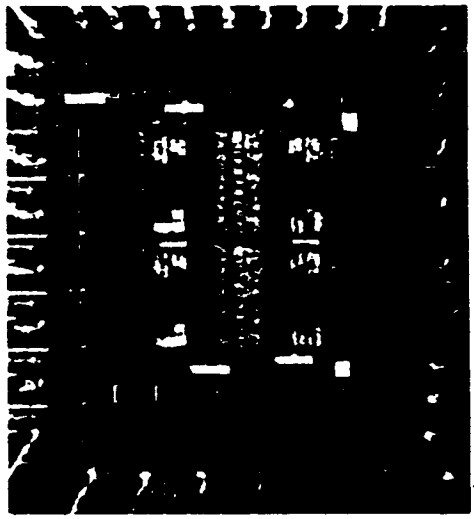

Fig.3 : Photomicrograph of the experimental IC with four versions of the 2nd. order SC decimator.

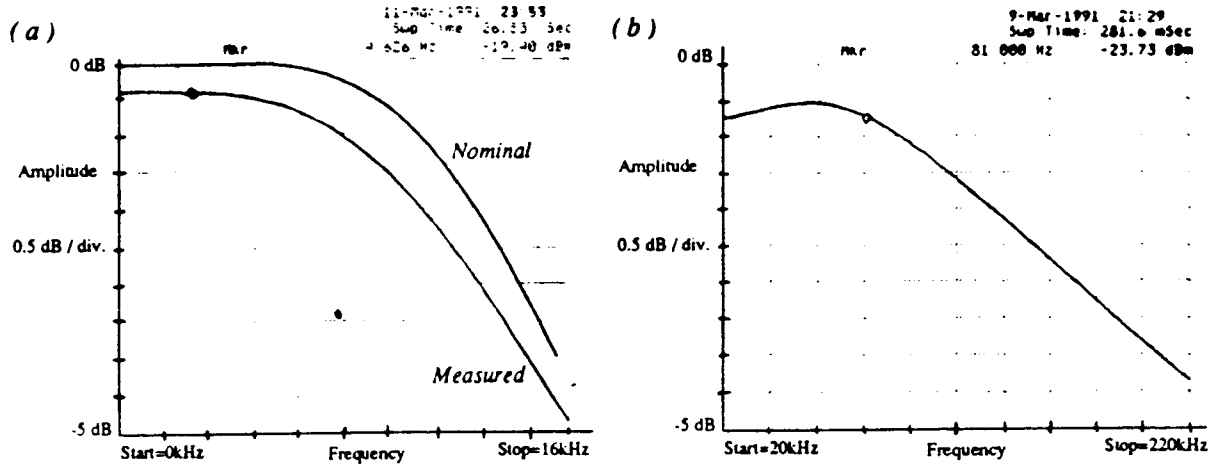

Fig.4 : Baseband amplitude responses of the prototype SC decimator.
(a) Nominal response at 3Fs = 1.152MHz and Measured response at 3Fs = 1.11MHz.
(b) Measured response at 3Fs = 16.59MHz.

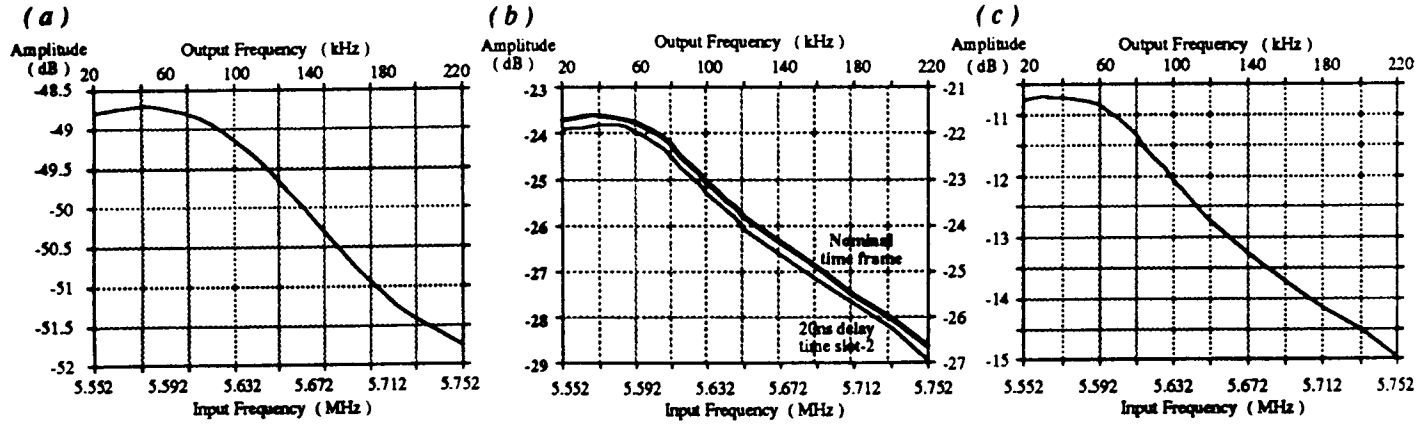

Fig.5 : Amplitude responses corresponding to input frequencies in the 1st. aliasing band around Fs=5.53MHz.
(a) Nominal response (Computer simulated with real OA's). (b) Measured response with nominal time frame (presented in Fig.1-b) and with 20ns delay of time slot 2. (c) Measured response with 20ns advance of time slot 4.