A Dual-VCO-Based Quantizer with Highly Improved Linearity and Enlarged Dynamic Range

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***Abstract*— In this paper, a novel structure of dual-VCO-based quantizer is introduced to significantly improve the VCO linearity. Compared with the precedent methods, the proposed structure can accomplish the linearity without sacrificing the intrinsic DEM function of the VCO-based quantizer, which greatly simplifies the structure of the circuit implementation. Moreover, a passive adder is introduced in this paper, instead normal active adder; the power consumption can be optimized. Besides, due to the dual-VCO structure, the dynamic range of the modulator can be greatly enlarged. A first order continuous-time (CT) sigma-delta (ΣΔ) modulator with the proposal quantizer is designed and simulated in 65 nm CMOS process. The performance of the modulator can reach 83.7/83 dB SNR/SNDR with 10MHz bandwidth and 1V supply voltage.**

I. INTRODUCTION

Recently, in order to achieve high-speed, high-resolution signal modulation with ΣΔ modulator, increasing people place their attention on the usage of voltage-controlled oscillator (VCO), which has the attribution of explicit one-order noise shaping function and high-bit quantization. However, the VCO-based quantization has some serious limitations which dramatically influence its performance; most of all is the VCO nonlinearity. Till now, several methods have already been designed to suppress this most serious influence. In [1], a pseudo-differential architecture is implemented to minimize the nonlinearity; however, the effect is not so obvious; [2] made efforts to reduce the tuning range of quantizer inputs, by which it can get a better linearity of voltage-to-frequency tuning curve, nevertheless, the tradeoff of this method is the limitation of the dynamic range; in [3], a feedback path is introduce into the VCO-based quantizer and the VCO nonlinearity is almost perfectly minimized; however, the idea sacrifice the VCO intrinsic Dynamic Element Matching (DEM) function and introduce the explicit Dynamic Weight Averaging (DWA) which significantly complex the circuit implementation.

In this paper, a dual-VCO-based quantizer is implemented which can significantly improve the linearity of VCO-based quantization; moreover, it can maintain the intrinsic DEM function, which greatly simplify the structure of the circuit structure. Furthermore, the dynamic range also gets obvious improvement in this design.

A first order sigma-delta modulator is designed in the circuit level to test the dual-VCO-based quantizer. The modulator structure presented which operates at a clock rate of 1.15GHz, achieves an SNR/SNDR of 83.7/83 dB in 10MHz of input bandwidth with 1V supply in 65 nm CMOS.

We begin by providing some basic theories of the VCO-based quantizers in section II. In section III, we point out our proposal structure of the modulator with the dual-VCO-based quantizer, the passive adder and some other circuit implementation. Section IV provides the simulation results and, finally, a conclusion in the section V.

II. REVIEW OF VCO-BASED QUANTIZATOR

Fig.1 illustrates a second order continuous-time (CT) ΣΔ modulator model with VCO-based quantizer, which identifies its behavior as an ideal integrator with an input signal in voltage and an output signal in phase.

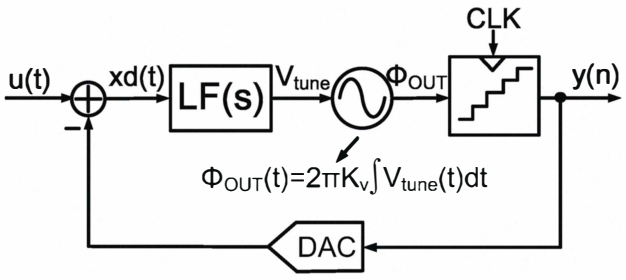

Fig.1 second order continuous-time ΣΔ modulator model

The internal structure of VCO-based quantizer shown in Fig.2 uses the multi-phase ring oscillator to achieve the voltage-to-frequency conversion with highly digital implementation. As revealed in [2], the D-flip flops and XOR gate perform as the counters and the register (with no reset)

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that allows high speed operation with small latency, which are important characteristics when placing the VCO-based quantizer within a CT ΣΔ modulator structure. Another benefit is its intrinsic ability to realize 1st order noise shaping, because that the truncation error at the end of a clock period boundary is not lost, but rather it is accounted for in the following measurement. Thereby, the Noise Transfer Function (NTF) introduces the additional $(1-Z^{-1})$ as the first order difference, which corresponds to comparison of the register values to their previous sample values by the XOR gates. As VCO converting the tuning voltage to its corresponding phase signal represents as an integrator with gain $2\pi K_v$; then, the following differential operation achieves the conversion from the VCO phase signal to frequency signal.

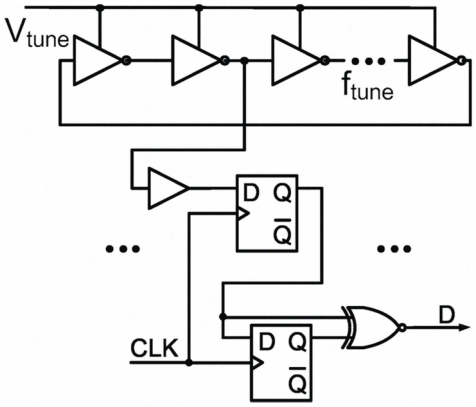

Fig.2 Internal structure of VCO-based quantizer

Another significant advantage of VCO-based quantizer structure in the CT ΣΔ modulator is the barrel shifting characteristic. Note that the output of XOR gates array in the thermometer-code, thus there is no need of DWA operations for the data outputs. With direct connection of quantizer outputs to the DAC inputs, the ΣΔ feedback loop provides implicit DEM of the DAC element which can noise shape the impact of mismatch between the DAC elements. Therefore compared with classical comparator-based quantizer with DWA, the circuit can be greatly simplified.

However in practice, the linearity of the voltage controlled ring oscillator still has some serious limitations which dramatically affect the performance of the modulator. One of the most is the impact of its nonlinearity which introduces harmonic distortion which can significantly degrade the SNDR performance of quantizer. Further test within the CT ΣΔ modulator shows that this nonlinearity will enlarge the noise floor for the increase of the mismatch and nonlinearity in DAC feedback. As the input range of VCO-based quantizer increases, this effect becomes even worse. In short, the nonlinearity of VCO-based quantizer has always been considered as the largest bottleneck to achieve high resolution for VCO-based quantizer. In order to minimize the nonlinearity of the VCO-based-quantizer, we discover a novel method which significantly improves the linearity of the quantizer.

III. PROPOSAL VCO-BASED SIGMA-DELAT MODULATOR

In this paper, we figure out a method which can significantly improve the linearity of the VCO-based quantizer. Unlike the precedent papers[1], [2], [3], the proposed structure does not need to limit the input swing or sacrifice the intrinsic DEM function, using newly introduced DWA instead, or be help with some off-chip calibrations. Therefore, compared to these former works, it is obviously that our proposal structure has the advantages of large dynamic range and simple circuit-level structure.

Fig. 3 display our proposed ADC structure, which contain an active loop filter, a dual-VCO-based quantizer with 5-bits (31 level) each, a passive adder and two current DACs. The clock frequency of the ADC is 1.15GHz, high enough to oversample the high frequency of the signal in the ring oscillator.

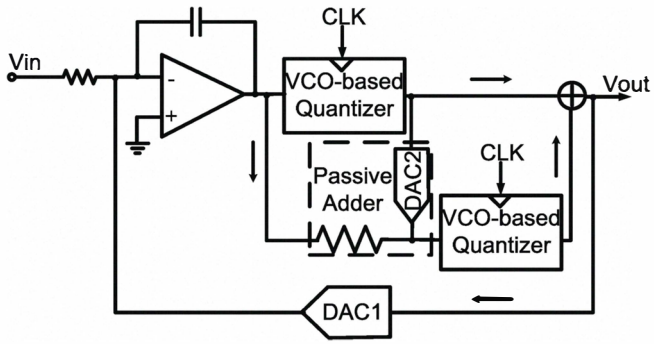

Fig.3 proposed structure with dual-VCO-based quantizer

A. *Dual-VCO-Based Architecture*

In original case, due to only one VCO-based quantizer do the quantization, the nonlinearity of the VCO can dramatically affect the performance of the modulator; the harmonic distortion often rather serious when quantizing large input signal, as a result, making the VCO-based quantizer only suitable for small input swing. The difference between the output of the VCO-based quantizer and the input signal, which caused mostly by the nonlinearity of the VCO, draws our attention that, if we can compensate this difference, the bottleneck of the nonlinearity can be eliminated. In our proposed structure, with the passive adder, which explained later, the subtraction of the input and the output of the 1st VCO-based quantizer can be accomplished, and the difference can directly quantized by the second quantizer, which produce digital signals correspondingly. After that, in the digital part, these two quantization results can be easily added together and, therefore, the nonlinearity of the VCO-based quantizer is perfectly minimized. We should notice that, although, as a counterpart of the first one, the second VCO-based quantizer also has the problem of the nonlinearity, in most of the cases, its input signal, the difference, is small enough to ensure the good linearity of the second quantizer.

B. *Passive Adder*

In our ADC, instead of using of some active adder which can cause larger power consumption and the complicity of the circuit, we introduce a pair of resistors to implement the subtraction of the signals; here, we call it "passive adder"

which consists of a path of current feedback and a pair of resistors. As the feedback signal is current-based and it oscillates around the zero synchronously with the output of the quantizer, the passive adder can precisely achieve the adding function without shift the common mode voltage. Furthermore, with the current pass through the resistors, the voltage of the output can be exactly replicated and, finally, the subtraction can be completed.

Here, the multiplication of the resistors and the feedback current value should be properly determined. As the VCO nonlinearity introduce the 3rd harmonic into the system, we suppose the output, y, of the 1st quantizer follows a function shown below:

$$y = ax^3 + bx + c \quad (1)$$

And it is obviously that when the difference value provided by the passive adder reaches to ax^3, the nonlinearity part can be perfectly elimination, which illustrates the best case of this structure. Nevertheless, the value cannot be so matching in non-ideal cases. As the current feedback value is proportional to the output and the resistors' values are constant, the multiplication can be described as:

$$y = k(ax^3 + bx + c) \quad (2)$$

Therefore, the real difference is shown like:

$$y = a(1-k)x^3 + b'x + c' \quad (3)$$

In the Eq.3, as the 1st order and the constant parts do not affect the linearity of the quantizer, we only focus on the coefficient of the 3rd order part which is a function related to the parameter *k*. It is clear that, without making the value *k,* equal to 1 by proper setting of the currents and resistors of the adder, the 3rd harmonic will still introduce to the system. In our circuit, we set the resistor to 560 Ω and the current to 10uA each element.

C. *Feedback DAC*

In our design, we implement the current-based NRZ DAC in our structure. As each stage of the VCO has a current feedback, which promises the accomplishment of the DEM function, the good linearity of the feedback signal without using DWA. In addition, we should notice that, although we implement a dual-VCO-based quantizer in our proposed structure, we use only one feedback path to the loop filter, which obviously due to the current-based feedback that the feedback signals can be easily combined together by connecting to the same point without any help of adders [2].

D. *Loop Filter*

In our structure proposed, we use a single stage active RC integrator, combined with the noise shaping ability of the VCO-based quantizer, to achieve 2nd order noise shaping. With the intrinsic noise shaping ability and the calibrated linearity of the VCO-based quantizer, the gain of the operation amplifier has been greatly released. In the structure, we implement an operation amplifier with 30dB gain, so that the structure of which can be rather simple and, more importantly, the economy of the power consumption can be rather considerable..

IV. MODELING AND SIMULATION RESULT

In the Matlab, we build a model of VCO-based quantizer shown in the Fig. 4. Far from the normal model structure of the ΣΔ modulator, we need to implement the 1st order noise shaping function of the VCO-based quantizer in the Simulink. Here, we use four separate blocks to realize the VCO-based quantizer. From the Fig.4, the combine of the blocks of the nonlinearity, discrete filter, quantization noise and differential realize the function of the noise shaping within the quantization process, in which, the nonlinearity is modeled as a coefficient with a 2nd order term to simulate the 3rd harmonic distortion; the discrete filter plays the role of the integrator which integrate the frequency of the VCO into phase; the introducing of the original quantizer aim to generate the quantization noise; and finally, a differential models is the counterpart of the XOR part of the circuit, which compute the difference of signals in the neighboring periods and, therefore, achieve the noise shaping [4].

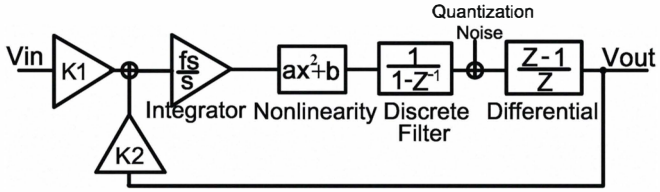

Fig.4 the Matlab model of the proposed 1st order modulator

In our design, we set the k1, k2 to 01 and 0.2 and, for the ideal case, we set the nonlinearity factor, a, to 0, the SNDR can reach 87 dB, which is very close to the calculating value of the 2nd stage ΣΔ modulator. For the non-ideal case, after tuning to match the circuit level design, we set the a equal to 0.3, as a result, the SNDR drops to 60dB, which exactly prove that the nonlinearity of the VCO can dramatically affect the performance of the modulator. The simulation result of the Matlab model is shown in the Fig.5. Interestingly, even without any loop filters, which means merely a VCO-based quantizer in the circuit, it can reach the gain over 60 dB for the ideal case, which clearly verifies the intrinsic noise shaping ability of the VCO-based quantizer.

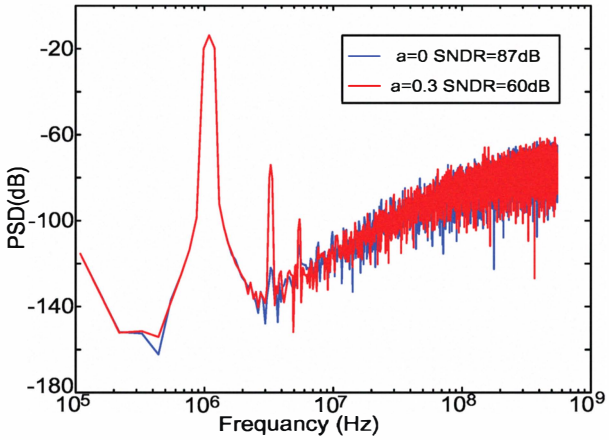

Fig.5 Matlab model results with and without nonlinearity

In the circuit level, we design a first order sigma-delta modulator with the proposed dual-VCO-based quantizer with 65 nm CMOS process. The proposed quantizer is the

combination of two 5-bit VCO-based quantizers which, in total, has 64 single VCO-elements. The loop filter in our proposed structure is only a RC integrator with a operational amplifier with gain of 34dB.

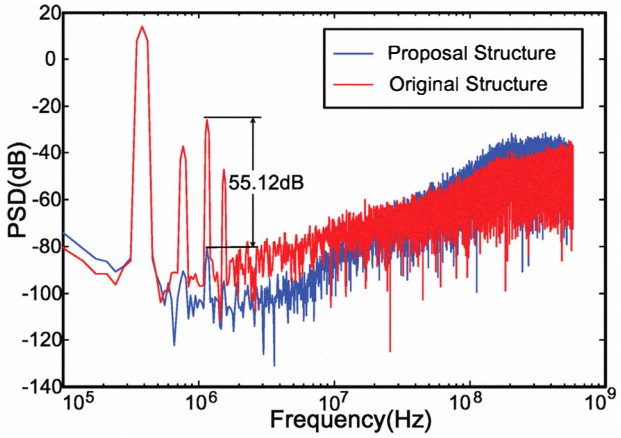

Fig.6 32768 point output spectrum

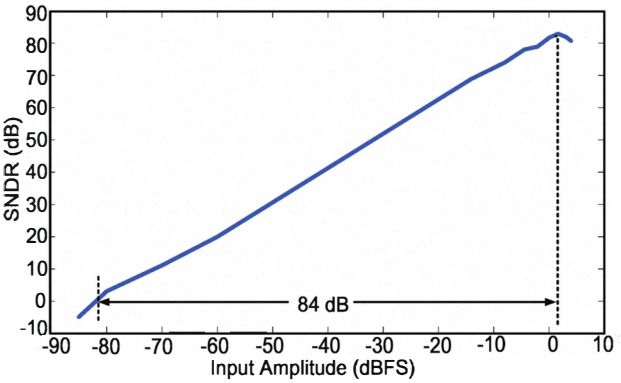

Fig.7 Dynamic range of the proposed structure

TABLE I

SUMMARY OF THE PERFORMANCE OF THE MODULATOR

Specification	Value
Sampling Frequency	1.15 GHz
Input Bandwidth	10 MHz
Supply Voltage	1V
Peak SNR	83.7dB
Peak SNDR	83dB
SNDR Improvement	39.8dB
Dynamic Range	84dB

The output spectrum of both of the original and the proposed ADCs with a 0.386 MHz input signal at 1.6dBFS are collated in the Fig. 6. By the comparison, it is clear that the two results both show an obvious 2nd order noise shaping which verify the function of the noise shaping of the VCO-based quantizer, while the noise floor of the original structure seriously increase by the nonlinearity. From the picture, it is clear that 3rd harmonic distortion of the proposal structure got a significant improvement with a 55.12 dB, and the SNDR of new structure increase 39.8dB compare to the original structure. Finally, with almost perfectly eliminating the interference of the nonlinearity, the SNR/SNDR of the proposal structure reaches 83.7/83dB with a 10 MHz bandwidth and 1.15 GHz sampling frequency.

Fig. 7 shows the dynamic range of the structure proposed, which is greatly enlarged compared to the original one, which verifies the improvement of the dynamic range to 84 dB by using the structure proposed. Finally, a summary of the performances of the proposed modulator is shown in Table I.

V. CONCLUSION

A novel method of the improvement of linearity of the VCO-based quantizer is implemented in this paper. A structure of dual-VCO-based structure is introduced which significant improves the linearity of the VCO-based quantizer and, as a result, the nonlinearity of the VCO is no longer the bottleneck of the achievement of the high resolution. Moreover, the method proposed in this paper does not need the sacrifice of the input swing, instead, it can significantly increase the input swing of the modulator. Besides, this structure of quantizer introduces the intrincis DEM, therefore no extra algorithm of DWA is needed. Thus, the simplicity and power-saveing of the circuit can be accomplished. Finally, a 1st order ΣΔ modulator is designed in this paper, which can achieve a 2nd order noise shaping with the help of the noise shaping ability of the VCO-based quantizer. The loop filter of the modulator only contains a simple RC integrator with relatively low gain of the interior operational amplifier, which uncontroversialy implys a low-level power consumption, also the simplicity, of the operational amplifier design. The CT ΣΔ modulator using a pair of 5-bit VCO-based quantizers in 65nm CMOS process can reach the SNR/SNDR of 83.7/83 dB in the 10 MHz bandwidth, under the supply voltage of 1V and with the sampling rate of 1.15 GHz.

ACKNOWLEDGMENT

This work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT).

REFERENCES

[1] Young-Gyu Yoon, Min-Chang Cho, SeongHwan Cho, "A linearization technique for voltage-controlled oscillator-based ADC," IEEE ISOCC, 2009 , pp: 317 – 320.

[2] Matthew Z. Straayer and Michael H. Perrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 4, APRIL 2008.

[3] Matthew Park and Michael H. Perrott, "A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time ΣΔ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 um CMOS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 12, DECEMBER 2009.

[4] Gaber, W.M., Allam, M., Aboushady, H., Louerat, M., and Eid, E., "Systematic design of continuous-time ΣΔ modulator with VCO-based quantizer," IEEE ISCAS, 2010 , pp: 29 - 32