Multi-Merged-Switched Redundant Capcitive DACs for 2b/cycle SAR ADC

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***Abstract*—This paper introduces a novel switch approach for redundant capacitive DACs of a 2b-per-cycle SAR ADC. By using the proposed multi-merged switching algorithm, the conventional trial-and-error search procedure is prevented, which leads to significant switching energy and DAC settling time reductions. The conversion power and speed analysis are presented, which is also verified in behavior simulations of a 6-bit 2b/cycle SAR ADC. The simulation results show that the proposed method can achieve about 37% power saving as compared to the conventional one.**

I. INTRODUCTION

A short-distance, high-bandwidth communications in Ultra-Wide-Band (UWB) receivers make use of the Analog-to-digital converters (ADCs) to operate at sampling rate over 500MHz with low resolutions up to 4-6 bit. Flash ADC architecture is commonly used due to high conversion speed and simplicity, however it suffers from large power consumption and offset errors in the comparator array. Hence the successive approximation register (SAR) ADC implemented with time-interleaved [1] or multi-bit [2] scheme becomes a compromise solution to achieve power efficiency for high speed applications. In order to reduce the power and die area, a 2b/cycle resistive–ladder based SAR ADC [3] is developed which implemented with interpolation principle to save the number of capacitive networks. However, the switch-selected resistive network requires complex digital control logic and may process long propagation delay that increases the DAC settling time.

To further enhance the power efficiency and speed up the DAC settling, researches [4][5][6] have been done to improve the switching energy efficiency for single channel SAR ADC. In this paper, we propose a multi-merged switch algorithm for a 2b/cycle SAR ADC, which is applied to two redundant capacitive DACs to perform the SA comparison. The monotonic switching sequence of bits capacitor prevents the conventional energy-inefficient switching of the capacitive DACs, thus, the switching energy of DAC array can be significantly reduced. Moreover, the method prevents the large switch transient during each 2-bit-cycling, which speeds up the DAC settling and improves the conversion accuracy. The simulation results show that the proposed switching method can reduce about 37% switching energy of the conventional one.

II. OVERALL ADC ARCHITECTURE

Fig.1 illustrates the 6b 2b/cycle SAR ADC architecture based on the interpolation technique. The structure is composed of two capacitor networks, 3 comparators and SAR control logic. The capacitor network includes the sample-and-hold (S/H) circuit and a fully differential redundant capacitive DAC array. Based on the binary search algorithm, the two capacitive networks are responsible for generating two differential reference voltages $1/4V_{ref}$ and $-1/4\ V_{ref}$ before the 1st bit comparison, and by interpolating the positive side of the first capacitor network V_{OP1} and the negative side of the second capacitor network V_{ON2}, the middle reference level is obtained. Then the input voltage is compared with the three reference levels and results in a thermometer code at three comparators' output. The SA control logic, which combines shift registers, bit registers and switching logic, is responsible for feeding back the 2-bit comparison result to the capacitive arrays, synchronously the next differential reference levels are generated for the next 2-bit conversion. The process is repeated for the other bits moving towards the LSB, until all the bits are determined and decoded into 6b binary format.

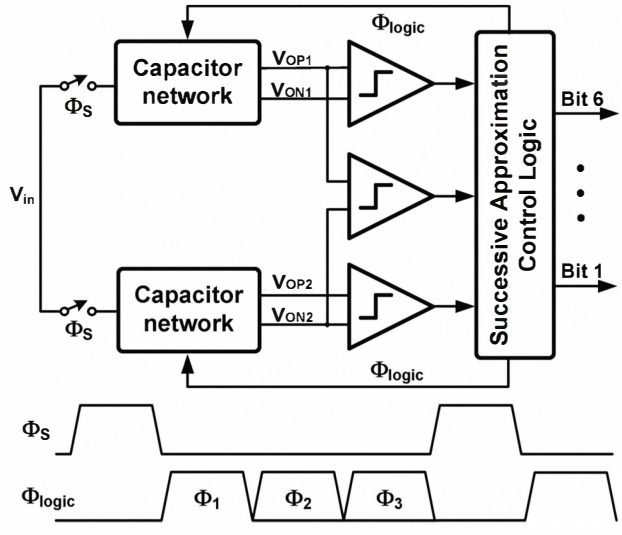

Fig. 1 6b 2b/cycle SAR ADC architecture and timing diagram.

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III. PROPOSED MULTI-MERGED SWITCHING METHOD

To demonstrate the proposed switching approach, a 6-bit example of the conventional and proposed 2b/cycle SAR ADC is shown in Fig.2. Note that the capacitive arrays are controlled by the thermometer code output from three comparators. The usage of a thermometer-code based capacitive DAC (CDAC) prevents the complex decode logic to control a binary-weighted CDAC. The solution allows the CDAC directly controlled by the comparators' output, which saves large digital propagation delay, thus speeding up the bit cycling. Thanks to the V_{cm}-based switching approach [5], the overall capacitance of the both capacitor arrays is half of the conventional counterpart.

The conventional switching method is seen from Fig.2 (a), where "↑" and "↓" represent the capacitor is charged and discharged respectively, and "~" means the maintenance of the previous state. During the sampling phase Φ_s, all capacitors are connected to V_{cm}, and the input is directly sampled onto the top-plate of the DAC, resulting in the output voltage

$$V_{out}[1] = V_{in}. \tag{1}$$

Then, in the phase Φ_{p1}, the first 2-bit comparison begins by pre-charging the MSBs capacitor C7 and C6 to V_{ref}, while keeping the other capacitors connected to V_{cm}. Thus the DAC output will finally settle to

$$V_{out}[2] = V_{in} + V_{ref}/4. \tag{2}$$

Since two reference levels are required to perform the 2bit/cycle conversion, the MSBs of the second CDAC will discharge to *Gnd*. To simplify the description, only the one of the DAC's operation will be presented. The first 2 bit decision is made by comparing V_{in} with three reference levels, $-1/4V_{ref}$, 0 and $1/4V_{ref}$ via three comparators. If $V_{in}<-1/4V_{ref}$, the three comparators' output will be "111". Thus, C5 is charged up by *1/2Vdd* level, i.e. from V_{cm} to V_{ref}, resulting in the DAC output $(V_{in}+3/8V_{ref})$. Simultaneously, C4 and C3 are pre-charged up to generate a $-1/16V_{ref}$ reference level for next 2b comparison. The above operation will continue until final 6 bit digital output is obtained. Fig.2 illustrates four cases of comparator output logics corresponding to their switching sequence. It can be found that some switching cases of bits capacitor are quite energy inefficient. For example, when the comparator output is equal to "011", according to the switching sequence shown in Fig.2 (a), the "up" and "down" transitions happening in C7, C5, C4 and C3, will cause the charge stored in C7 to be redistributed in C5, C4 and C3. In fact, it is not necessary, since discharging C7 leads to the change of the DAC's output by $\Delta V_1=-1/4V_{ref}$, while charging C5, C4 and C3 results in output voltage changing by $\Delta V_2=3/16V_{ref}$. Consequently, the above operation will lead to the output of the DAC finally settle to

$$V_{out}[3] = V_{out}[2] + \Delta V = V_{in} + 3/16V_{ref} \tag{3}$$

where $\Delta V=\Delta V_1+\Delta V_2=-1/16V_{ref}$. In fact, the equivalent output can be directly achieved by simply discharging a capacitance of 4C from V_{cm} to *Gnd*.

According to the above discussion, we propose a multi-merged switching method for redundant CDACs to improve the switching efficiency. As shown in Fig. 2 (b), by splitting the C5 and C2, as

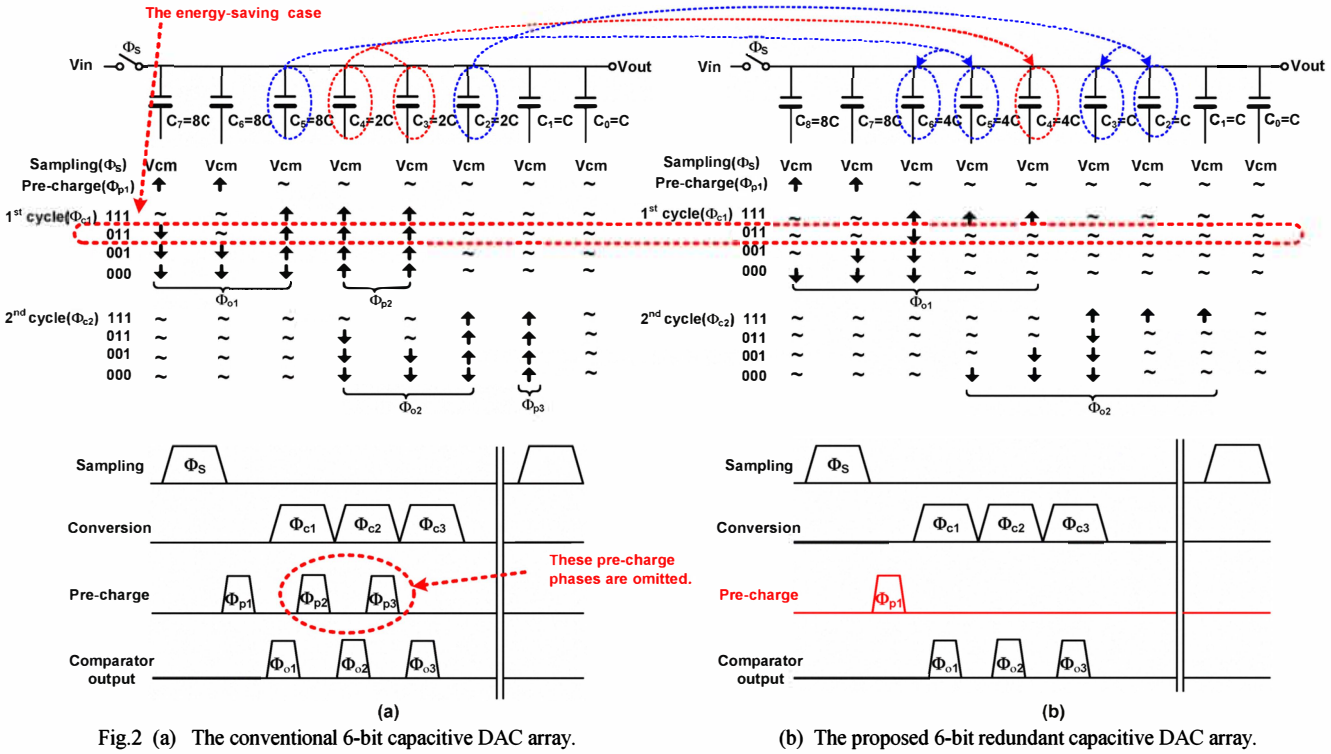

Fig.2 (a) The conventional 6-bit capacitive DAC array. (b) The proposed 6-bit redundant capacitive DAC array.

well as merging C4 and C3 in conventional DAC, a redundant CDAC is obtained to perform the multi-merged switching. During the sampling phase, V_{in} is directly sampled onto the top-plate of the DAC as that was done conventionally. Then the conversion begins by charging up the C7 and C8 to V_{ref} while keeping the other capacitors connecting to V_{cm}, which results in the DAC's output $V_{out}[2]=V_{in}+1/4V_{ref}$. If the comparators' output equals to "011", the SA logic will only control C6 to be discharged , and leave C8, C7, C5 and C4 maintaining the previous state. The proposed switching algorithm prevents the conventional charge-inefficient operation in C8 to C4, which smartly switches the minimum number of bits capacitance to obtain the same final DAC output for the next 2-bit comparison. Accordingly, the pre-charge phases in conventional method shown in Fig.2 (a), will be no longer needed in the following conversion process.

IV. Analysis of Conversion Power & Speed

The proposed multi-merged switching can enable the monotonic sequence to control the bit capacitors, which are charged up as the final desired DAC's output goes high, or charged down as it goes low. To further verify the proposed switching method that is superior to the conventional one, the power and speed analysis of the two switch approaches will be presented in this section.

Considering the case "011" in 1st conversion cycle, where the conventional switching method requires to charge up C5, C4 and C3 from V_{cm} to V_{ref} , and discharge C7 from V_{ref} to Gnd. Accordingly, the switching energy can be expressed as

$$E_{up} = -12CV_{ref}[(V_{out}[3]-V_{out}[2])-(V_{ref}-V_{cm})] = 27/4CV_{ref}^2 \quad (4)$$

$$E_{ref} = -8CV_{ref}(V_{out}[3]-V_{out}[2]) = 1/2CV_{ref}^2 \quad (5)$$

$$E_{conv} = E_{up}+E_{ref} = 29/4CV_{ref}^2 \quad (6)$$

where E_{up} is the energy required to charge up the capacitors, and E_{ref} is the energy drawn from the capacitors kept connected to V_{ref}. Thanks to the charge-recovery implementation [5], there is no switching power drawn from V_{cm} as the DAC operates differentially. Thus, the switching energy discussion of V_{cm} will be omitted.

In the proposed switching method, since there is no "up" transition required in the corresponding comparators output, E_{up} is equal to zero. The E_{ref} consumed by C8 and C7 can be obtained as

$$E_{proposed} = E_{ref} = -16CV_{ref}(V_{out}[3]-V_{out}[2])=CV_{ref}^2 . \quad (7)$$

From (6) and (7), it can be found that the proposed switching method can achieve about seven times lower switching energy than the conventional one. The switching benefit is due to the proposed switching algorithm prevents the conventional pre-charge action of C4 and C3 by a merged operation of the DAC. The final output after switching C6 is corresponding to the combined operation of comparators' decision as well as the pre-charge action. Qualitatively, it can be explained that the proposed switching method achieves the minimum charge transfer according to the final desired DAC output, as the charge that initially stored in C8 and C7 is reused in the next conversion cycles. Note that the total capacitance connected to V_{ref} in (7) is less than the one in (5), which means the power drawn from the supply is also less in the proposed switching method.

The average switching power of conventional switching method can be derived as

$$E_{total,n-bit} = 2^{(n-3)} + \frac{1}{2^n}\sum_{i}^{\frac{n}{2}-1} 2^{(2n-4i-3)}(14\times 4^i - 17)CV_{ref}^2, (n = 4,6,8...) \quad (8)$$

and the average switching energy of the proposed switching method is

$$E_{total,n-bit} = 2^{(n-3)} + \frac{1}{2^n}\sum_{i}^{\frac{n}{2}-1} 2^{(2n-4i-3)}(9\times 4^i - 17)CV_{ref}^2, (n = 4,6,8...). \quad (9)$$

From (8) and (9), it implies that the proposed multi-merged switching consumes much lower switching energy than the conventional one. For a 6-bit 2b/cycle SAR ADC the conventional switching consumes $33.9CV^2_{ref}$ switching power, while the proposed switching consumes only $21.4CV^2_{ref}$, which is about 37% lower than the conventional one.

On the other hand, the switch sequence also affects the DAC's settling, thus limiting the conversion speed of the ADC. Fig.3 shows the simulation result, which compares two DAC's settling time in the case of "011". In the conventional switching, the output voltage of the DAC rises up initially because of the pre-charge actions of C4 and C3. Then, triggered by the comparators' output, C7 is discharged from V_{ref} to *Gnd*, and C5 is charged from V_{cm} to V_{ref}, which causes the voltage drop down by $1/8V_{ref}$. While in the proposed switching, the output voltage is driven down immediately by simply turning down C6 from V_{cm} to *Gnd*. Consequently, the settling time is reduced by 60% as compared to the conventional switching.

In the conventional switching sequence, the conversion is implemented based on the trial-and-error search procedure, which requires pre-charge action before comparators' determination. Then, according to the comparison results, the rearranged control logic will cause the bits capacitors switch simultaneously. The large switching transient leads to the excessive supply voltage undershoot as well as potentially exacerbating an overdrive condition of the preamplifier, which will finally result in a wrong decision on the comparator's output. , On the contrary, free from the trial-and-error search procedure, the proposed switching can predict the "up" or "down" transitions of the capacitors after each 2-bit decision, i.e. if the output voltage is determined to settle to a higher value, appropriate capacitors are selected to be charged up, and vice versa. In any cases, the multi-merged switch algorithm can drive the DAC's output to directly settle to a right voltage, thus achieving much less settling time than the conventional one.

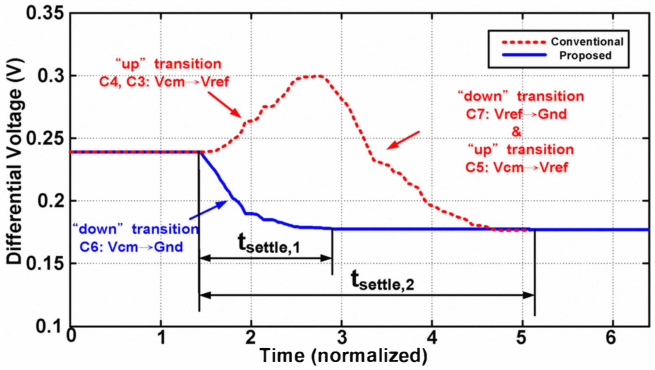

Fig.3 Simulation of the settling time of the proposed and conventional switching methods.

V. Simulation Results

To verify the power-efficiency of the proposed switch method, behavioral simulations of a 6-bit 2b/cycle SAR ADC are performed. The value of unit capacitor is Gaussian random variables with standard deviation of 3% and the ADC is otherwise ideal. Fig.4 shows the energy comparison of conventional and proposed methods. The given figure assumes equal unit capacitor and total array capacitance. The overall switching energy is output digital code dependent, where the proposed switch method can achieve the most energy saving in interval B. The energy saving in interval A and C is around 20%, while the interval B grants 2 times more. This happens because there are more energy-saving cases occurring during SA conversion, where the comparators' output equals to "001" and "011". Otherwise, when the comparators' output equals to "111" and "000", the energy consumed in two methods are almost the same.

Fig.5 shows the 100-times Monte-Carlo capacitor mismatch simulation of a 6b 2b/cycle SAR ADC, where the average SNDR of the ADC is 37.6dB. The differential-non-linearity (DNL) and integral-non-linearity (INL) shown in Fig.6 are within ±0. 4LSB and ±0.2LSB, respectively. The simulation results verified the good conversion performance with the implementation of the proposed multi-merged switching method.

VI. Conclusions

This paper reports a novel switch method to optimize ADC's power and speed while performing 2b/cycle SA comparison. The proposed multi-merged searching algorithm was implemented in redundant capacitive DACs, which allows a monotonic switching operation in each 2-bit cycling. The conversion power and speed analysis as well as the verification of the behavioral simulations clearly demonstrate the effectiveness of the proposed method.

Acknowledgment

This work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT).

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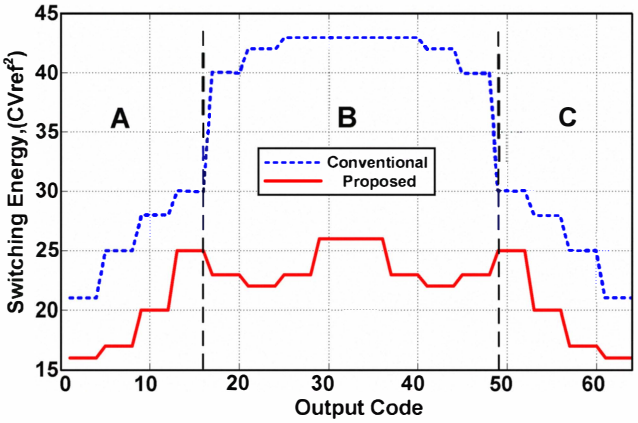

Fig.4 The energy versus output code for different switching methods.

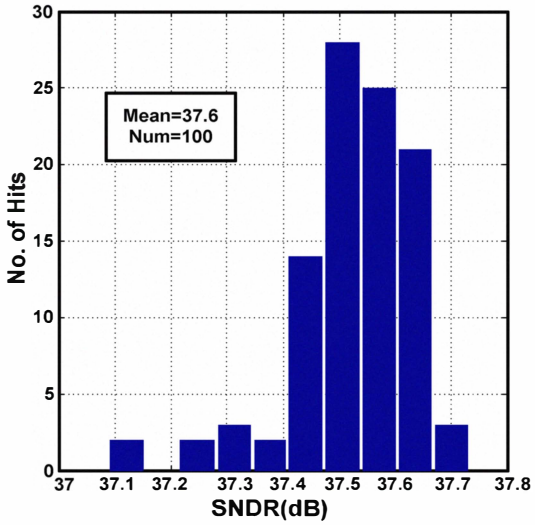

Fig.5 100-time Monte-Carlo simulation of 6b SAR with the propose switching method.

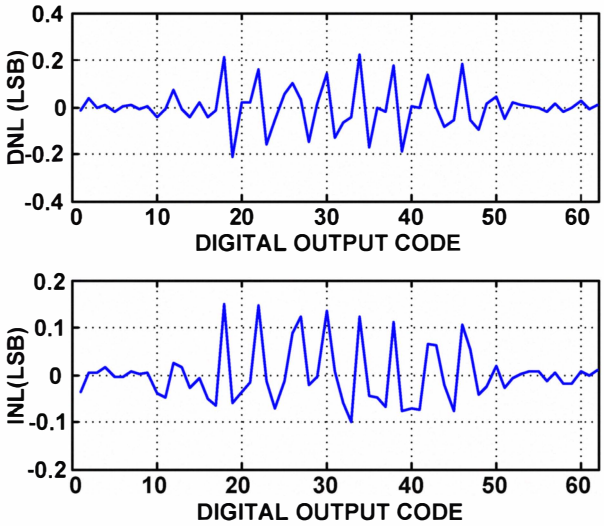

Fig.6 Simulated DNL and INL of the 6b SAR ADC.