Noise Shaping Implementation inTwo-Step/SAR ADC Architectures Based on Delayed Quantization Error

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***Abstract*—Noise shaping can aid ADC architectures to achieve high resolution. A new technique to increase ADC resolution is presented in this paper. It is based on Nyquist-rate ADC architectures and uses delayed analog quantization error to implement noise shaping function. The new technique is implemented using two-step and SAR ADC respectively. When the noise shaping order is one and the Over-Sampling Rate (OSR) is only 8, the system based on 5-bit two-step ADC can achieve the SNDR of 62.5-dB, while the SNDR of the system based on 6-bit SAR ADC can obtain 59.6-dB. Actually, this new technique consumes tiny amount of extra power. Although the speed of the system is decreased slightly because of the small OSR, as the resolution is increased significantly. As a result, the Figure of Merit (FOM) of the overall ADC can be improved.**

***Index Terms*— Nyquist ADC, over-sampling ADC, noise shaping**

I. INTRODUCTION

It is well known that data converters work at the interface of the analog and digital worlds, so the ADC plays a very important role in the electronic world. With many years of research, several kinds of ADCs had been developed, such as flash ADC, SAR ADC, two-step ADC, sigma-delta ADC. Furthermore, these ADCs can be classified in two main categories: Nyquist-rate ADC and over-sampling ADC [1].

As is well-known, sigma delta modulation, which is used in the over-sampling ADC, is the effective way to obtain high resolution, whose two main characteristics are noise shaping and oversampling. Especially the noise shaping, it is the main element for over-sampling ADC to achieve high resolution. To be specific, the quantization noise is suppressed in the signal band by the noise shaping. Furthermore, the out-band noise will be digitally filtered in order to achieve high resolution.

Actually, the technique of sigma delta modulation has been developed for nearly five decades. In this period, several architectures have been proposed. The single-loop architecture is well-known for its tolerance with non-ideal factors. However, when the order of noise shaping is higher than two, the system becomes unstable and is difficult to implement [2]. The Multi-Stage noise Shaping (MASH) architecture can solve the stability problem. Nevertheless, it is sensitive to the non-ideal factors and it is stringent to analog part. In [3], the author proposed a sturdy-MASH architecture in order to solve this problem, using an op-amp whose open-loop gain is only 35-dB but achieved 74-dB SNDR. And another architecture is single-loop with feed-forward, it succeeds the advantage of single-loop and also reduce the output swing. In this way, it can reduce the power. Whatever architectures have been proposed or improved, the original impetus is to increase the order of noise shaping and to reduce the OSR.

In this paper, we proposed a new technique which is using Nyquist-rate ADC architectures and analog quantization error with delay to implement noise shaping. Firstly, obtain analog quantization error from the Nyquist-rate architectures. And then feedback it to the input of the system through delay arrays for the sake of achieving various order of noise shaping. Finally, the noise shaping will be constructed in two kinds of Nyquist-rate ADC architectures. One is based on 5-bit two-step ADC and the other is based on 6-bit SAR ADC.

This paper is organized as follows. The fundamental knowledge of constructing noise shaping in the Nyquist-rate ADC architecture is discussed in Section II. In Section III, the way of constructing noise shaping in the Nyquist-rate ADC architectures will be presented and the simulation resluts will be provided in Section IV. Conclusions are drawn in Section V.

II. DELAY-BASED NOISE SAHPING

The sigma delta modulator(SDM) has different effects on input signal and quantization error. So the input signal can go through the SDM system directly or just with some delay but the quantization error will be suppressed in the signal band. In a general way, the linear system flow diagram of the SDM is illustrated in Fig. 1. It consists of three main parts: integrator, quantizer and DAC. In Fig. 1, X is the input signal, and Y is the output digital signal. Besides, the integrator is denoted as H, and the quantizer in the SDM is modeled as an additive noise source, Q.

The Z-domain equation of the SDM system is given as below,

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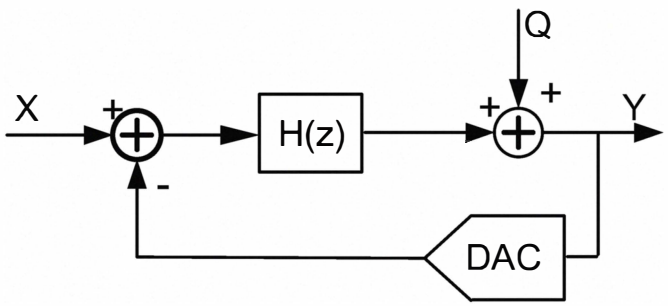

Fig. 1. Traditional SDM structure

$$Y(z) = Z^{-m} \cdot X(z) + (1 - Z^{-1})^n \cdot Q \tag{1}$$

In the eq. (1), m denotes m cycles of delay and n means n-th order noise shaping. The expression of the eq. (1) can be developed into eq. (2) showed as below,

$$Y(z) = Z^{-m} \cdot X(z) + [C_n^0 + C_n^1(-Z^{-1})^{-1} + ... + C_n^i(-Z^{-1})^{-i} + ... C_n^n(-Z^{-1})^{-n}]Q \tag{2}$$

From the eq. (2), it indicates that the noise shaping will be constructed if it can acquire the analog quantization noise from a system and feedback the noise to the input of the system with some delay. And then, the quantization noise will also be suppressed in the signal band. But the input signal will go through the system directly or just with some delay. That means it gives us the opportunity to implement noise shaping in this way. This concept is depicted in Fig. 2.

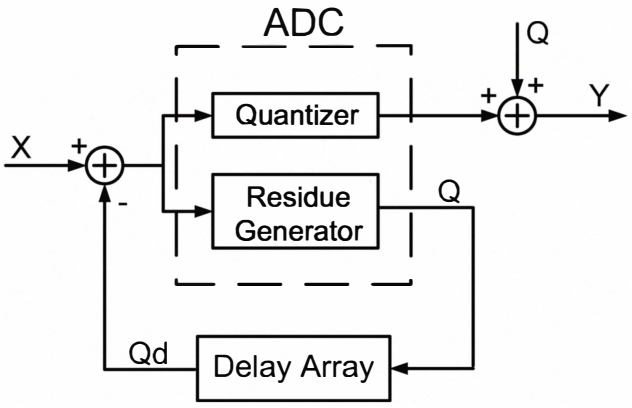

Fig. 2 Concept of constructing noise shaping in the Nyquist ADC structure

In Fig. 2, X is the input signal, Y is the digital output, Q is the quantization noise and Qd is the quantization noise after delay. Residue generator is to obtain analog quantization noise. Delay array is to get different form of delay. It can derive the Z-domain equation as below,

$$Y(z) = X(z) - Qd(z) + Q(z) \tag{3}$$

Qd(z) can be expressed as eq. (4),

$$Qd(z) = -[C_n^1(-Z^{-1})^1 + ... + C_n^i(-Z^{-1})^i + ... + C_n^n(-Z^{-1})^n]Q(z) \tag{4}$$

Substitute the eq. (4) into eq. (3), and the formula can be changed into eq. (5),

$$Y(z) = X(z) + [C_n^0 + C_n^1(-Z^{-1})^1 + ... + C_n^i(-Z^{-1})^i + ... + C_n^n(-Z^{-1})^n]Q(z) \tag{5}$$

Simplify the eq. (5), the result can be expressed as eq. (6)

$$Y(z) = X(z) + (1 - Z^{-1})^n \cdot Q \tag{6}$$

In the equations, n denotes the order of noise shaping. From the eq. (6), it demonstrates that the quantization noise is really suppressed in the signal band (assume that the signal band is base band). Basically, this equation verifies the possibility of using delay to construct the noise shaping in the theory. In order to further verify this concept, the system will be constructed in two kinds of Nyquist ADC architectures and also simulation results will be presented next.

III. DELAY-BASED NOISE SHAPING IMPLEMENTATION

A. Construct Noise Shaping in the Two-Step ADC

The most important factor is to acquire the analog quantization noise and then feedback this quantization noise to the input. With regard to two-step ADC, it is well known that it can obtain analog quantization noise between stages. So it is easily to construct noise shaping in two-step ADC arthitecture based on delay. This concept can be interpreted as Fig. 3.

In the Fig. 3, it contains traditional two-step ADC and modified two-step ADC with noise shaping. The DAC converts the digital code into analog signal, and subtracted this signal from the input of the ADC can obtain the analog quantization noise. Then feedback the quantization noise to the input of the second stage through H(z). X is the analog input, D_i (i=1,2) denotes the digital output., and Q_j (j=1,2) is the j-th stage quantization noise. It can derive the Z-domain equation as below,

$$D_1 = X + Q_1 \tag{7}$$

$$D_2 = -GZ^{-1} \cdot [Q_1 + Q_2 H(z)] + Q_2 \tag{8}$$

From eq. (7) and (8), it can derive the final digital output as eq. (9),

$$D = D_1 \cdot Z^{-1} + \frac{D_2}{G} = X \cdot Z^{-1} + [1 - H(z) \cdot Z^{-1}]\frac{Q_2}{G} \tag{9}$$

If H(z)=1, the eq. (9) can be changed into eq. (10),

$$D = D_1 \cdot Z^{-1} + \frac{D_2}{G} = X \cdot Z^{-1} + [1 - Z^{-1}]\frac{Q_2}{G} \tag{10}$$

In the eq. (10), it clearly reveals that the system has one order noise shaping on the quantization error Q_2. Namely, the two-step ADC has the function of one order noise shaping.

Similarly, when $H(z)=Z^{-1}-2$, the system can implement two order noise shaping. In this theory, it can realize any order of noise shaping just with some delay in ideal. In short, the two-step ADC architecture succeed in constructing noise shaping by this technique.

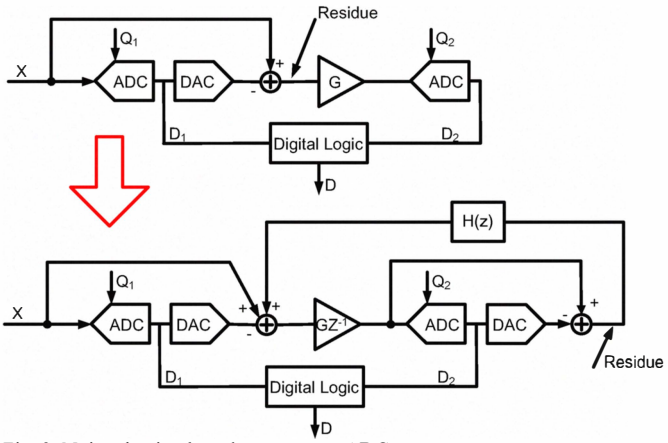

Fig. 3. Noise shaping based on two-step ADC

B. *Construct Noise Shaping In SAR ADC*

For SAR ADC, its residue will be stored in the DAC capacitor after several periods' conversions. It provides the possibility to construct the noise shaping in the SAR ADC.

The concept of constructing noise shaping in the SAR ADC structure is interpreted in the Fig. 4. Firstly, the system sample the signal, which is combined with the input signal and the quantization noise with various delay, to the capacitors controlled by the sequence $\Phi_{S\&H}$. Secondly, the system will experience several periods' conversion controlled by the sequence of Φ_{DAC}. Then, the residue stored in the capacitors will be sampled by the Source Follower which is controlled by the sequence of Φ_{SF}. Finally, the residue experiences Delay array and feedback to the sample and hold part.

For example, the system feedback the residue with one delay, then the output D can be described as eq. (11),

$$D = X - Q \cdot Z^{-1} + Q = X + (1 - Z^{-1})Q \qquad (11)$$

From eq. (11), it obviously proves that the system has one order of noise shaping. In the system, one can transform the Delay Array in order to achieve various order of noise shaping.

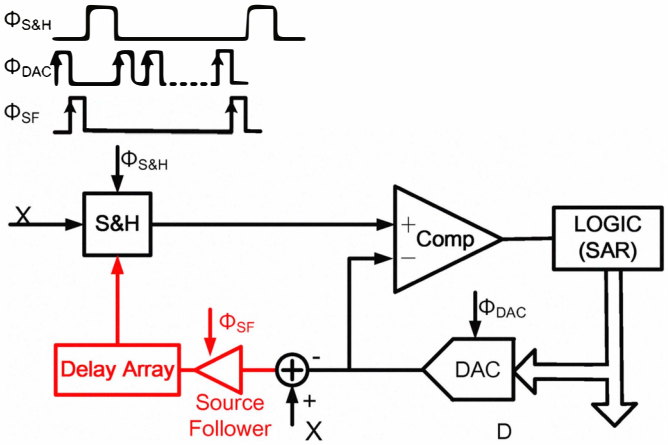

Fig. 4. SAR ADC with noise shaping

IV. Simulation Results

A. *Simulation Results Based on Two-Step ADC*

In the system based on two-step ADC, the ADC and DAC of both stages are 3-bits respectively. The OSR is 8. The order of noise shaping is one. And the bandwidth (BW) of the input signal is 1 MHz. Eventually, the ideal PSD of Two-Step ADC With Noise Shaping (TSWNS) is showed in Fig. 5. And the SNDR of the ideal TSWNS is 65.2dB.

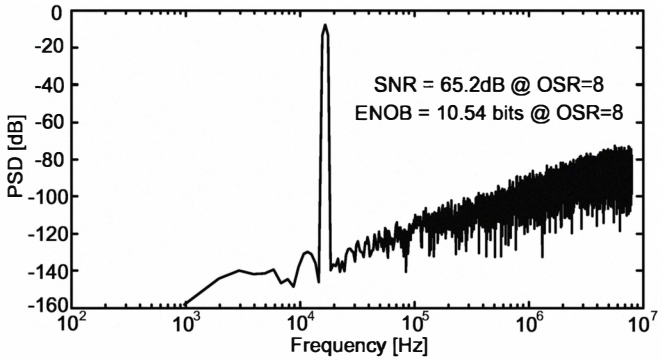

Fig. 5. Ideal PSD of TSWNS

To further verify the TSWNS system, we must consider the non-ideal factors in the system. Actually, the DAC mismatch is the worst factor of the TSWNS. So firstly, it needs to study the influence of DAC mismatch and analyze the tolerance of the system. In the simulation, the standard deviation of the DAC mismatch σ is set to 0.3%. The Monte-Carlo simulation result (the simulation number is 50) is depicted in Fig. 6.

From the Fig. 6, it can know that the mean of SNDR is 48.27-dB, and the stand deviation is 4.18-dB. From this simulation result, we can conclude that the DAC mismatch influences the system negatively. So it needs to calibrate the DAC error.

After several years' research on DEM, many kinds of solutions have been proposed. The hot research directions are DWA and tree-structured DEM The simple one is DWA proposed in [4], and also some DWA have been improved, such as Bi-DWA [5]. Several tree-structured DEMs have been proposed and improved recently. Such as paper [6], it is about the DACs with arbitrary numbers of levels. In the simulation, we use tree-structured DEM [6].

And the simulation result is showed in the Fig. 7. From this result, we know that the two-step ADC is only 5-bit without any handling. But the ADC with noise shaping achieves 10-bit. Actually, the power consumption is almost not increased due to only add one feedback route which using one capacitor to realize. However, the resolution is increased to 10-bit. Because the OSR is 8, which is 8 times higher than the Nyquist-rate but the ENOB has been improved by 32 times. As a result, the FOM of the whole system is improved by 4 times. That is the performance of the whole system can be improved by this technique.

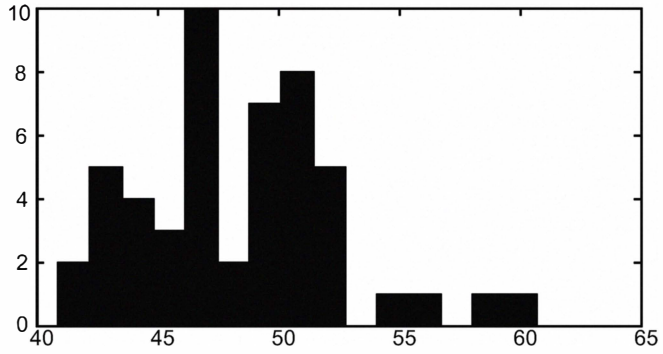

Fig. 6. Monte-Carlo simulation result

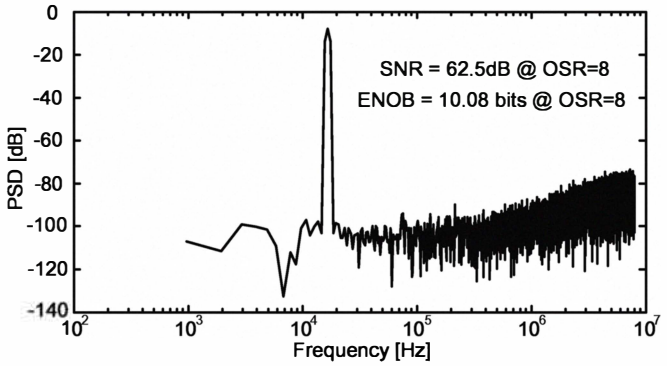

Fig. 7. Real PSD of TSWNS

Besides, another advantage is that it only needs j-bit DEM but realizes i-bit quantization noise shaping(i>j>=0). For example, if the first stage quantizer is 2-bit, and the second stage is 2-bit, so the result is 4-bit noise shaping but we just use 2-bit DEM to solve the problem of DAC nonlinearity. A special case is the first stage is 1-bit and the second stage is 1-bit, and there is no value to use DEM to solve the problem of DAC nonlinearity but implements 2-bit noise shaping. In short, it can relax the complexity of the calibration.

B. Simulation Results Based on SAR ADC

The SAR ADC is 6 bit. The Delay Array is just Z^{-1}, and the system is one order noise shaping. The OSR is 8 and the BW of the input signal is also 1 MHz. In this architecture, it also using DEM [6] to solve the DAC mismatch. The SAR ADC only has one comparator and the SAR ADC is only 6-bit, so the offset is in the tolerance of the system. After DAC calibration, the simulation result is showed as Fig. 8. The SNDR is 59.6-dB. Similarlly, the FOM of the whole system will be improved by the noise shaping. Besides, most part of the SAR ADC is digital, so it has the advantage to consume low power.

The noise shaping of these two examples is 1st order, so the improvement of the FOM by noise shaping is limited. It is better to construct high order noise shaping in these architectures, and the result will be further improved.

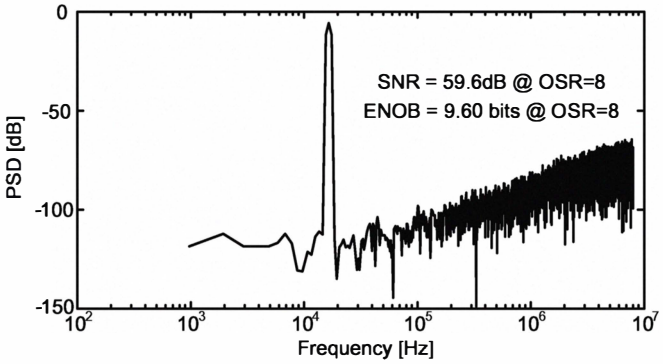

Fig. 8. Real PSD of SAR with noise shaping

V. CONCLUSION

From the discussion above, the proposed architecture can construct noise shaping function based on Nyquist-rate ADC architectures and delayed analog quantization error. Using 5-bit two-step ADC with 1st order noise shaping, it can achieve 62.5-dB SNDR and exploiting 6-bit SAR with 1st order noise shaping, it can achieve 59.6-dB SNDR. Thus the FOM of the whole system can be optimized. The proposed technique is effective to improve the ADCs' performance.

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