A Single-to-Differential LNA Topology with Robust Output Gain-Phase Balancing against Balun Imbalance

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***Abstract*—This paper presents a technique to enhance the output balancing precision of a low-noise amplifier (LNA) against balun imbalance. By utilizing two capacitive-cross-coupling common-gate amplifiers in cascode, wideband output balancing, high voltage gain and low noise figure (NF) can be concurrently achieved. A 2.4GHz LNA design example optimized in a 0.13µm CMOS process shows that the tolerable balun's gain and phase imbalances are up to 2dB and 10º, respectively. With just 3.6mW of power, the NF is 2.6dB at a voltage gain of 30dB.**

I. Introduction

Differential circuits are common in wireless applications as they can reduce even-order distortion and the susceptibility to common-mode noise. In a mixed-signal wireless transceiver, differential RF circuits can help to avoid unwanted common-mode noise couplings through the substrate and supply rails. A differential low-noise amplifier (LNA) is critical to maximize the receiver path sensitivity. The main concern is the need of a single-to-differential circuit to interface directly with the antenna or a band-select filter; both are normally single-ended. Passive baluns (also known as transformers), both off-the-shelf and integrated types, are the components of choice for their ultra-high linearity and reasonable insertion loss. Regrettably, in massive manufacturing (discrete baluns) and with process variation (integrated baluns), certain differential imbalance is unavoidable. This issue has not been relevantly addressed in the literature [1, 2], though LNAs with a balanced differential output can increase the robustness of the LNA against process variations, and reduce the even-order distortion of the mixers.

In this paper, a new differential LNA that can effectively eliminate the differential imbalance due to balun imperfection is proposed. The circuit topology is based on the capacitive-cross-coupling common-gate amplifier (CCC-CGA) [3] that was proposed to improve the noise figure (NF) and voltage gain through current-reuse g_m-enhancement. Differently here the idea is further extended; a cascode use of two CCC-CGAs ensures robust output differential balancing against input imbalance. Further, with a *LC* tank as the load, the LNA can reject the out-of-band interferers to relax the linearity of the mixers, while rendering it more suitable for advanced low-voltage technologies.

II. Circuit Description

The schematic of the proposed LNA is presented in Fig. 1. A balun with a middle-grounded secondary is selected to directly provide the bias currents to the LNA. The balun features the simplest 1:1 inductance ratio to alleviate the implementation of the integrated balun. Ideally, the input balun should divide

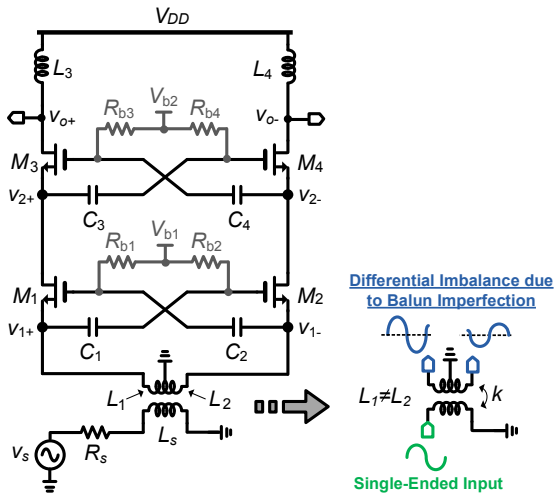

Fig. 1. Proposed LNA.

the single-ended input signal into two equal-amplitude out-of-phase differential signals. In practice, baluns suffer from imperfect single-to-differential conversion. On one hand, if the balun is an external off-the-shelf component, certain ranges of gain and phase imbalances are unavoidable (as defined in the datasheet). On the other hand, if the balun is integrated and is laid out asymmetrically with multiple metal layers in stack [4] the differential output can also show gain and phase imbalances due to different parasitic capacitors to the substrate, and different metal conductivities.

The proposed LNA addresses this issue by adopting two CCC-CGAs in cascode. Transistors M_1 and M_2 (M_3 and M_4) are cross-coupled by capacitors C_1 and C_2 (C_3 and C_4). In this way, the overall transconductance (g_m) is approximately doubled with no extra power. Each CCC-CGA can be treated as a voltage-difference amplifier from another viewpoint, offering the desired differential balancing inherently. Their double use in this work significantly increases the precision of the balancing, i.e., from ($v_{1+} - v_{1-}$) to ($v_{2+} - v_{2-}$) and from ($v_{2+} - v_{2-}$) to ($v_{O+} - v_{O-}$). Under this double correcting scheme, the final differential imbalance should be just the residual of the residual of the original error. The key features of this LNA are theoretically analyzed next.

III. Circuit Analysis

The key characteristics of this LNA including input impedance, voltage gain and noise figure are analyzed first. Then, the mathematical treatment of the imbalance correction capability of the LNA is addressed.

Input Impedance – It is calculated based on the incremental model of the LNA as shown in Fig. 2. Assuming that i_1=-i_2, $v_{gs1} = -v_{gs2}$ and $c_{gs1} = c_{gs2}$, the input impedance is given by,

$$Z_{in} = \frac{v_x}{i_x} = sL_S - 2sM\frac{2sM(2sC_{gs1} + g_{m1})}{1 + 2sL_1(2sC_{gs1} + g_{m1})} \quad (1)$$

where M is the mutual inductance: $M = k\sqrt{L_S L_1} = k\sqrt{L_S L_2}$. Assuming that $L_s = 2L_1$, $g_{m1} >> |2sC_{gs1}|$ and $g_{m1} = 1/R_s$, Z_{in} can be simplified as,

$$Z_{in} = \frac{2sL_1\left(R_S + 2\left(1-2k^2\right)sL_1\right)}{R_S + 2sL_1}. \quad (2)$$

Eq. (2) can be used to determine the input resonant frequency. With $Z_{in} = R_S$, the resonant frequency is obtained,

$$f_0 \approx \frac{1}{2\sqrt{2k^2 - 1}}\frac{R_S}{L_1}. \quad (3)$$

Eq. (3) reveals that f_0 is independent of C_{gs} since v_{gs} is determined by the balun and is directly applied to the gate-source terminals of M_1 and M_2. The input impedance is relatively wideband because the Q is low, the same as CCC-CGLNA. It also implies that the impedance matching is insensitive to the input parasitic capacitance.

Voltage Gain – This LNA can be partitioned into 3 stages. Each features an internal voltage gain. If the channel length modulation is neglected, the final gain of the 3 stages can be determined independently. The gain of the 1st stage corresponds to the gain of the balun. Considering Fig. 2 again and assuming that $g_{m1} >> |2\text{ s }c_{gs1}|$, and L_S=2 L_1, the gain of the 1st stage can be obtained,

$$\frac{v_{gs1}}{v_x} = \frac{\sqrt{2}k}{1 + 2g_{m1}(1-2k^2)L_1 s}. \quad (4)$$

The balun voltage gain has a pole at around $-1/2g_{m1}L_1$ that must be apart from the resonant frequency desired for the LNA. Neglecting C_{gs} and let $v_{gs3} = -v_{gs4} = v_{s4} - v_{s3}$, the gain of the 2nd stage (v_{gs3}/v_{gs1}) is simply given by the ratio between the transistors transconductances g_{m1}/g_{m3}. Finally, considering that $v_o = v_o^+ - v_o^-$, the gain of the 3rd stage is given by,

$$\frac{v_o}{v_{gs3}} = g_{m3}\left(r_{o3} \,//\left(sL_3 + r_3\right)// \frac{1}{sC_L}\right). \quad (5)$$

r_3 is the inductor series resistance and C_L is the load capacitance. The resonance of the load of the LNA determines the LNA tuning frequency. This is determined by the load capacitance and inductance values. Neglecting r_3, the LNA voltage gain is the product of the 3-stage voltage gains,

$$\frac{v_o}{v_x} \approx g_{m1}\frac{sL_3 r_{o3}}{r_{o3} + sL_3 + s^2 C_L L_3 r_{o3}}\frac{\sqrt{2}k}{1 + 2g_{m1}L_1(1-2k^2)s} \quad (6)$$

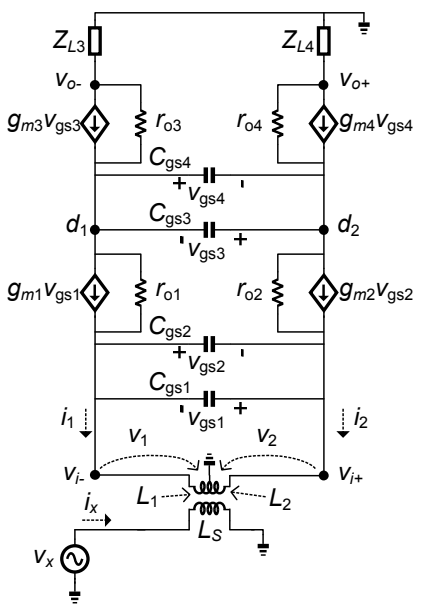

Fig. 2. Incremental model of the proposed LNA.

Noise Factor – The noise generated by M_1 and M_2 dominate the noise factor, F, of the LNA. Considering a perfect input impedance matching, i.e. $g_{m1} = g_{m2} = 1/R_s$, the LNA noise factor is,

$$F = 1 + \left|1 - \varphi - \frac{Z_1 g_m}{1 + Z_1 g_m}\right|^2 \gamma, \quad (7)$$

where Z_1 is given by,

$$Z_1 = \frac{v_1}{i_1} = Ms - \frac{M^2 s^2}{R_S + L_S s}(1 - \varphi). \quad (8)$$

and φ is given by,

$$\varphi = \frac{sL_1\left(R_S + 2\left(1-2k^2\right)sL_1\right)}{R_S^2 + 3L_1 R_S s + 2\left(1-2k^2\right)L_1^2 s^2}. \quad (9)$$

One important feature of the CCC technique is that the noise due to transistors M_3 and M_4 is approximately canceled as shown in [1].

Imbalance Calculation – To determine the LNA phase and gain imbalances, the first step is to define the input signal. The input signal corresponds to the difference between the two balun output signals: v_{i+} and v_{i-}. Using v_{i+} as the reference, v_{i-} will correspond to the negation of v_{i+} multiplied by a complex number with gain and phase errors. The differential signal at the balun output is then,

$$v_i = v_{i+} - v_{i-} = \left(1 - (1-\alpha)e^{j\beta}\right)v_{i+}. \quad (10)$$

where α is the ratio between the amplitude of both signals and β is the phase error. As a note, the gain error is determined by $20\log(\alpha)$. Now we have to determine the signals at the drain of the two input stages,

TABLE I.
COMPONENT SIZES.

Parameter	Value	Parameter	Value
$(W/L)_{M1,M2}$	38.4/0.13	$L_S(R_s)$	4.0 nH (6 Ω)
$(W/L)_{M3,M4}$	32.0/0.13	$L_{\{1,2\}}$ (R_s)	2.0 nH (3 Ω)
$R_{BIAS\{1,2,3,4\}}$	10 kΩ	$L_{\{3,4\}}$ (R_s)	8.0 nH (12 Ω)
$C_{BIAS\{1,2,3,4\}}$	0.5 pF	k	0.9

$$\begin{cases} v_{d1} = g_{m1} Z_{load1} v_{in} \\ v_{d2} = g_{m2} Z_{load2} v_{in} \end{cases} \tag{11}$$

where g_{m2} is equal to $x\,g_{m1}$, and x accounts the mismatch between M_1 and M_2. Z_{load1} and Z_{load2} are symmetrical, thus we will just determine Z_{load1}. Z_{load1} is a parallel of the following three impedances: the output impedance of M_1: r_{o1}, the impedance made by M_3: Z_{load13}, and the impedance made by M_4: Z_{load14}. The expression of Z_{load1} is given by,

$$Z_{load1} = \left(r_{o1} \,//\, Z_{load13} \,//\, Z_{load14}\right), \tag{12}$$

where Z_{load13} and Z_{load14} are respectively,

$$\begin{cases} Z_{load13} \approx \left(\dfrac{1}{g_{m3}} \,//\, r_{o3}\right) + Z_{load3} \\ Z_{load14} \approx \dfrac{1}{s\left(C_{gs3} + C_{gs4}\right)} + \left(\dfrac{1}{g_{m4}} \,//\, r_{o4}\right) + Z_{load4} \end{cases} \tag{13}$$

Both, Z_{load13} and Z_{load14} are obtained under the assumption that the impedance seen to the source of M_3 (M_4) is much smaller than that seen to the drain of M_1 (M_2) and Z_{load3} and Z_{load4} are given by,

$$Z_{load3} = Z_{load4} = Z_{load} = \left(\left(sL_3 + r_{L3}\right) // \frac{1}{sC_3}\right), \tag{14}$$

where r_{L3} is the series resistance of L_3. The differential voltage v_d is,

$$v_d = v_{d2} - v_{d1} = \left(Z_{load2}\,x - Z_{load1}\right) g_{m1} v_i \tag{15}$$

We conclude from (15) that the imbalance just depends on the mismatches inside the circuit and is independent on the mismatches due to the balun. Finally, $v_o = v_{out+} - v_{out-}$ is obtained,

$$v_o = \left(g_{m3} - g_{m4}\right) Z_{load} v_d = \left(1 - y\right) g_{m3} Z_{load} v_d \tag{16}$$

where $g_{m4} = y\,g_{m3}$. y accounts for the mismatch existing between M_3 and M_4. From (16) we conclude that the phase and gain imbalance existing at the LNA output is only due to the mismatch between M_3 and M_4. It implies that if M_3 and M_4 are purely matched and there is no channel length modulation, independently on the remaining circuit, the output imbalance can be nullified.

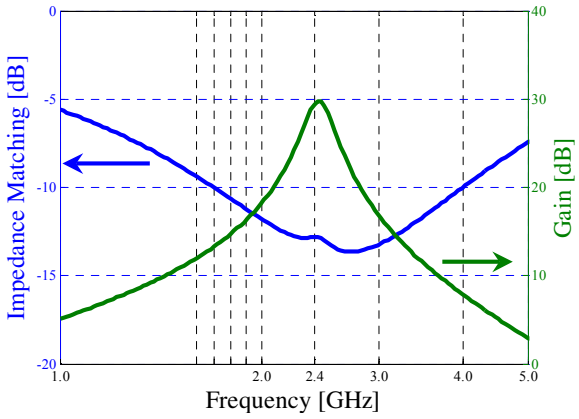

Fig. 3. Voltage gain and input impedance matching (S11).

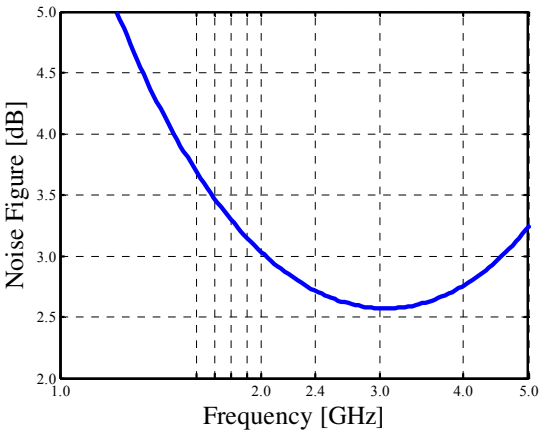

Fig. 4. Simulated noise figure.

IV. DESIGN VERIFICATION

A 1.2-V 2.4-GHz LNA design example with a 0.5-pF capacitive load is designed in 0.13-µm CMOS. The associated component sizes are given in Table. I. The balun coupling coefficient (k) is assumed to be 0.9, and the Q of all inductors is assumed to be 10 in practice, which defines their series resistance Rs at 2.4 GHz. The input impedance is matched with R_S = 50 Ω with $g_{m1} = g_{m2} = 1/R_S$. With 3 mW of power consumption, the achieved voltage gain, noise figure and input impedance matching (S_{11}) at 2.4 GHz are, respectively, 30 dB, 2.6 dB and –12.5 dB, as shown in Fig. 3. and Fig. 4, which are competitive values when compared to the state-of-the-art.

The output gain-phase balancing is accessed by varying the ratio between L_1 and L_2 as listed in Table II. For a phase error up to 10º and a gain error up to 2 dB (referred to the balun output) the LNA can adequately balance their outputs if the transistors are differentially matched. A simulation example is shown in Fig. 5 and Fig. 6 for the input-output gain and phase balancings, respectively. The LNA can tolerate up to 20% of transistor mismatch between the differential branches given such a gain-phase mismatch, which are easily manageable in modern technologies. Consequently, this circuit is highly

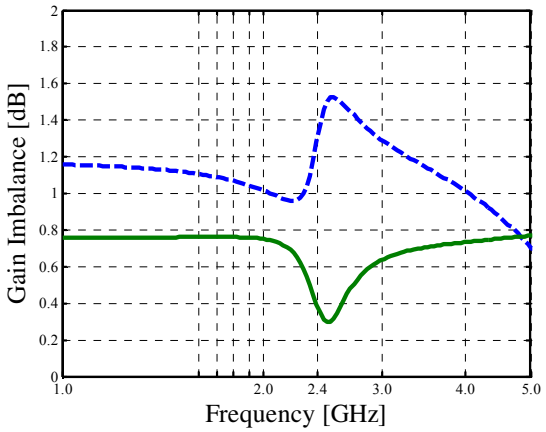

Fig. 5. LNA gain balancing capability example. Balun output inductance ratio of 1.3 and transistor differential mismatch (ratio between transistor widths) of 1.1.
- - - - - Gain imbalance induced by the balun.
——— Gain imbalance after gain-phase balancing.

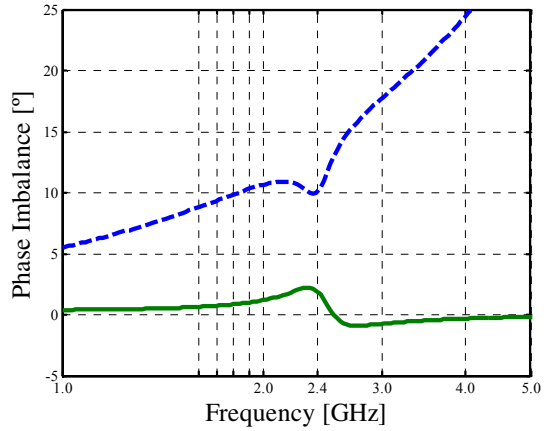

Fig. 6. LNA phase balancing capability example. Balun output inductance ratio of 1.3 and transistor differential mismatch (ratio between transistor widths) of 1.1.
- - - - - Phase imbalance induced by the balun.
——— Phase imbalance after gain-phase balancing.

robust to the input differential imbalance induced by the balun.

The die size of the LNA using an integrated balun is 510 µm × 750 µm including the bond pads (Fig. 7). The chip is currently under fabrication.

V. Conclusions

This paper introduced a new differential LNA with robust output gain-phase balancing. Two capacitive-cross-coupling common-gate amplifiers are in cascode to realize double gain-phase equalization. This topology not only realizes a high voltage gain with low noise through current-reuse g_m-enhancement, but also corrects robustly a wide range of input gain-phase imbalance under component mismatches. The feasibility has been demonstrated through the design of a 2.4-GHz LNA, which can tolerate up to 2 dB and 10º gain and phase imbalances, respectively.

Table II.
LNA Balancing Capability at 2.4 GHz Against Balun Imbalance and Transistor Mismatch.

Balun Imbalance	Transistor Mismatch		Phase before & after balancing		Gain before & after balancing	
L_1/L_2	W_{M1}/W_{M2}	W_{M3}/W_{M4}	$\Delta\Phi_{in}$ [º]	$\Delta\Phi_{out}$ [º]	$\Delta Gain_{in}$ [dB]	$\Delta Gain_{out}$ [dB]
1.1	1	1	2.57	0.03	0.48	0.01
1.3	1	1	7.73	0.09	1.32	0.04
1.3	1.1	1.1	8.92	1.56	0.98	0.38
1.3	1.2	1.2	9.63	2.93	0.69	0.65
1.4	1	1	10.32	0.12	1.69	0.05
1.4	1.2	1.2	12.42	2.98	1.03	0.66
1.4	1.3	1.3	12.78	4.25	0.78	0.86

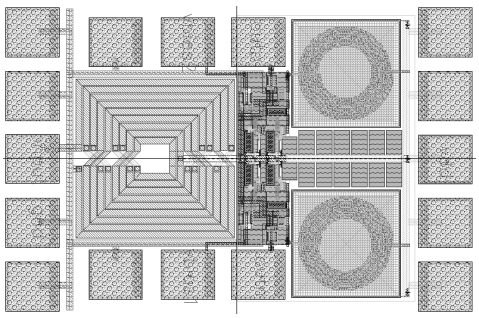

Fig. 7. Layout of the LNA.

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