China 1991 International Conference on Circuits and Systems, June 1991, Shenzhen, China

SENSITIVITY ASPECTS RELATED TO THE SWITCH TIMING OF MULTIRATE SWITCHED-CAPACITOR CIRCUITS

Rui P. Martins José E. Franca

Instituto Superior Técnico - Department of Electrical and Computer Engineering
Av. Rovisco Pais, 1, 1096 Lisboa Codex, Portugal

Abstract : This paper evaluates the operation of multirate switched-capacitor circuits under non-ideal characteristics of the switching waveform generators. Analytical expressions are derived showing the influence of switch-timing errors in the frequency response of both finite impulse response and infinite impulse response circuits. In order to reduce such errors, efficient digital switching waveform generators are discussed. The results obtained by computer simulation and by experimental characterization of integrated circuit prototypes demonstrate the validity of the theoretical analysis.

1. INTRODUCTION

Switched-Capacitor (SC) decimators and interpolators are multirate sampled-data circuits which provide an appropriate filtering function together with the alteration of the sampling frequency of the signal. In SC decimators the input sampling frequency is higher than the output sampling frequency, whereas in the case of SC interpolators the output sampling frequency is higher than the input sampling frequency. Various types of SC decimators and interpolators have been proposed to implement discrete-time transfer functions with either finite impulse response (FIR) [1,2] or infinite impulse response (IIR) [3,4]. Until now we have considered the evaluation of the performance behavior of such circuits with respect to the non-ideal characteristics of the amplifiers, switches and capacitors [5,6], but little attention has been given to the performance evaluation under non-ideal characteristics of the switching waveform generators.

This paper is concerned with the study of the non-ideal characteristics associated with the multiple switching waveforms employed in multirate SC circuits, and their effect on the behavior of the overall frequency response. Errors on the switching operation of multirate SC circuits include the timing errors between two sampling points (differential timing errors) as well as the time jitter associated with each one of those sampling instants. Differential timing errors are particularly accute in SC decimator and interpolator circuits where they are mainly responsible for the modification of the multiple zero pattern which determines the levels of rejection of the unwanted aliasing and imaging frequency components, respectively. On the contrary, time jitter errors are common to all sampled-data circuits where they can be shown to give rise to low frequency noise increasing the total harmonic distortion [7]. In order to significantly reduce the differential timing errors associated with the operation of multirate SC circuits we shall also discuss efficient digital switching waveform generators paying particular attention to their attractiveness for integrated circuit implementation. This, combined with the analog circuitry required for the implementation of the signal processing circuits renders the complete SC decimators and SC interpolators suitable for implementation using state-of-the-art mixed analog-digital technologies. The results derived from theoretical analysis are supported by computer simulated results of an FIR SC decimator and by the experimental evaluation of an integrated IIR SC decimator realized using a 1.8 μm double-poly CMOS technology.

2. SWITCH TIMING EFFECTS

The general architecture of a multi-phase switching waveform generator, presented in Fig.1, comprises a counter which divides the crystal clock frequency, and a decoder that allows the implementation of different types of switching waveforms. Typical arrangements of the switching waveforms include two different time frames, namely one for controlling the operations of input (output) sampling of the decimator (interpolator), and the other for controlling the operations of charge transfer through the virtual ground of the amplifiers [1-4]. The sampling time frame of an SC decimator comprises M (L in the case of an SC interpolator) switching waveforms with narrow time slots, whereas the time frame for charge transfer possesses only two much wider time slots which have direct influence on the settling of the amplifier. Switch timing errors may occur if the original time frames have deviations from their nominal arrangement, as illustrated in Fig.2. Fig.2-a shows the example of a sampling time-frame where typical switch-timing errors are associated with *time-slot i*. Such timing errors occur either due to an advance ($+\Delta i$) or due to a delay ($-\Delta i$) of the actual *time-slot i* relative to the nominal *time-slot i*. Fig.2-b shows switch-timing errors of the same type but associated with *time-slot B* ($\pm\Delta n$) of the charge transfer time-frame. The errors illustrated in Fig.2 result from different propagation delays which can be due either to different electronic paths, as is shown in Fig.3-a, or in equivalent electronic paths due to digital gates of the same type with different delay characteristics (Fig.3-b). A combination of both causes can also contribute to produce differential timing errors associated with the time frames.

3. VARIABILITY OF THE FREQUENCY RESPONSE RELATED TO THE SWITCH TIMING

Multirate FIR SC Circuits : The evaluation of an FIR discrete-time transfer function on the unit circle, $z=e^{(-j\Omega)}$, gives

$$H(j\Omega) = \sum_{i=0}^{N-1} h_i . e^{-j i \Omega} \qquad (1)$$

where $\Omega=\omega/MF_S$, for an SC decimator, and $\Omega=\omega/LF_S$ for an SC interpolator. For positive symmetry FIR discrete-time transfer functions, i.e. $h_i=h_{N-1-i}$, we can write (1) as

$$H(j\Omega) = H(\Omega) . e^{-j\frac{N-1}{2}\Omega} \qquad (2)$$

where $H(\Omega)$ is the amplitude response and the corresponding attenuation, in decibels, is

$$A(\Omega) = -20 \log H(\Omega) \ \text{dB} \qquad (3)$$

If we consider switch timing errors, they only influence the terms $e^{(-j\Omega i)}$ in such a way that

$$h'_i(j\Omega) = h_i . e^{-j(i \pm \Delta i)\Omega} \qquad (4)$$

where $\pm\Delta i$ is associated to a timing error in the *time-slot i* which produces the delay z^{-i}. Usually, such error is small, i.e. $\pm\Delta i \ll 1$, and thus we can write (4) as

$$h'_i(j\Omega) = h_i . (1 \pm j\Delta i\Omega) e^{-j i \Omega} \qquad (5)$$

and by entering (5) into (1), and by using (2), we obtain

$$H'(j\Omega) = H(\Omega) . e^{-j\frac{N-1}{2}\Omega} \pm j\Delta i\Omega . h_i . e^{-j i \Omega} \qquad (6)$$

The errors in the passband of FIR SC decimator and interpolator circuits, where $H(\Omega)\approx 1$, are small, since $\pm\Delta i \ll 1$. On the contrary, the errors which arise in the multinotch stopband, even if they are small, become much more important since $H(\Omega)\approx 0$.

Multirate IIR SC Circuits : The analysis of the influence of switch timing errors on IIR decimators and interpolators can be simplified if we consider separately the two types of errors described above. For example, a switch timing error on *time-slot i* of the sampling time-frame occuring on an N.th-order multirate SC circuit leads to the following modified discrete-time transfer function [8,4]

$$H'(z) = \frac{\sum_{i=0}^{M.(P+2S)} a'_i \cdot z^{-(i \pm \Delta i)}}{\prod_{i=1}^{P} [\beta_i - z^{-M}] \cdot \prod_{i=1}^{S} [1 + \frac{\delta_i}{\gamma_i} z^{-M} + \frac{\varepsilon_i}{\gamma_i} z^{-2M}]} \quad (7)$$

where N=P+2S, and P and S are, respectively, the number of first and second order sections. The above expression indicates that such variations on the multi-phase arrangement do not affect the denominator polynomial function whereas the numerator polynomial function is affected in the same way as in an FIR discrete-time transfer function. This implies the modification of the existent notches in the stopband and of the multiple pole-zero pattern cancelation [3,4,8] with the inherent reduction of the level of rejection of the aliasing (imaging) frequency components. Since the denominator polynomial function is not affected, any change in the baseband frequency response is only due to numerator variations.

A switch timing error occuring on the charge transfer time-frame (for example, time-slot B in Fig.2-b implies that the discrete-time transfer function becomes

$$H'(z) = H(z) \cdot z^{\pm \Delta n.M.[1-(P+S)]} \quad (8)$$

where H(z) is the nominal transfer function. Then, the overall amplitude response is only affected by a phase error which does not modify the baseband response nor the multiple pole-zero pattern cancelation.

4. SWITCHING WAVEFORM GENERATORS

Based on the general architecture of Fig.1, two different types of multi-phase switching waveform generators can be developed. Fig.4 shows a generator that can implement decimation factors of $M=2^i$ and is composed by a ripple counter with outputs connected to a decoding logic block appropriate for the determination of the different time-slots of the multi-phase arrangement. This is one of the basic and simplest circuit solutions for a great number of applications, but does not allow the realization of arbitrary integer decimation factors M. To overcome this difficulty an alternative type of generator is presented in Fig.5, where the ripple counter is now replaced by a ring counter and where the decoding logic can also be significantly simplified. The synchronizing logic is used only to obtain a complementary and synchronous multi-phase arrangement which is extremely useful in high frequency applications [10].

5. EXPERIMENTAL RESULTS

SC FIR Lowpass Decimator : The FIR SC decimator circuit to be evaluated is illustrated in Fig.6-a, together with the associated switch-timing shown in Fig.6-b. Such circuit implements a lowpass amplitude response with length N=7 and reduces the sampling rate from $4F_S$=192kHz to F_S=48kHz[6]. For a relative timing error of $\pm\Delta 3$ occuring in *time-slot 3* the actual frequency response in (6) becomes

$$H'(j\Omega) = e^{-j3\Omega} \cdot [H(\Omega) \pm j\Delta 3 \cdot h_3 \cdot \Omega]$$

At the nominal notch frequencies, $H(\Omega)=0$, the attenuation is given by

$$A(\Omega)|_{Notches} = -20 \log(\Delta 3 \cdot h_3 \cdot \Omega)$$

which indicates an error variation which increases with frequency. Therefore, the attenuation around the notches at higher frequencies becomes much more critical. This effect can be observed in the computer simulated results of Fig.7, which were obtained considering an advance of 65.1ns of slot 3, i.e. 1/80 of the unit delay period 1/192kHz.

SC IIR Lowpass Decimator : The IIR SC decimator circuit shown in Fig.8 has been realized in integrated circuit form using a 1.8µm double-poly CMOS technology. It implements a bilinear 2nd. order lowpass amplitude response together with a reduction of the sampling frequency from $3F_S$=16.59MHz to F_S=5.53MHz [9]. The baseband response of the decimator is presented in Fig.9, has been evaluated with the nominal time frame (Fig.9-a) and two different switch-timing errors (Fig.9-b and 9-c). The results show that a variation on *time-slot 2* only introduces a small gain error, whereas a variation on *time-slot 4* does not modify the baseband response. With the same time frames as in Fig.9, we also present in Fig.10 the frequency response aliased into the baseband when the source generator produces input signals from 5.55MHz to 5.75MHz and the output signals are synchronously detected from 20kHz to 220kHz. The results confirm that a variation on *time-slot 2* only affects the response in this band with a small gain error of approximately 2dB, whereas a variation on *time-slot 4* reduces the level of rejection of the aliasing component by a value of approximately 13dB, as expected from our theoretical analysis.

6. CONCLUSIONS

This paper presented the performance evaluation of multirate switched-capacitor circuits under non-ideal characteristics of the switching waveform generators, and it was shown how the resulting timing errors could produce modifications of the frequency response of both FIR and IIR SC decimator and interpolator circuits. To reduce differential timing errors, efficient digital switching waveform generators were discussed. Results obtained by computer simulation and by characterization of an experimental 1.8 µm CMOS integrated circuit were shown to be in agreement with the theoretical analysis.

References

[1] **J.E.FRANCA,** "Non-Recursive Polyphase Switched-Capacitor Decimators and Interpolators", *IEEE Transactions on Circuits and Systems* ,Vol. CAS-32,No. 9, pp.877-887, Sept.1985.

[2] **J.E.FRANCA, S.SANTOS,** "FIR Switched-Capacitor Decimators with Active Delayed Block Polyphase Structures", *IEEE Transactions on Circuits and Systems* ,Vol. CAS-35,No. 8, pp.1033-1037, August 1988.

[3] **J.E.FRANCA, R.P.MARTINS,** "IIR Switched-Capacitor Decimator Building Blocks with Optimum Implementation", *IEEE Transactions on Circuits and Systems* ,Vol. CAS-37,No. 1, pp.81-90, January 1990.

[4] **R.P.MARTINS, J.E.FRANCA,** "Infinite Impulse Response Switched-Capacitor Interpolators with Optimum Implementation", *Proceedings International Symposium on Circuits and Systems 1990*, New Orleans, U.S.A., pp.2193-2197, May 1990.

[5] **V.F.DIAS, J.E.FRANCA,** "Optimum Design of FIR Switched-Capacitor Decimators using Low-Gain Amplifiers", *Electronics Letters*, vol.24, pp.195-197, 18th. February 1988.

[6] **J.E.FRANCA,** "Switched-Capacitor Systems for Narrow Bandpass Filtering", *Ph.D.Dissertation*, University of London, May 1985.

[7] **J.C.VITAL, G.C.TEMES,** "Clock Generation system with reduced jitter noise in the baseband", to appear in the *International Symposium on Circuits and Systems 1991 - Proceedings*, Singapore, June 1991.

[8] **R.P.MARTINS, J.E.FRANCA,** "A Novel N-th Order IIR Switched-Capacitor Decimator Building Blocks with Optimum Implementation", *Proceedings International Symposium on Circuits and Systems 1989*, Portland, U.S.A., pp.1471-1474, May 1989.

[9] **R.P.MARTINS, J.E.FRANCA, F.MALOBERTI,** "A 1.8µm CMOS Switched-Capacitor IIR Decimator for high frequency applications", submitted to presentation at next *ESSCIRC'91*, Milan, Italy, September 1991.

[10] **R.GREGORIAN, G.TEMES,** *"Analog MOS Integrated Circuits for Signal Processing"*, John Wiley & Sons, Inc., 1986.

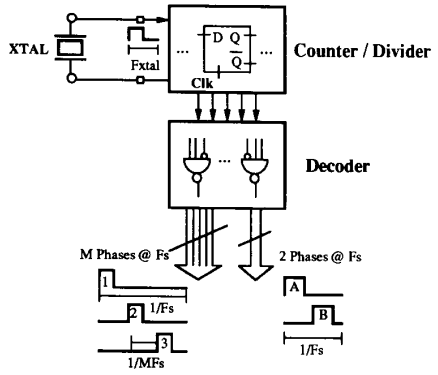

Fig.1 : Block diagram of a multi-phase switching waveform generator

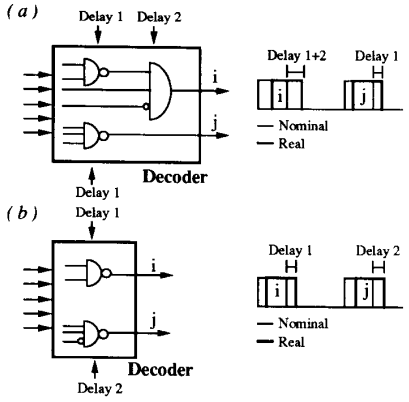

Fig.3 : Switch timing errors due to different propagation delays.
(a) With different paths.
(b) With similar gates (with different characteristics).

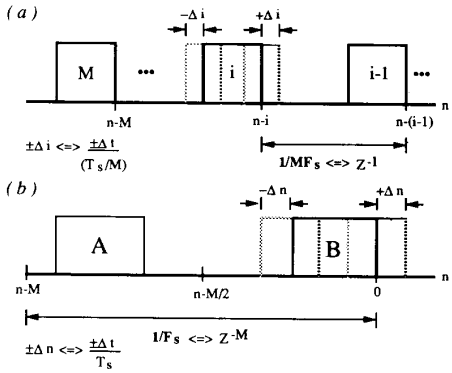

Fig.2 : Timing errors.
(a) Sampling time-frame.
(b) Charge-transfer time-frame.

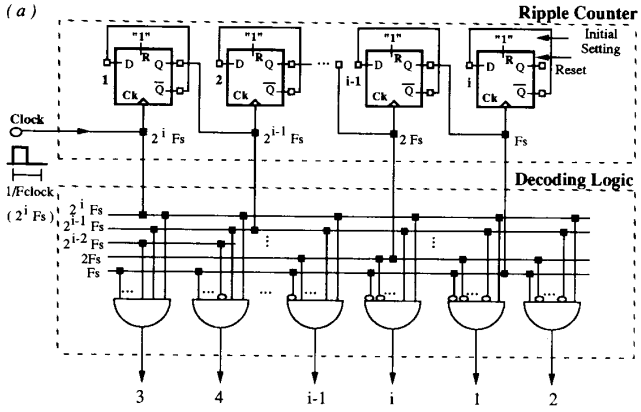

Fig.4 : Example of a multi-phase switching waveform generator for a decimation factor M = 2 i .
(a) Circuit and (b) switch timing.

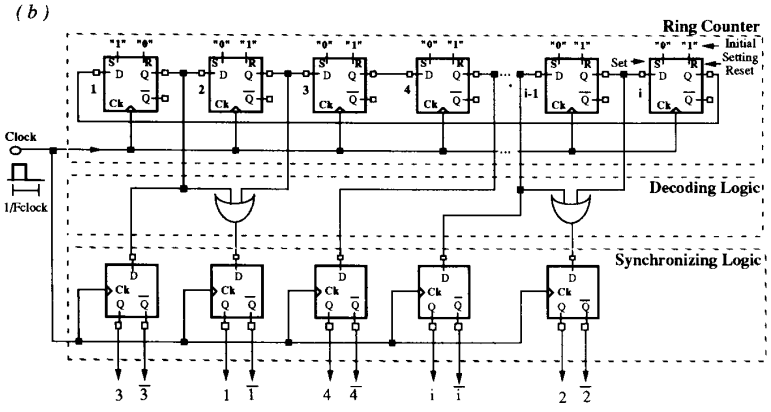

Fig.5 : Example of a multi-phase switching waveform generator for an arbitrary decimation factor M.
(a) Switch timing and (b) circuit.

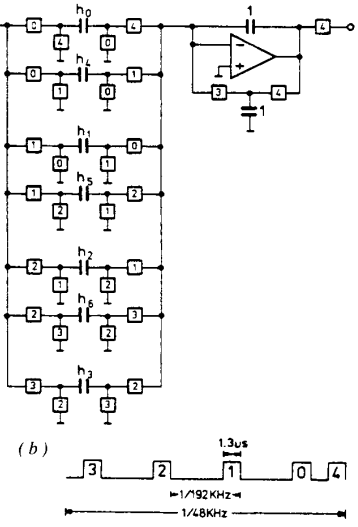

Fig.6 : FIR SC decimator M=4.
(a) Circuit and (b) Time frame.

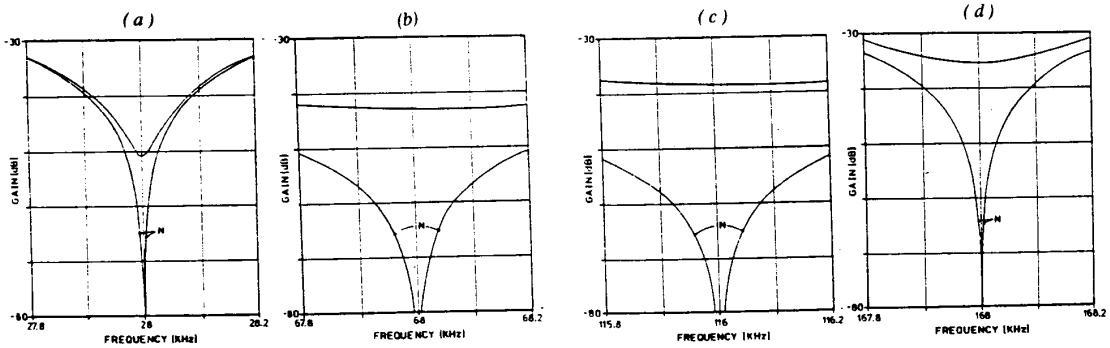

Fig.7 : Computer simulated amplitude responses of the FIR SC decimator M=4. Response around notch frequencies at (a) 28kHz, (b) 68 kHz, (c) 116kHz, (d) 168kHz, for 65.1ns advance of time slot 3.

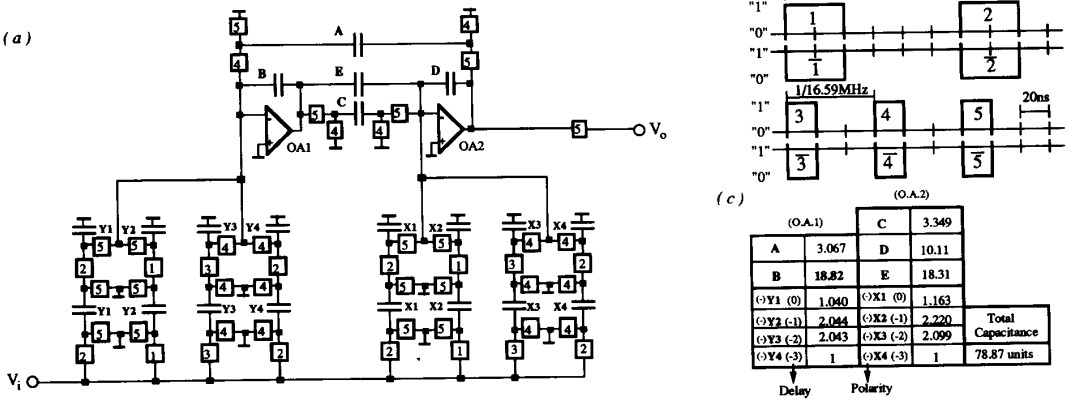

Fig.8 : IIR SC decimator with M=3. (a) Circuit. (b) Time frame. (c) Capacitor values.

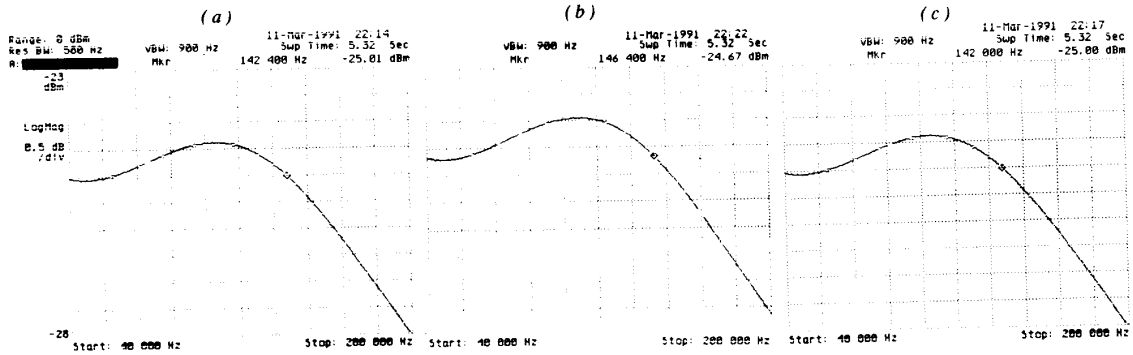

Fig.9 : Experimental evaluation of the IIR SC decimator M=3. Baseband response with (a) nominal time frame (b) for 20ns delay of time slot 2 and (c) for 20ns advance of time slot 4.

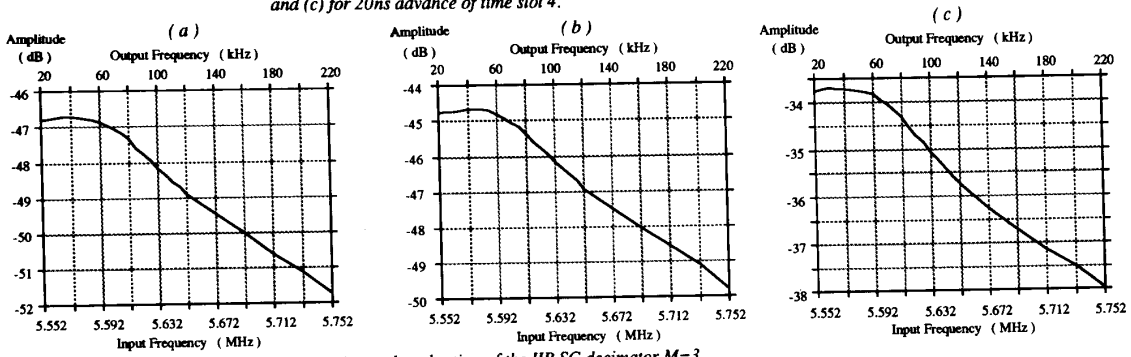

Fig.10 : Experimental evaluation of the IIR SC decimator M=3. Aliased response in the baseband of the 1st. aliasing component (5.53 MHz) with (a) nominal time frame (b) for 20ns delay of time slot 2 and (c) for 20ns advance of time slot 4.