A Linearity-Improved Ultra-Wideband Balun-LNA for Cognitive Radio

Weng-Fai Cheng, Ka-Fai Un, Pui-In Mak, and R. P. Martins [1]

Analog and Mixed-Signal VLSI Laboratory, University of Macau, Macao, China
1 – On leave from IST/TU of Lisbon, Portugal

Abstract

An ultra-wideband low noise amplifier for cognitive radio applications covering 50 MHz to 10 GHz is designed in a 65-nm CMOS technology. A three-stage dc-coupled common source amplifier with *RC* degeneration at the last stage optimizes the gain, linearity and output gain-phase balancing. Throughout the covered band, the simulated voltage gain is >23.3 dB whereas the noise figure is <3.4 dB. The *RC* degeneration technique improves the IIP_2 to 29.3 dBm and IIP_3 to -2.7 dBm. The power consumption is 21.4 mW at 1.2 V.

I. Introduction

Rapid downscaling of CMOS has led to more compact and faster RF circuits. The emerging cognitive-radio (CR) receivers demand a high-performance ultra-wideband (UWB) balun low-noise amplifier (LNA) to support the many possible communication channels from 50 MHz up to 10 GHz in one block, avoiding the need of multiple off-chip baluns and maximizing the hardware reuse in expensive nanometer-length CMOS technologies [1]. The focused UWB LNA in this work is based on the resistive-feedback technique to achieve inductive peaking, widening the passband bandwidth without needing inductor. The LNA is assumed to be applied into a direct-conversion receiver as outlined in Fig. 1.

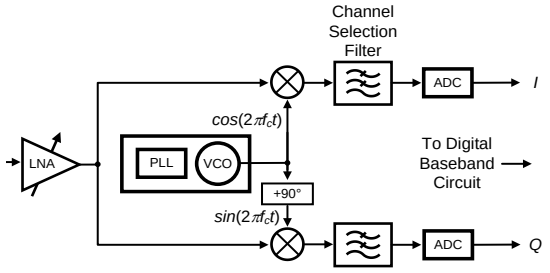


Fig. 1. The use of the LNA in a direct-conversion receiver.

The two key challenges associated with CR receivers are 1) the broadband characteristic, i.e., relatively flat gain, low noise figure (NF) and matching over the cover frequency band, and 2) the linearity. A high linearity is essential to minimize unwanted mixing of blockers, generating many intermodulation distortion products throughout the spectrum. In this work, in order to achieve sufficient input matching quality (i.e., S_{11} <-10dB), low NF, high linearity including both IIP_2 and IIP_3, and low power consumption, a novel UWB balun-LNA is introduced, which can show more optimum tradeoffs among the desired parameters and befit ultra-scaled CMOS technologies.

The conventional common-gate (CG) LNA [2], which was preferable for its wideband impedance matching capability ($R_{in} = 1/g_m$), unfortunately shows a high NF (typically greater than 3 dB). In this work, we extend the concept from [3] that employs three common-source (CS) amplifiers in cascade as the LNA core, proposing an UWB balun-LNA that is capable to generate differential outputs, avoid any inductor, improve output gain-phase balancing and enhance both IIP2 and IIP3.

Section II discusses the design considerations of the proposed wideband balun-LNA. Section III provides the simulation results. The conclusions are drawn in Section IV.

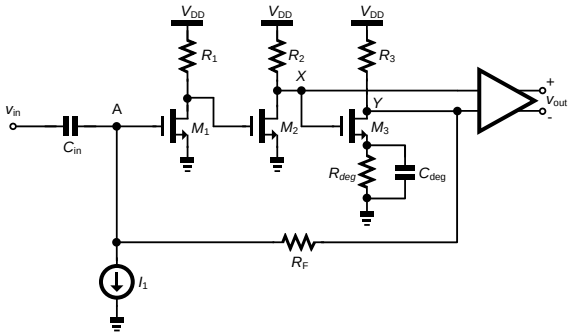


Fig. 2. Schematic of the proposed UWB balun-LNA.

II. Proposed UWB Balun-LNA

The schematic of the proposed UWB balun-LNA is depicted in Fig. 2. The input signal is fed into the CS

input stage. The external capacitor C_{in} is for AC coupling. With the high-pass corner frequency as low as 50 MHz, C_{in} is selected as 120 pF to guarantee the high-quality matching at low frequency. In this work, the LNA employs three CS stage in cascade to provide the sufficient loop gain for the negative feedback with R_F. The input transistor M_1 has a large width to minimize the noise where the thermal noise of MOS device is approximately given by $I_n^2 = 4kT(2g_m/3)$. The output signal is obtained from the pseudo-differential sensing i.e. subtracting v_Y from v_X. Based on such a pseudo-differential sensing, the even-order linearity (IIP2) can be improved due to cancellation. However, the non-linearity cancellation relies on phase and gain matching between the two paths which are nodes *X* and *Y*. The gain of the third stage is therefore sized to offer a gain close to 0 dB. In [3], the third stage of the LNA is a simple CS amplifier which provides relatively a large gain. In this case the nonlinearity cancellation is degraded.

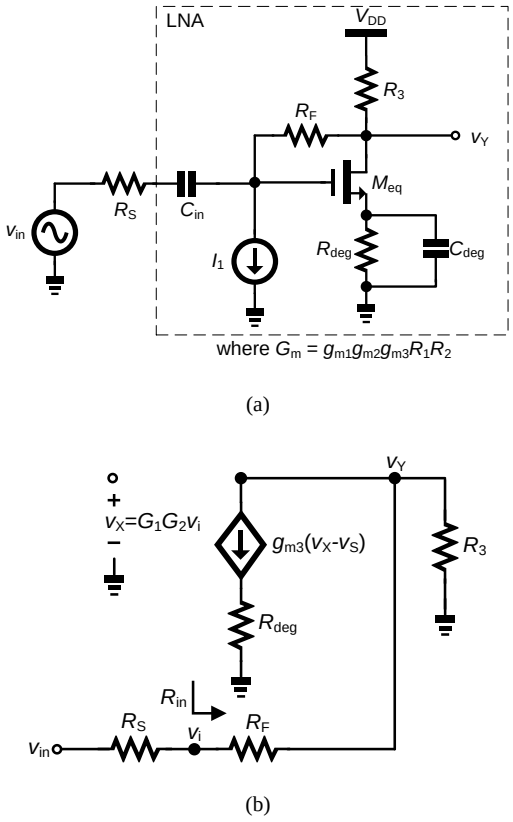


Fig. 3. LNA's (a) Equivalent circuit of the proposed balun-LNA and (b) its small signal model.

In this work, *RC* source degeneration is applied for the third stage to lower the gain which provides better matching between nodes *X* and *Y*. Also, the linearity of the third stage can be improved due to the source degeneration for the third stage which can lower the overall IIP_3. However, adding the source degeneration resistor R_{deg} degrades the high frequency input matching. Thus, we also add the degeneration capacitor C_{deg} to boost up the bandwidth of the balun-LNA which also helps the input impedance matching at high frequency.

The gain and R_{in} calculations are based on the equivalent circuit and its small signal model as shown in Fig. 3. The gain and the input impedance can be derived as,

$$G = \frac{v_X - v_Y}{v_{in}} = \frac{G_1G_2(1+G_3)}{1+\frac{R_S}{R_F}(1+G_1G_2G_3)}, \quad (1)$$

and

$$R_{in} = \frac{R_F}{1+G_1G_2G_3}, \quad (2)$$

where

$$\begin{aligned} G_1 &= g_{m1}R_1 \\ G_2 &= g_{m2}R_2 \\ G_3 &= g_{m3}(R_3//R_F) \end{aligned} \quad (3)$$

Noting that the three CS amplifiers are combined to represent the original circuit equivalently to simplify the analysis. The other design considerations are similar to those described in [3], which are omitted here for sake of brevity.

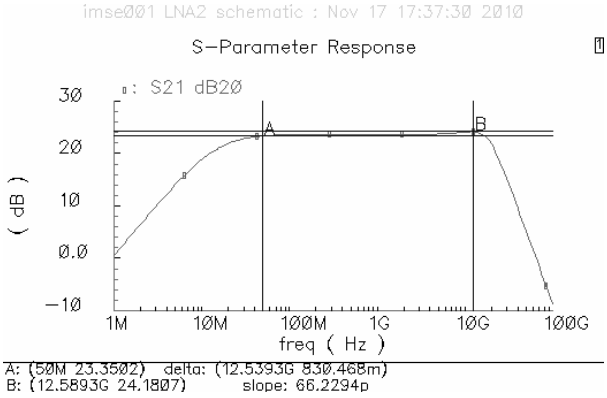


Fig. 4. Simulated S_{21} form of the LNA.

III. Simulation Results

The proposed UWB balun-LNA is designed and optimized in a 65-nm CMOS process with Cadence™ as the simulator. The employed devices are 1.2-V thin-oxide transistors. The loading capacitance is assumed to be 100 fF (differentially). Figure 4 shows the simulated S_{21} of the balun-LNA. The voltage gain ranges from

23.3 to 24.2 dB from 50 MHz up to 10 GHz. The simulated S_{11} of the LNA is plotted in Fig. 5. The S_{11} is less than -10 dB over the covered frequency.

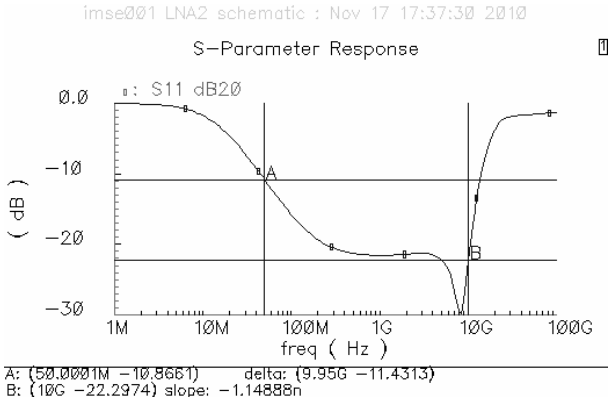
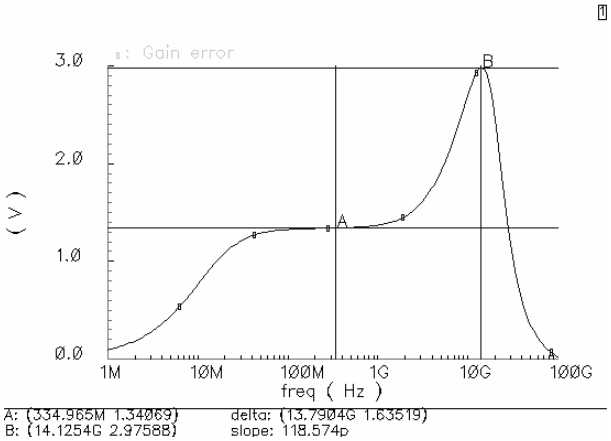
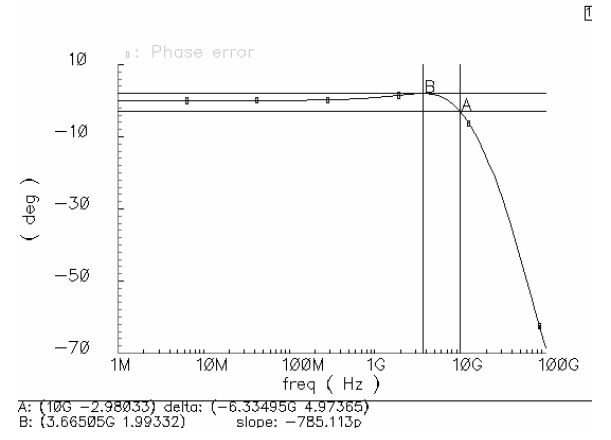


Fig. 5. Simulated S_{11}.



(a)



(b)

Fig. 6. Pseudo-differential sensing's mismatch (a) gain and (b) phase.

We also concern the gain and phase matching of the nodes X and Y throughout the passband. The simulated gain and phase mismatch are plotted in Fig. 6(a) and (b), respectively. The gain mismatch ranges from 1.3 to 3 dB and the phase mismatch ranges from -3.0º to 2.0º from 50 MHz to 10 GHz. With the better gain and phase matching due to the sizing strategy as described as Section II, a better IIP_2 can be achieved.

The achieved NF is plotted in Fig. 7, which varies from the minimum 2.5 dB, up to 3.4 dB at 10 GHz.

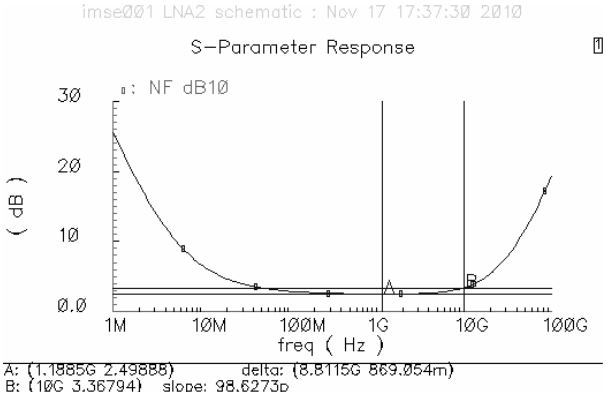


Fig. 7. NF of the UWB balun-LNA.

For the IIP_2 and IIP_3 simulation results, the two-tone test is applied. The input frequencies of the two tone signals are 4 GHz and 5 GHz. Thus the IM_2 and IM_3 are located at 1 GHz and 3 GHz, respectively. The simulated IIP_2 and IIP_3 of the balun-LNA as shown in Fig. 8 and Fig. 9 are +29.1 and -2.7 dBm, respectively. Table I compares the performance of this work with [3], confirming the feasibility of the proposed UWB balun-LNA in improving both IIP3 and IIP2 with minor add-on circuitry. The other parameters are maintained highly comparable.

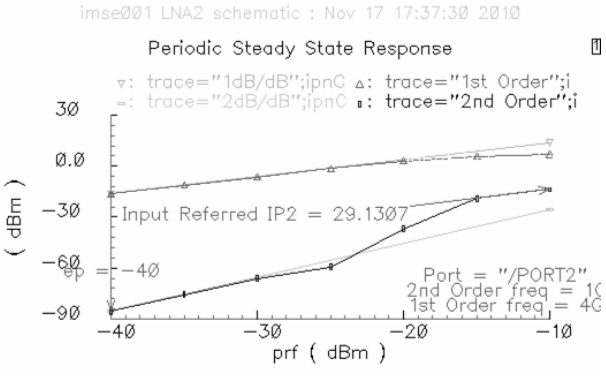


Fig. 8. IIP_2 of the UWB balun-LNA.

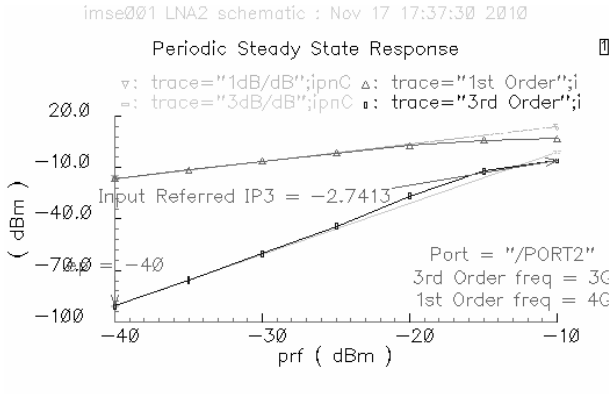


Fig. 9. IIP_3 of the UWB balun-LNA.

TABLE I
COMPARISON OF THE PROPOSED BALUN-LNA
TO THE STATE-OF-THE-ART.

	[3]	This work*
Technology	65 nm	65 nm
Voltage Supply (V)	1.2	1.2
Bandwidth (GHz)	0.05-10	0.05-10
S_{11} (dB)	-10	-10
S_{21} (dB)	18-20	23.3-24.2
Noise Figure (dB)	2.9-5.9	2.5-3.4
IIP_2	14-19.5	29.1
IIP_3	-11.2/-7	-2.7
Power (mW)	22	21.4

* Simulation results.

IV. Conclusions

A novel UWB balun-LNA employing cascade of CS amplifiers with resistive feedback, pseudo-differential sensing and partial *RC* degeneration showing improved linearity and better output gain-phase balancing is demonstrated in 65-nm CMOS. Extensive simulation results verify the feasibility of the circuit with respect to the state-of-the-art. Throughout the covered band the simulated voltage gain is >23.3 dB whereas the noise figure is <3.4 dB. The IIP_2 is 29.3 dBm and the IIP_3 is -2.7 dBm. The power consumption is 21.4 mW at 1.2 V.

Acknowledgement

This work was supported by the Research Committee of University of Macau, and Macao Science and Technology Development Fund (FDCT).

References

[1] S. Chehrazi; A. Mirzaei; R. Bagheri; A. A. Abidi; "A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-Band Use," in *Proc. IEEE CICC*, pp. 801-804, Sept. 2005.

[2] H. Zhang, X. Fan, and E. S. Sinencio, "A Low-Power, Linearized, Ultra-Wideband LNA Design Technique," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp.320-330, Feb. 2009.

[3] B.Razavi, "Cognitive Radio Design Challenges and Techniques," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1542-1553, Aug. 2010.