10.5 A 0.024mm² 8b 400MS/s SAR ADC with 2b/Cycle and Resistive DAC in 65nm CMOS

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The successive-approximation (SA) algorithm is traditionally used for low-bandwidth applications because it requires n clock cycles or more to obtain n-bit resolution. However, the use of modern nanometer CMOS technologies and special design solutions overcome the speed limit, enabling conversion rates in the hundreds of MHz with very low power consumptions [1]. This design uses the successive-approximation method to obtain 8b up to 400MS/s with very low power using a 1.2V supply. Key features of the architecture are a resistive DAC and a 2b-per-cycle conversion with interpolated sampling front-ends and shift registers. A cross-coupled bootstrapping network is also implemented to alleviate the signal-dependent clock feed-through. The very compact layout leads to a silicon area of 0.024 mm².

Converting more than one bit per cycle in SA schemes requires using multiple reference voltages that scale along the conversion cycle. Since this need leads to complex and multiple capacitor-based DACs [2], this design uses a Kelvin divider and an effective switch-selection network. Moreover, dynamic bit registers and synchronous successive approximation operation avoid the possible speed bottleneck established by a conventional SAR logic.

Figure 10.5.1 shows the block diagram of the proposed architecture. The shift registers control 170 switches to provide two differential reference voltages, V_{rH} and V_{rL}. Two sampling front-ends generate the difference between input and references. The differential signals serve a 3-level interpolation network with three fast comparators. An on-chip foreground offset calibration circuit minimizes the offset of the comparators. The scheme adjusts the comparator offset with digitally controlled MOS-capacitance located at the output of the comparator. The use of interpolation reduces the number of switches and shift registers, and results in diminishing consumed power and area.

Figure 10.5.2 shows the schematic of the sampling front end. Capacitors C_S sample the input signal during the sampling phase, Φ_S, and hold it for the entire conversion period. The reference voltages at the left terminal of C_S shift the differential voltages V_{in} at the comparator input. The use of a resistive DAC enables a very fast settling with a relatively small dynamic and reasonable power, since it is required to charge only the parasitic capacitances including the parasitics of switches, input capacitance of the comparator and parasitics of the C_S, but not the C_S itself due to the high-impedance node at the comparator input.

Clock feed-through occurring when sampling the input signal is a key limit to the overall accuracy. Bootstrapping the sampling switch, driven with an almost constant V_{GS}, minimizes the clock feed-through. However, the rising edge of the bootstrapped clock phase depends on V_{in}. This determines a second-order signal-dependent clock feed-through term that is alleviated by the cross-connected capacitance C_C. The value of C_C matches the parasitic C_{gd} of M_{SW}.

Figure 10.5.3 shows the resistive DAC consisting of 128 taps connected between V_{ref} and ground. It also includes 170 switches which has been reduced by 1/3 from the original 255 switches, due to the interpolation. The 127 shift register unit with the AND function is laid out with the corresponding switch locally. The inputs of the shift registers are the corresponding approximation phases and the determined digital bits. As shown in Fig. 10.5.3, the two active switches in the 4th cycle are quite close to each other to be able of sharing one shift register, thus achieving power and area optimization. V_{ref} is at mid-supply to allow the use of single NMOS switches. This choice enables rapid settling having minimum parasitic capacitances. Figure 10.5.3 also highlights an example of switching operation for selecting the positive reference voltage from the resistive DAC. The selection for obtaining the complementary reference is similar. The ADC approximates the input with four steps. At the first step, all the digital bits given to the shift registers are reset to '0' and Φ_1 will enables two switches to provide $3V_{ref}/4$ and V_{ref} to $V_{rH,p}$ and $V_{rL,p}$, respectively. The following steps are similar but with the control of the determined digital bits. At the last cycle, since the difference of $V_{rH,p}$ and $V_{rL,p}$ is twice of V_{LSB} ($V_{ref}/2^8$), only 128 resistive taps of the DAC would be required. As the matching of the resistive DAC is not an issue in 8b, reducing the taps by half can save significant area and also alleviate the gradient effect in the DAC.

The already determined bits select the voltages needed for the next conversion step by closing the related switches. An alternative circuit, different from the AND gates structure shown in Fig. 10.5.4 (a), makes the selection while saving power and area. Figure 10.5.4 (b) presents that special configuration of inverters, using our method for the 1011 selection control, referring to the one used at the 3rd-step in Fig. 10.5.3. The cascade uses the output of an inverter as ground connection of the subsequent one. The consumption is low and the speed is very high. The operation, similar to pass transistor logic, foresees at the beginning of the conversion cycle, all zeros at the input for setting the outputs V_X at V_{DD}. Only 1011 at the input brings the control of the last inverter, used to drive the N-channel switch, to zero. The operation is very fast because the speed only depends on the transition time of the last inverter, being the controls of others already set.

The prototype of the ADC is fabricated in 65nm CMOS with low-V_T option. Figure 10.5.7 shows the chip micrograph. The ADC core occupies 154×158μm². The on-chip foreground digital calibration is implemented to alleviate the comparator offset and occupies 35×117μm². The large INL and DNL of 5 LSB are optimized to 1 LSB by the calibration. Figure 10.5.5(a) shows that the SNDR is flat and above 46dB from 50MS/s to 350MS/s. At the maximum conversion rate of 400MS/s, the SNDR is 44.5dB. Figure 10.5.5(b) shows the measured SNDR versus the input frequency. The ADC consumes 4mW at 400MS/s from a 1.2V supply, resulting in a peak FOM of 73 fJ/conversion-step. The reference DAC consumes 500μW from the mid supply using about 12% of the total power. At 250MS/s, the ADC consumes 1.8mW from a 1V supply, resulting in a peak FOM of 42 fJ/conversion-step. Figure 10.5.5(c) shows the frequency spectrum for a low-frequency input and Fig. 10.5.5(d) shows the spectrum for a near-Nyquist tone. Figure 10.5.6 summarizes the performance of the proposed ADC. It achieves a smaller active area and a lower FOM as compared to the previously reported 7b+ 200M+S/s ADCs. It is also faster than the previous single-channel successive approximation ADC with SNDR>40dB.

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References:
[1] W. Liu, Y. Chang, S.-K. Hsien, et al., "A 600MS/s 30mW 0.13μm CMOS ADC Array Achieving Over 60dB SFDR with Adaptive Digital Equalization," *ISSCC Dig. Tech. Papers*, pp. 82-83, Feb., 2009.
[2] Z. Cao, S. Yan, and Y. Li, "A 32mW 1.25GS/s 6b 2b/Step SAR ADC in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 542-543, Feb., 2008.
[3] Y. Shimizu, S. Murayama, K. Kudoh, and H. Yatsuda, "A Split-Load Interpolation-Amplifier-Array 300MS/s 8b Subranging ADC in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 552-553, Feb., 2008.
[4] L. Brooks and H.-S. Lee, "A Zero-Crossing-Based 8b 200MSs Pipelined ADC," *ISSCC Dig. Tech. Papers*, pp. 460-461, Feb., 2007.
[5] Y.-D. Jeon, Y.-K. Cho, J.-W. Nam, et al., "A 9.15mW 0.22mm2 10b 204MS/s Pipelined SAR ADC in 65nm CMOS," *IEEE CICC*, Sept., 2010.

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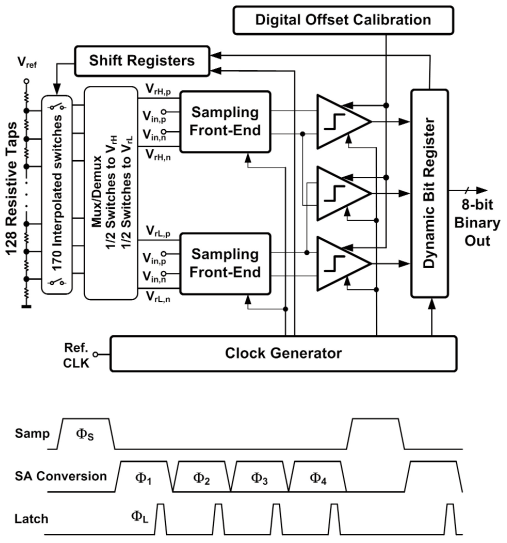

Figure 10.5.1: ADC architecture and timing diagram.

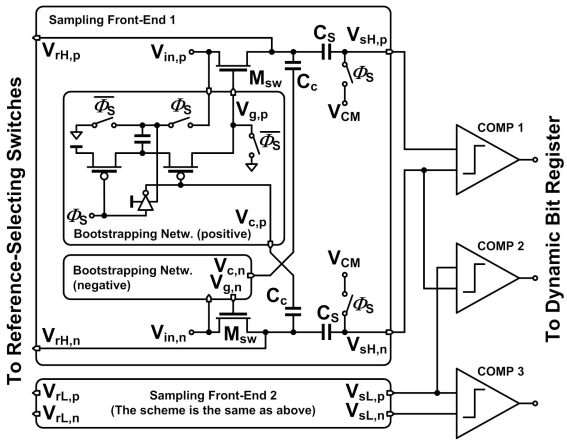

Figure 10.5.2: Interpolated sampling front-ends with cross-coupled bootstrapping network.

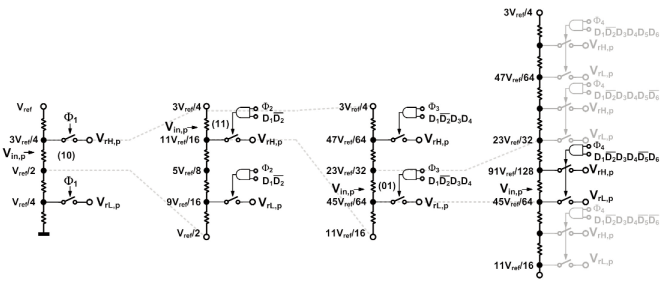

Figure 10.5.3: Switching of the reference voltage.

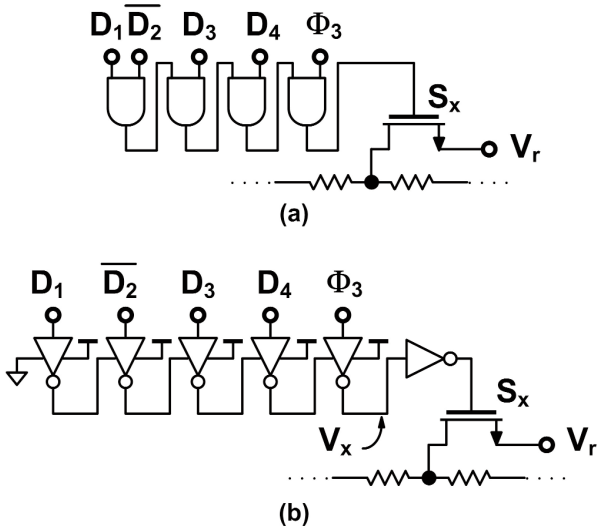

Figure 10.5.4: Implementation of the shift-register unit in 3rd conversion cycle with (a) AND gates and (b) inverters.

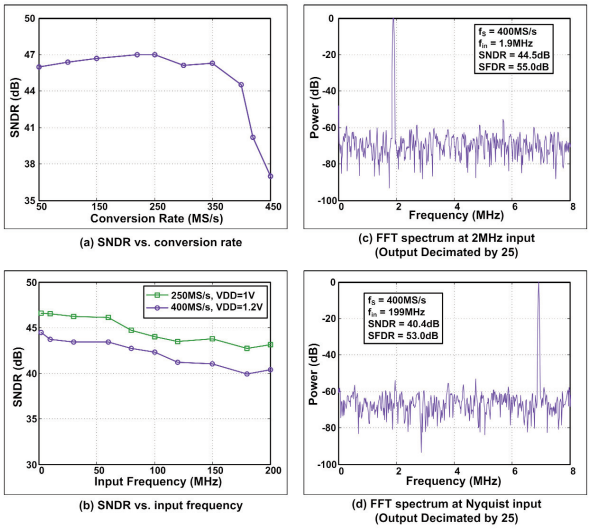

Figure 10.5.5: Measured SNDR versus conversion rate or input frequency.

Specifications	ISSCC'09 [1]	ISSCC'08 [3]	ISSCC'07 [4]	CICC'10 [5]	This Work	
Architecture	TI-SAR	2-Step	Pipelined	TI-SAR	SAR	
Technology (nm)	130	90	180	65	65	
Resolution (bits)	8	8	8	10	8	
Sampling Rate (MS/s)	600	300	200	204	400	250
Supply Voltage (V)	1.2	1.2	1.8	1	1.2	1
SNDR (dB)	47	46.1	40.3	55.2	44.5	46.7
Power (mW)	30	34	8.5	9.15	4	1.8
FOM (fJ/Conv.-step)	208	680	510	95.4	73	42
Active Area (mm^2)	1.1	0.29	0.05	0.22	0.024	

Figure 10.5.6: Performance summary and comparison with the state-of-the-art ADCs.

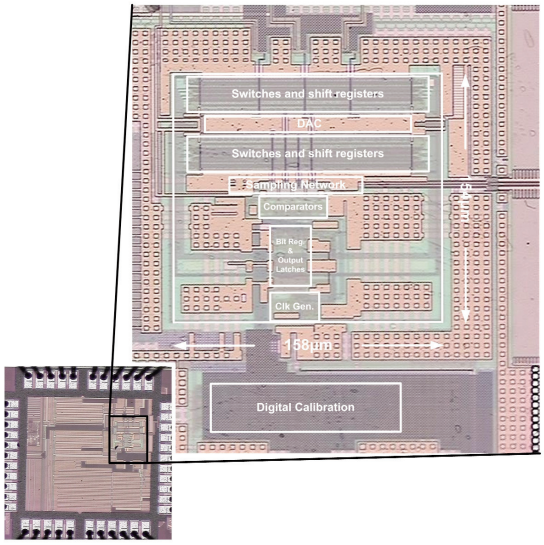

Figure 10.5.7: Chip micrograph.

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