An Ultra Low Power 9-bit 1-MS/s Pipelined SAR ADC for Bio-medical Applications

Guohe Yin[1, 2], U-Fat Chio[2], He-Gong Wei[2], Sai-Weng Sin[2], Seng-Pan U[2], Rui Paulo Martins[2, 3], Zhihua Wang[1]

1. Institute of Microelectronic, Tsinghua University, Beijing, China

[1]ma96588@umac.mo

2. Analog and Mixed Signal VLSI Laboratory, FST, University of Macau, Macau, China

[2]TerrySSW@umac.mo

3. On leave from Instituto Superior Técnico/TU of Lisbon, Portugal

***Abstract*—This paper presents a pipelined successive approximation register analog-to-digital converter (SAR ADC) for bio-medical applications based on 65 nm CMOS technology. Without using op-amp, the proposed 9-bit pipelined SAR ADC can reduce the capacitance from 512C to 64C. The pipelined architecture can enhance the operation efficiency of the ADC and also save the digital power consumption in the SAR. The simulation results show that the total power of the ADC is 10.26 μW only, and the figure of merit (FOM) of the ADC is 28.3 fJ/conversion-step.**

Keywords- SAR ADC; pipelined; ultra-low power; bio-medical applications.

I. INTRODUCTION

With the development of the healthcare electronics system, there is an increasing demand for portable and wearable devices to continuously monitor vital bio-signals such as ECG, EMG and AAP, etc, whose frequencies span from DC to a few MHz [1]. The analog-to-digital converter (ADC) with Mega-Hertz conversion rate is required to convert the vital signals to the digital form which can be analyzed by the digital processor. To maximize the battery life, energy-efficient ADCs are needed. The Successive Approximation Register (SAR) ADC architecture is well suitable for large-scale wireless sensor and bio-medical applications due to its moderate speed, resolution and very low-power consumption.

An N-bit charge redistribution SAR ADC consists of N+1 capacitors having a total capacitance of $2^N C_0$, where C_0 is the unit capacitance. Due to this large capacitance, the power is proportional to the charge/discharge of the capacitor array by the switch sequence. The conventional capacitor array consumes more power in charging and discharging the capacitor array. Meanwhile, the ADC uses the bottom plate of the capacitor array to sample the input signal. To drive such large capacitive load, a power-hungry buffer is demanded before the ADC. All these consume significant power [2].

This paper proposes a low-power 9-bit 1MS/s pipelined SAR ADC without the use of any op-amps. With the pipelined architecture, the conversion rate in each stage can be relaxed thus reducing the digital power which is the domination in the SAR ADC. In addition, the proposed ADC also reduces the sampling capacitance and save the power of the switch buffers, as well as the input driver of the ADC.

II. PROPOSED ADC ARCHITECTURE

As shown in Fig. 1, the proposed 9-bit pipelined SAR ADC architecture consists of a 5-bit coarse stage, a 5-bit fine stage, a clock generator and a digital error correction circuit. Each stage is mainly composed by a set of binary weighted capacitor DAC array, a comparator and 5-bit successive approximation registers, etc. The switch S_1 connects the MSB DAC array in coarse stage and the LSB DAC array in fine stage to share the charge during pipelined operation. The controlling phases are generated from the clock generator. To alleviate the error induced by the comparators and DAC arrays, the digital error correction is applied to combine the coarse 5-bit and the fine 5-bit digital code to the final 9-bit output code. The circuit blocks are explained in detail in the next section.

The timing diagram of the ADC is shown in Fig. 2. Firstly, the MSB DAC array samples the input signal with the

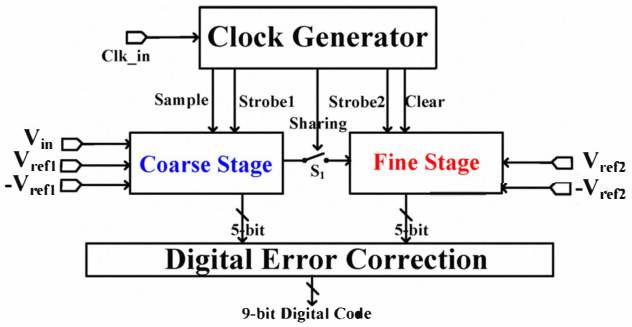

Fig.1. A proposed 9-bit two-stage pipelined ADC architecture

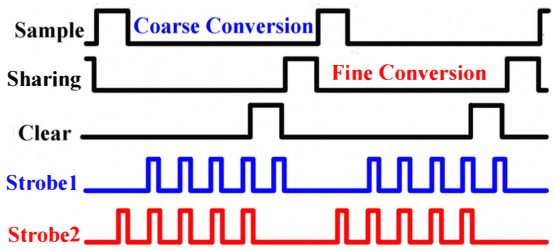

Fig.2. Timing diagram of pipelined SAR ADC

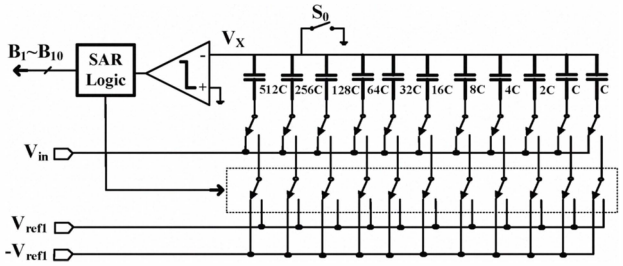

Fig.3. A 10-bit conventional SAR ADC.

bootstrapped switch [3] by the "sample" clock phase. After sampling, the "strobe1" activates the coarse stage comparator to perform the 5-bit coarse conversion with the MSB DAC array. The residue signal is produced in the MSB DAC while the coarse conversion is completed. Then, the switch S_1 is turned on in the "sharing" phase, and the MSB DAC share the charge of residue to the LSB array. Before the sharing, the memory charge of the LSB DAC array is cleared by the "clear" phase to avoid the nonlinearity effect. After sharing, the LSB DAC array starts the 5-bit fine conversion, where the fine stage comparator is triggered by the "strobe2". Meanwhile, the coarse stage samples the new input and starts the next coarse conversion in pipelining fashion.

III. SWITCHING SCHEME OF PROPOSED PIPELINED SA-ADC

Same as the conventional SAR ADC, the proposed pipelined SAR follows the binary search algorithm to perform the quantization, but the quantization is split as two steps and operates as a pipelined scheme. Fig. 3 shows a conventional 10-bit SAR ADC, which consists of a comparator, SAR logic, and a 10-bit binary weighted capacitive DAC array. $\pm V_{ref1}$ are the reference voltages for the switching of the 10-bit DAC array. By the binary search algorithm, the output voltage of the DAC (the top plate of the capacitors) V_X can be expressed as

$$V_X = -V_{in} - V_{ref1} + \sum_{i=1}^{10} \frac{B_i}{2^i} 2V_{ref1}$$

$$= -V_{in} - V_{ref1} + \sum_{i=1}^{5} \frac{B_i}{2^i} 2V_{ref1} + \sum_{i=6}^{10} \frac{B_i}{2^{i-5}} \frac{2V_{ref1}}{2^5} \quad (1)$$

where V_{in} is the sampled input signal, B_i is the comparison result in the i-bit conversion cycle. Supposing there is another reference voltage V_{ref2}, and the relationship between V_{ref1} and V_{ref2} is given as below:

$$V_{ref2} = \frac{V_{ref1}}{2^5} \quad (2)$$

Therefore, the eq. (1) can be expressed as

$$Vx = -V_{in} - V_{ref1} + \sum_{i=1}^{5} \frac{B_i}{2^i} 2V_{ref1} + \sum_{i=1}^{5} \frac{B_{i+5}}{2^i} 2V_{ref1} \quad (3)$$

Eq. (3) reveals that the single step 10-bit quantization of SAR ADC can be equalized as a two-step scheme, where the 10-bit DAC array should be split as two 5-bit DAC arrays with different reference voltages.

Fig. 4 shows the circuit diagram of the capacitive DAC arrays of the proposed pipelined SAR ADC in single-end scheme, which are implemented differentially in transistor-level. The 5-bit MSB and 5-bit LSB DAC arrays are performed the switching with $\pm V_{ref1}$ and $\pm V_{ref2}$, respectively. The 5-bit coarse code is quantized in the coarse stage, where the output voltage V_{X1} of the MSB DAC can be derived as

$$V_{X1} = -V_{in} - V_{ref1} + \sum_{i=1}^{5} \frac{B_i}{2^i} 2V_{ref1} \quad (4)$$

Fig. 5 shows the switching of MSB and LSB DAC arrays in sharing phase. After the switch S_1 is turned on, the LSB DAC can share a half of charge from the MSB, since the identical capacitance of the 5-bit DAC arrays. The sharing charges contain the residue information which is the both input signal and coarse code, where the coarse code is '11011' as an example in Fig. 5. Supposing that the LSB DAC is cleared before S_1 is on and the bottom plate of the LSB DAC connects to V_Y during the charge sharing, the LSB array's output V_{X2} can be calculated as

$$V_{X2} = -\frac{1}{2} V_{in} - \frac{1}{2} V_{ref1} + \frac{1}{2} \sum_{i=1}^{5} \frac{B_i}{2^i} 2V_{ref1} - \frac{1}{2} V_Y \quad (5)$$

After sharing, the switch S_1 is turned off and the fine conversion starts in the LSB array. The top plate voltage on the LSB array, V_{X2} becomes as

$$V_{X2} = \frac{1}{2}(-V_{in} - V_{ref1} + \sum_{i=1}^{5} \frac{B_i}{2^i} 2V_{ref1} - V_Y - 2V_{ref2} + 2\sum_{i=1}^{5} \frac{B_{i+5}}{2^i} \frac{2V_{ref2}}{2^5}) \quad (6)$$

Since the output voltage of the LSB DAC array must be equivalent to eq. (3) dividing by half during the fine

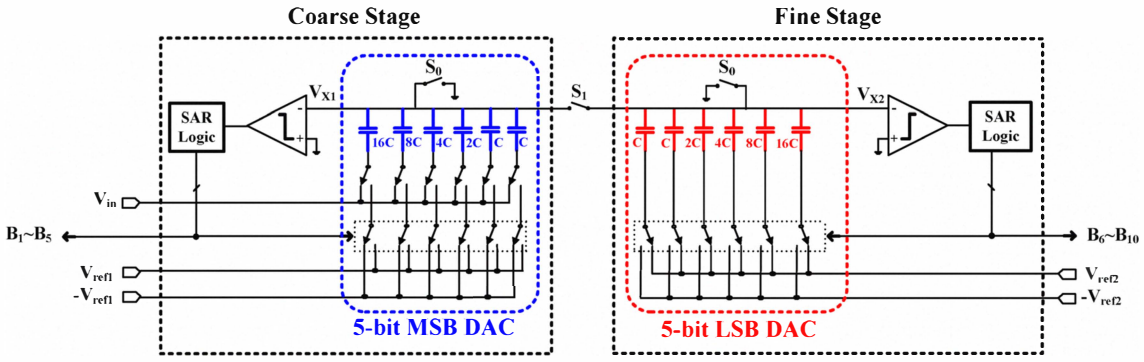

Fig.4. Capacitive DAC arrays of the proposed pipeline SAR ADC

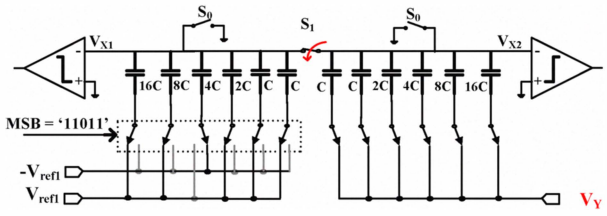

Fig.5. Circuit diagram of MSB and LSB DAC arrays in sharing phase for equation (5)

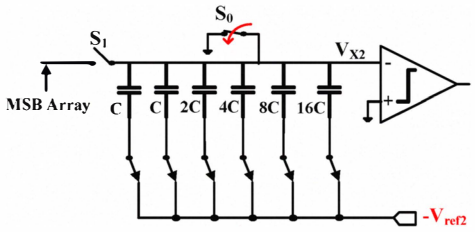

Fig.6. Pre-charging of LSB DAC arrays in clear phase

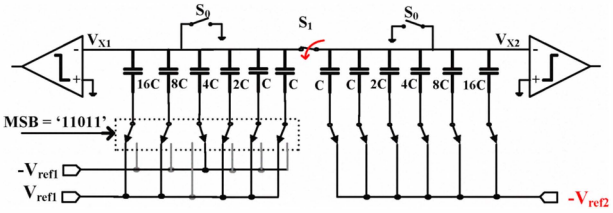

Fig.7. Circuit diagram of MSB and LSB DAC arrays in sharing phase with determined LSB reference voltage

conversion, V_Y can be derived from eq. (3) and eq. (6) as

$$V_Y = -2V_{ref2} \tag{7}$$

Eq. (7) means that, in order to implement the correct binary search algorithm during the fine conversion, the bottom plates of the LSB DAC array should be connected with $-2V_{ref2}$ at the sharing phase. However, if the dynamic range of the ADC approaches to the supply voltage, which is $1V_{p-p}$ in 65 CMOS process, the required reference voltages $|2V_{ref2}|$ will be higher than the supply voltage. Therefore, the realizable switching of $-2V_{ref2}$ is accomplished in two phases. The LSB DAC array is pre-charged to $-V_{ref2}$ in the clear phase as shown in Fig. 6, and then the bottom plate of LSB DAC stays connected with $-V_{ref2}$ in the sharing phase as shown in Fig. 7.

For the 5-bit binary weighted capacitor array, the total capacitance is 32C, where C is the unit capacitance. Comparing to a 9-bit conventional SAR ADC, the total capacitance in the proposed pipeline SAR can reduce the capacitance from 512C to 2*32C. It can save the power consumption during the charging of DAC, as well as the switching power dissipated on the switch buffers. The energy dissipation of charging the capacitor can be given as

$$E = C \cdot \Delta V^2 \tag{8}$$

where ΔV is the voltage difference between the capacitor. As ΔV reduces to 1/32 for the switching of LSB DAC array, it can save the power drastically in the fine conversion [4].

IV. Circuit Implementation

A. Comparator

The comparator circuit is employed by the dynamic latch [5]. The auto-zeroed preamplifier is preceded to the dynamic latch alleviating the comparator offset, with the gain of about 16. To improve the noise performance of the comparator, two capacitors with 10fF are connected to the output of the comparator. Although the comparator's settling time is enlarged by the loading capacitors, it's still short enough for conversion in this design.

For the 9-bit traditional SAR ADC with conversion rate of f_S, the speed of the comparator is required as $10f_S$. Although in this 1 MS/s ADC includes two comparators, the speeds of the comparators are about 5 MS/s, only a half of the one in the traditional SAR ADC. The power of two dynamic latches in the proposed ADC will not consume more power compared to the one in traditional SAR ADC, as it is proportional to the conversion rate.

B. Digital Error Correction

The digital error correction is employed here to eliminate the nonlinearity from the comparator offsets in coarse and fine stages. The 10-bit codes are processed in the digital error correction with 1-bit overlapping, where the last bit of the coarse code and the first bit of the fine code is combined into one bit with digital addition. Finally, a 9-bit output code is obtained.

C. Successive Approximation Registers

The successive approximation registers requires the D Flip-Flops to provide the approximation clock cycles. For the traditional SAR ADC, N-bit ADC needs N+1 D-FFs. In the proposed 9-bit ADC, only 6 D-FFs are utilized instead of 11 D-FFs, since both the coarse and fine stages contain only 5 conversion cycles and share the D-FF. Therefore, the speed of the digital logics almost reduces to half and the digital power is optimized.

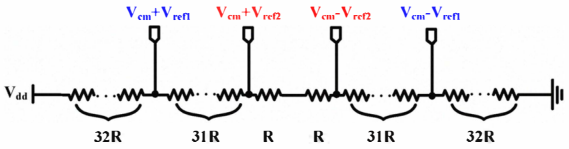

Fig.8. Resistive ladder providing the reference voltages $\pm V_{ref1}$ and $\pm V_{ref2}$

D. Reference Ladder

The reference voltages $\pm V_{ref1}$ and $\pm V_{ref2}$ are generated from the resistive ladder, where 128-tap resistors are demanded. The resistive ladder is shown as in Fig. 8. In this design, the tap resistor is 1.6 KΩ for the unit capacitance of 16 fF in the DAC arrays.

V. Simulation Results

The proposed pipelined SAR ADC has been verified with transistor-level simulation based on the 65nm CMOS technology with high threshold option.

The static performance is characterized through the differential nonlinearity (DNL) and integral nonlinearity (INL).

As shown in Fig. 9, the simulated DNL and INL are +0.46/-0.66 LSB and +0.37/-0.53 LSB, respectively. Fig. 10 shows a frequency spectrum simulation @ f_{in} = 403.3 KHz and f_S = 1 MS/s with the SNDR of 53.0 dB. The 50 times Monte-Carlo simulations in Fig. 11 show that the proposed 9-bit pipelined SAR ADC SNDR can achieve an average of 53.3 dB. Fig. 12 and Fig. 13 illustrate the SNDR of the ADC versus the input frequency and the sampling rate variation, respectively.

For the figure of merit (FOM) [6] of the ADC which is defined as FOM = Power/(2^{ENOB}*fs), this work can be achieve the FOM as 28.3 fJ/conversion-step. The ADC simulation results are summarized in the Table I.

VI. Conclusion

A 9-bit 1MS/s SAR ADC with pipelined architecture is presented. By the pipelined operation, the proposed ADC reduces the digital consumption as well as the total capacitance. The ADC consumes power 10.26 μW and achieves the FOM 28.3 fJ/conversion-step at the maximum sampling rate.

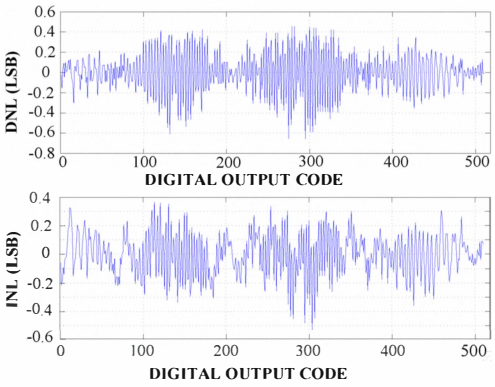

Fig.9. Simulated DNL and INL of the proposed ADC

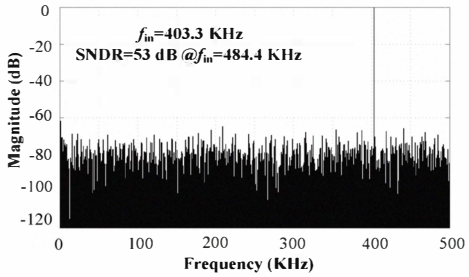

Fig.10. FFT of the digital output @ f_{in}=403.3 kHz and f_S =1 MS/s.

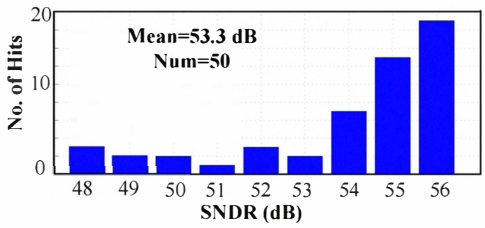

Fig.11. Histogram of SNDR of proposed novel ADC @ f_{in} =484.4 KHz and f_S =1 MS/s.

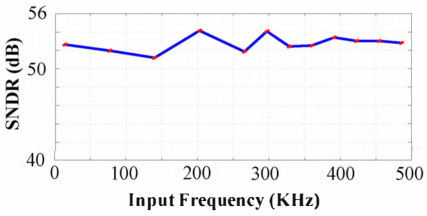

Fig.12. Simulated SNDR versus input frequency @ f_S =1 MS/s.

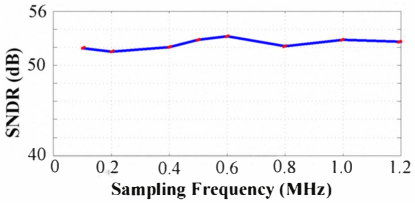

Fig.13. Simulated SNDR versus sampling rate.

TABLE I. Performance Summary of The Proposed ADC

Technology	65 nm	Power Supply	1 V
Resolution	9 bit	Power Dissipation	
Sampling Rate	1 MS/s	Analog	4.371 μW
Dynamic Range	1.0 $V_{p\text{-}p,\ diff}$	Digital	0.791 μW
SNDR(@f_{in}=484.4kHz)	53.0 dB	Reference ladder	5.098 μW
DNL (LSB)	+0.46/-0.66	Total Power	10.26 μW
INL (LSB)	+0.37/-0.53	FOM	28.3 fJ/conv-s

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References

[1] X. Zou, X. Xu, L. Yao, Y. Lian, " A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," *IEEE J. Solid State Circuits*, vol. 44, no.4, pp. 1067 - 1077, Apr. 2009.

[2] C. Liu, S. Chang, G. Huang, Yi. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," *IEEE J. Solid State Circuits*, vol. 45, no.4, pp. 731 – 740, Apr. 2010.

[3] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipelined analog-to-digital converter," *IEEE J. Solid State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.

[4] M. V. Elzakker, V. E. Tuijl , P. Geraedts, D. Schinkel, E. Klumperink, B. Nauta, "A 10-bit Charge-Redistribution ADC Consuming 1.9 uW at 1 MS/s," *IEEE J. Solid State Circuits*, vol. 45, no.5, pp. 1007 – 1015, May 2010.

[5] G. Y. Huang, C. C. Liu; Y. Z. Lin, S. J. Chang, "A 10-bit 12-MS/s successive approximation ADC with 1.2-pF input capacitance," *Procs. IEEE ASSCC*, pp. 157 - 160, Dec. 2009.

[6] J. Craninckx, G. van der Plas, "A 65 fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9 b charge-sharing SAR ADC in 90 nm digital CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 246–247, Feb. 2007.