A Fixed-Pulse Shape Feedback Technique with Reduced Clock-Jitter Sensitivity in Continuous-Time Sigma-Delta Modulators

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Abstract—**A novel fixed-Pulse Shape (PS) clock-jitter insensitive Return-to-Zero (RZ) feedback technique in CT ΣΔ modulators is presented. This technique offers a method to reduce the clock-jitter effect in feedback DAC. A switched-RC network and a zero-crossing detector are applied to generate jitter insensitive feedback pulse. This technique was verified in a designed 2nd order CT ΣΔ modulator. A stable 64dB SNDR was obtained with the clock-jitter effect of 2% of a clock cycle. Simulation results show that using the proposed technique, an SNDR improvement up to 30dB can be achieved comparing with traditional RZ DAC.**

Keywords-Clock-jitter, continuous-time sigma-delta modulator, fixed-pulse shape feedback, RC discharge, zero-crossing detector.

I. INTRODUCTION

Continuous-time (CT) sigma-delta ADC has been turned into a dominating tendency in wireless communication system with its significant advantages over the traditional Discrete-Time (DT) structure: high speed, low power and inherent anti-aliasing filtering [1]. In recent years, the designed signal bandwidth of CT ΣΔ modulators can be achieved over 20MHz to meet the most advanced communication standard. The power consumption can be reduced within 10mW [2].

In CT ΣΔ modulator design, one of the most critical non-ideality is the clock-jitter effect to the feedback DAC. Clock-jitter induces the random variation to the feedback Pulse Shape (PS), including Pulse Width (PW) variation and Pulse Position (PP) variation, which inject feedback white noise. This effect is worse in the case of Return-to-Zero (RZ) and single-bit design [3]. Because of the jitter-induced PS variation, feedback DAC directly couples noise to the input of integrators. Especially for the feedback to the 1st stage loop filter, this noise will not be shaped; hence it can increase the noise floor in FFT spectrum and degrade system SNDR significantly.

Several shaped-feedback waveform techniques have been proposed to reduce the clock-jitter sensitivity of feedback DAC in CT ΣΔ modulator. The main principle is through minimizing the feedback pulse amplitude at the end of the feedback phase to reduce the PW variation caused feedback PS variation. In [4], a SCR DAC structure was proposed to reduce clock-jitter sensitivity by generating an exponential decreasing feedback pulse. But due to the large feedback peak current, it requires a higher op-amp slew rate and GBW. A SCSR feedback DAC was proposed in [5]. It realized the same function as SCR DAC with reduced feedback peak current. However it requires a careful theoretical design and complicated clock phase generation. Besides, a common issue of shaped-feedback waveform DACs is the unprecise feedback charge amount. Thus another solution to reduce DAC clock-jitter sensitivity would be preferred, which is fixed-PS feedback, due to the lower peak current, simple clock phase and precise amount of feedback charge. This technique is proposed to fix the feedback PS to be unchanged by clock-jitter effect.

In this work, a novel fixed-PS clock-jitter insensitive feedback technique is proposed. The feedback PW can be fixed while DAC suffering clock-jitter. An accurate amount of feedback charge can be defined. This is realized by detecting a specified potential on a RC network during its discharge by using a Zero-Crossing Detector (ZCD). The designed feedback PW depends on the time constant of the RC network. The generation of the clock edge triggering the feedback pulse employs delay elements to avoid jitter-induced feedback PP variation. A 2nd order, single-bit CT ΣΔ modulator with RZ feedback was designed to verify the effectiveness of the proposed technique.

A detail introduction to the proposed feedback technique is given in Section II. Section III shows a designed example of CT ΣΔ modulator. Simulation result is discussed in Section IV. Finally a conclusion is summarized in section V.

II. RC DISCHARGE DETECTION TECHNIQUE

The structure of RC Discharge Detection (RCDD) DAC proposed to accurately determine the feedback PS is illustrated in Fig. 1. The main concept is that using ZCD to detect a time interval between two specified voltage crossing points on a discharged RC network. This interval of time is used to determining the feedback PW in order to avoid jitter-induced PW variation. The operation principle and design non-idealities of RCDD DAC will be discussed hereinafter.

A. Operation Principle of RCDD DAC

A brief implementation of RCDD feedback DAC is shown in Fig. 1(b). The feedback current I_{fb} is generated by using the

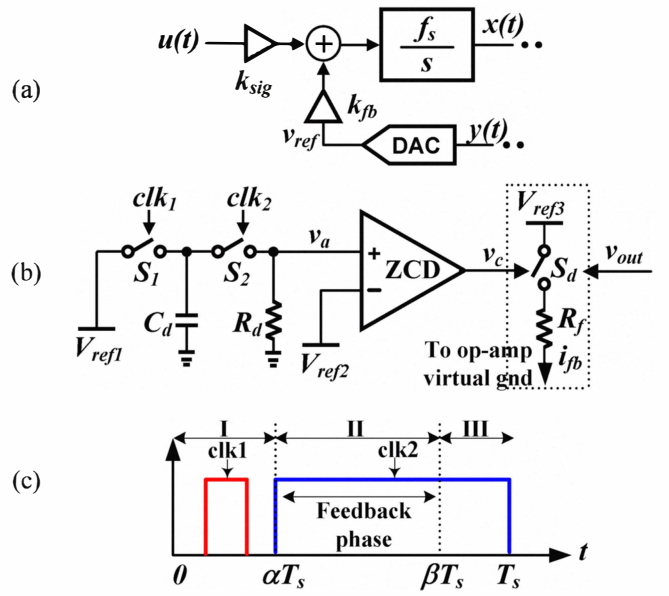

Fig. 1 (a) Signal flow expression in CT ΣΔ modulator. (b) RCDD feedback DAC. (c) Control clocks for RCDD circuit.

voltage reference V_{ref3} and the resistor R_f which is switched by S_d. The feedback control clock is generated by RCDD circuit which consists of a Switched-Capacitor-Resistor (SC-R) network and a ZCD. Fig. 1(c) shows the control clocks of the SC-R network. To avoid jitter effect, clock clk_1 and the rising edge of clk_2 are generated by delaying and logically operating the same rising edge of master clock in a clock cycle. The operation of RCDD DAC can be divided into three phases: Phase I, II and III as shown in Fig. 1(c) and Fig. 2.

1). Charging phase. In phase I, the generated clock clk_1 switches on S_1 then C_d will be charged on V_{ref1}. Because of S_2 is kept off during this phase, there is no voltage crossing can be detected by the ZCD. Since the value of V_{ref2} is larger than the ground voltage (V_{CM} in differential case), the output of the ZCD v_c will be maintained as logic '0'. Therefore S_d will be kept off and there is no feedback current in this phase.

2). Current feedback phase. Current feedback phase is from αT_s to βT_s as shown in Fig. 1(c). In this phase, the PW of the feedback current will be determined. At αT_s, clk_2 switches on S_2, since S_1 has been turned off by clk_1, C_d will be discharged through R_d. Voltage v_a will instantaneously increase to V_{ref1} then decrease exponentially as shown in Fig. 2(a). Because of the increase of v_a, up to V_{ref1} which is higher than V_{ref2}, the ZCD will detect a voltage crossing and output logic '1' as shown in Fig. 2(a) & (b). Then S_d will be turned on by v_c and feedback current i_{fb} will be generated through R_f. At βT_s, due to the discharge of C_d, v_a drops down to lower than V_{ref2} which leads ZCD output turn to '0'. S_d will be switched off and the feedback current turns to zero. Completed pulse shape of the feedback current i_{fb} is shown in Fig. 2(c). The end of the feedback pulse in a clock cycle depends on the 2nd crossing position of v_a and V_{ref2}. It is observed that the RC time constant

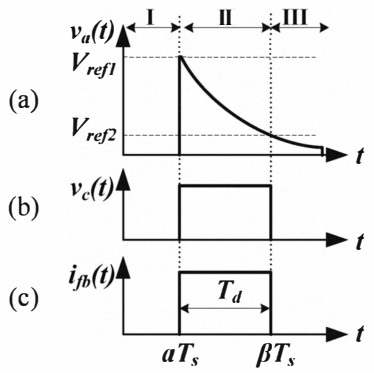

Fig. 2 DAC operations. (a) Input of the ZCD. (b) Feedback control signal v_c. (c) Feedback current pulse.

determines the feedback PW. Based on the structure of RCDD DAC shown in Fig. 1(b), the feedback PW can be calculated by

$$T_d = R_d C_d \ln\left(\frac{V_{ref1}}{V_{ref2}}\right) \quad (1)$$

3). Return to zero phase. This phase starts at βT_s. S_d is firstly turned off by the ZCD output. v_a is keeping decreasing sequentially in this phase. Its value will maintain lower than V_{ref2}, hence S_d will be kept off. Feedback current is returned to zero in this phase.

B. Clock-jitter Insensitivity

The RCDD DAC illustrated in Fig. 1(b) is clock-jitter insensitive. From (1), the feedback PW T_d can be controlled by R_dC_d since the voltage references are maintained. T_d does not depend on any clock signal therefore it is clock-jitter insensitive. Another effect caused by clock-jitter is feedback PP variation. Feedback PP is determined by the value of α and β. Its variation will change feedback coefficients. Feedback PW is equal to $(\beta - \alpha)T_s$ which is jitter insensitive using RCDD DAC, thus the feedback PP can be jitter insensitive as long as α is jitter insensitive. In the operation of RCDD DAC, the feedback current is triggered by clk_2 whose rising edge is generated by delaying master clock. So the relative position of clk_2 and the master clock is independent of clock-jitter, which means the α will not change with clock-jitter. Thus the feedback PP is clock-jitter insensitive in RCDD DAC feedback.

The operation of RCDD DAC with clock-jitter effect is illustrated in Fig. 3. The red regions represent the jittered area of clock edge. Fig. 3(a) shows the jittered master clock. clk_2 has the same jitter-induced variation on its rising edge as shown in Fig. 3(b). However the relative position between their rising edges is fixed which is equal to αT_s. In other words, the feedback PP is fixed. The waveform of voltage v_a is shown in Fig. 3(c). The exponential decreasing speed of v_a is not affected by clock-jitter. This guarantees that the 2nd voltage crossing point can be fixed relative to the 1st crossing point in every clock cycle to ensure the fixed feedback PW. Only the ending position of v_a in each clock cycle is changed due to clock-jitter effect. But it has no influence to the feedback PS. This can be

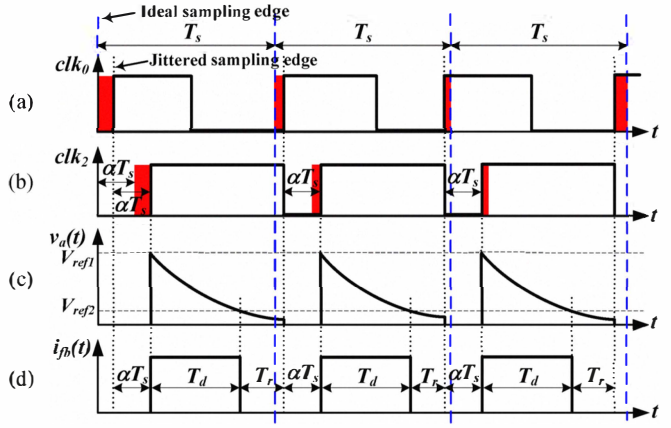

Fig. 3 Clock-jitter effect to the feedback pulse shape. (a) Jittered master clock. (b) Control clock clk_2 for RCDD circuit. (c) Transient RC discharge curve at the input of the ZCD. (d). Feedback current pulse.

observed from Fig. 3(d) which shows the feedback current pulse. It can be seen that the feedback PW and PP are all fixed in every clock cycle, so the feedback PS is clock-jitter insensitive. The only jitter-induced impact is the remain time T_r after switching off the feedback current as shown in Fig. 3(d). Since clock-jitter causes sampling position variation, the jitter-induced variation to T_r is ineluctable, however it does not compromise the jitter insensitivity function of RCDD DAC.

C. *Feedback RC Variation Insensitivity*

Feedback PW is relied on R_dC_d time constant. Therefore RC process variation will affect the feedback PS. Based on the feedback loop signal flow expression shown in Fig. 1(a), by employing the RCDD feedback DAC and RC integrator together, the output of the feedback loop filter can be written as

$$V_x = -\frac{V_{ref3}}{sR_fC_i} \tag{2}$$

where C_i is the feedback capacitor of the RC integrator and V_x represents the output voltage of the loop filter. Based on the principle of RZ feedback and the expression of feedback PW in (1), the total feedback current translated voltage integrated on C_i in a clock cycle can be derived as

$$V_{\text{int}} = -\frac{V_{ref3}R_dC_d}{R_fC_i}\ln\left(\frac{V_{ref1}}{V_{ref2}}\right) \tag{3}$$

Form the equation above, the integrated feedback signal is proportional to the capacitor ratio and the resister ratio. This relationship ensures that the feedback result will not be altered by the RC variation in feedback DAC and loop filter.

Although the RC variation will not compromise feedback result, the increase of R_dC_d will extend the feedback PW. Excess increase of R_dC_d time constant will slow down the discharge speed and lead β to be close to 1. It will compromise DAC's clock-jitter insensitivity. If v_a cannot decrease lower than V_{ref2} finally, the output of the ZCD will maintain logic "1" which means S_d cannot be switched off. The falling edge of the feedback current pulse will be determined by the falling edge

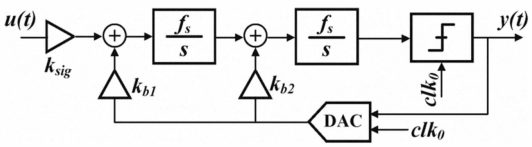

Fig. 4 System architecture of 2nd order, single bit, CT sigma-delta modulator.

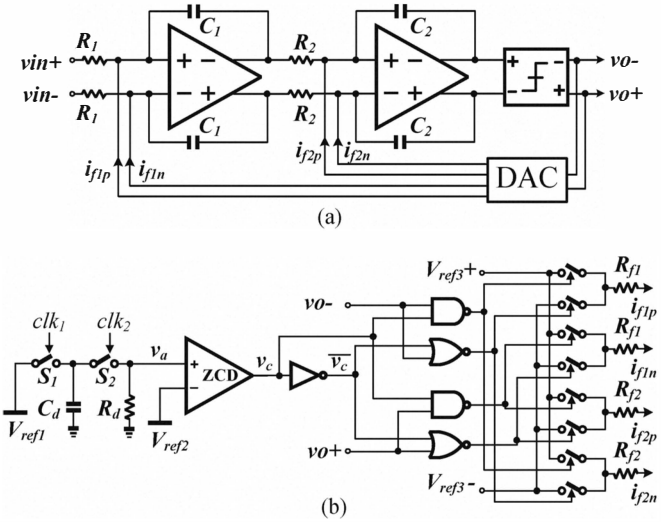

Fig. 5 Circuit implementation of 2nd order, 1-bit, CT sigma-delta modulator. (a) Overall architecture. (b) Proposed feedback DAC.

of clk_2 which is clock-jitter sensitive. Thus DAC's clock-jitter insensitive function will be lost. In order to compensate this effect, feedback pulse can be chosen as a shorter width and the value of αT_s could be smaller. This non-ideality can be avoided by choosing appropriate values of α and β based on the practical RC process variation in a specific technology.

III. CT ΣΔ Modulator Design Example

A. *System Overview*

A 2nd order, single-bit, lowpass CT ΣΔ modulator was designed to verify the clock-jitter insensitive function of the proposed RCDD feedback DAC. The sampling rate of the designed modulator is 250MS/s; the input bandwidth is 2MHz corresponding to the standard of 3G WCDMA receivers. The OSR is 64. The system model is shown in Fig. 4.

RZ feedback method was employed. The DT-CT conversion is done by using impulse-invariant transformation. The transformed CT coefficients shown in Fig. 4 were scaled down to guarantee that the signal swing do not reach the saturation level of the loop filter. The selected values of α and β are 0.2 and 0.7 respectively in this design.

B. *Circuit Implementation*

Transistor level design of the CT ΣΔ modulator shown in Fig. 4 was implemented in 65nm CMOS with 1V supplied voltage. The schematic of the designed modulator is given in Fig. 5. Active RC integrators are employed as loop filters for good linearity. The values of R_i and C_i in the integrator are determined based on the system coefficients. Fully differential

folded-cascode amplifier with gain boosting circuit was employed as the 1st stage integrator. 55dB DC gain and GBW of 750MHz which is three times of the sampling rate were achieved. The 2nd stage integrator was implemented using folded-cascode structure with much relaxed gain and GBW.

The implemented RCDD DAC is shown in Fig. 5(b). R_{fi} is the switched-resistor to generate feedback current. NAND and NOR gates are applied to determine the feedback polarity by connected with the system output. The waveforms of clk_1 and clk_2 has been shown in Fig. 1(c), they are generated by using inverter-based delay elements and NAND gates. The ZCD is implemented based on the structure presented in [6] for high transition speed.

IV. Simulation Results

The proposed clock-jitter-insensitive feedback technique is verified by simulations on transistor-level. The amplitude of the testing signal is -1.9dBFS and the frequency is 0.1MHz. Clock jitter was injected into the master clock. All the circuit noises including thermal noise, 1/f noise, kT/C noise and quantization noise are simulated in transient noise simulation.

RCDD DAC and traditional RZ DAC were employed in the designed modulator respectively to make a comparison. As shown in Fig. 6, with very slight clock-jitter, traditional RZ DAC achieved 67dB SNDR while RCDD DAC achieved 65dB SNDR. The 2dB SNDR drop is induced by the comparator noise in the ZCD in RCDD DAC. Well design of ZCD can minimize this noise. With clock-jitter increased, the maximum SNDR degradation coursed by PW variation (with jitter of 3%) is 30dB for traditional RZ DAC comparing with using RCDD DAC. The total average power consumption of the modulator using RCDD DAC is 4.5mW, while the RCDD DAC consumes 700uW power. The total power consumption of using traditional RZ DAC is 4.1mW. The proposed RCDD DAC does not greatly increase the system power consumption.

Simulated Power Spectrums Density (PSD) of designed modulators using proposed RCDD and traditional RZ DAC are shown in Fig. 7. PSDs for using both two types of DAC are compared in different clock-jitter effect conditions. From Fig. 7, the noise floor and distortion level are very close for using RCDD DAC with 1% clock-jitter and traditional RZ DAC without clock-jitter. Simulation results show that RCDD DAC effectively reduced the clock-jitter sensitivity in RZ feedback.

V. Conclusions

In this paper a novel RZ feedback technique used in CT ΣΔ modulators is presented. By using RC discharge detection technique, the clock-jitter sensitivity in RZ feedback DAC can be greatly reduced with low peak current and simple structure. It ensures that the feedback PS is unswayed by the jitter-induced PW variations in master clock. The proposed DAC was implemented in a designed 2nd order, 1-bit CT ΣΔ modulator. Its jitter insensitive function was verified through the simulation with varying clock-jitter effect. Comparison between the simulated results of using proposed DAC and traditional RZ DAC shows that ZCD noise didn't increase the noise floor evidently and the proposed feedback DAC provides a significantly improvement to reduce clock-jitter sensitivity.

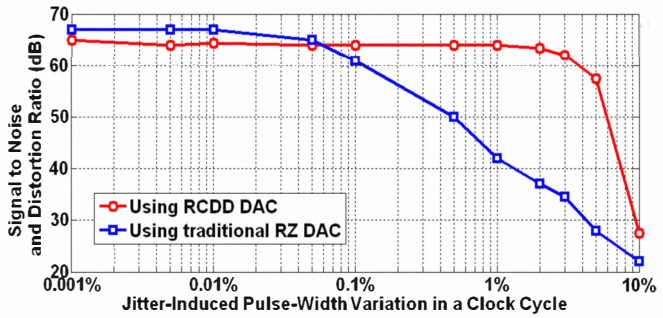

Fig. 6 Simulation (noises introduced) results for system sensitivity to the jitter-induced PW variation using RCDD DAC and traditional RZ feedback DAC.

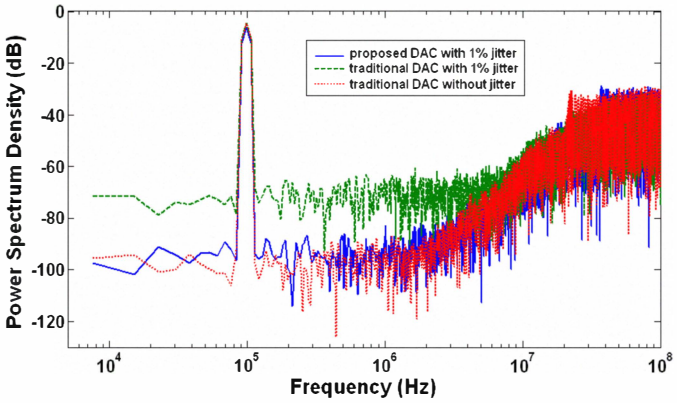

Fig. 7 Simulated PSDs (noises introduced) comparison of the modulator using RCDD and traditional RZ feedback DAC.

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