# An Efficient DAC and Interstage Gain Error Calibration Technique for Multi-bit Pipelined ADCs

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*Abstract*—**This paper presents a novel digital calibration technique for pipelined ADCs, which compensates both sub-DAC and interstage gain error. The proposed calibration technique is very efficient comparing to other existing calibration techniques, in which only additions and subtractions are employed in this algorithm, no multiplication and division is included. The simplicity of the calibration makes it very easy to be embedded in the mixed signal system design. The power and area overheads due to the calibration circuit are minimized. An example pipelined ADC is designed to demonstrate this calibration technique. Simulation results show that significant improvements can be achieved with the proposed calibration technique.**

*Keywords*— **Pipelined ADCs, digital calibration, capacitor mismatch, interstage gain error.**

## I. INTRODUCTION

Pipelined Analog to Digital Converters (ADCs) are widely used in high speed high resolution applications such as communication transceivers and imaging systems. However, the subranging architecture makes them very sensitive to the sub-DAC error and the interstage gain error in the first few stages. Traditionally, large capacitors and high performance opamps are used in the first few pipeline stage to meet the accuracy requirements. Unfortunately, with the technology scaling down, capacitor mismatches and opamp finite gain become more and more serious, high resolution is hard to be achieved if only the analog boosting and compensation technique are used. The utilization of digital assisted techniques attracts designer's attention in recent years. Those techniques first digitally measure the error arising from the error sources such as sub-DAC [1], [2] or the interstage residue amplifier [3], and compensate the error by manipulating the digital output of the pipelined ADC. They are robust comparing to analog technique, but most of them is very complex in digital circuit [1], [4], [5].

This paper presents a simple and efficient digital calibration technique for pipelined ADCs. The errors arising from the sub-DAC and interstage gain error are both compensated. The proposed calibration technique takes advantages of its simplicity. Only additions and subtractions are employed in the algorithm, no multiplication and division is used. Therefore, little digital complexity is introduced into the whole system, and the power and area overhead are minimized. An example pipelined ADC is designed with the proposed calibration technique. Simulation results demonstrate the effectiveness of this calibration algorithm.

This paper is organized as follows: first, the architecture of the example pipelined ADC is described in Section II. Section III explains the effect of the sub-DAC and the interstage gain error. Section IV describes the digital calibration algorithm. Section V shows the simulation results and the conclusions are presented in Section VI.

## II. PIPELINED ADC ARCHITECTURE

The example pipelined ADC is shown in Fig.1(a), which utilizes the conventional architecture in the literature [4], [5]. It comprises totally 7 pipeline stages. Each of the first 6 stage contains a 9-level sub-flash ADC and a 9-level sub-DAC. Unlike the conventional binary weighted capacitor DAC, unit capacitor DAC is used. The sub-DAC in each stage consists of 8 1-bit DACs. The interstage amplifier has a nominal gain of 4. The circuit of the MDAC is shown in Fig.3(a). The last stage is simply a 9-level sub-flash ADC. The signal processing model for an ADC is suggested in [1] as:

$$D = (\frac{V_{in}}{\Delta} + e_{ADC})\Delta \tag{1}$$

where $\Delta$ is the step size of the ADC, and $e_{ADC}\Delta$ is the normalized quantization error. Apply (1) in the k-th pipeline stage in Fig.1, the digital output is given by

$$D_k[n] = [\frac{V_{in,k-1}(nT_s)}{\Delta_k} G + e_{ADCk}(nT_s)]\Delta_k \tag{2}$$

Apply (2) recursively, the digital output $D_{out}$ of the pipelined ADC is represented by

$$\begin{aligned} D_{out}[n] &= D_1[n] + \frac{1}{G} D_2[n] + \cdots + \frac{1}{G^6} D_7[n] \\ &= V_{in1} + \frac{1}{4^6} e_{ADC7}\Delta_7 \end{aligned} \tag{3}$$

Since the quantization error $1/4^6(e_{ADC7}\Delta_7)$ is bounded in 1LSB, the example ADC behaves like a 36864-level ADC, which has an effective resolution of 15.17 bits. The input range of the ADC is (-4.5Δ~+4.5Δ), the amplified residue has a range of (-2Δ~+2Δ), so the example ADC has an over-range margin of (-2.5Δ~+2.5Δ) [5]. The redundancy accommodates

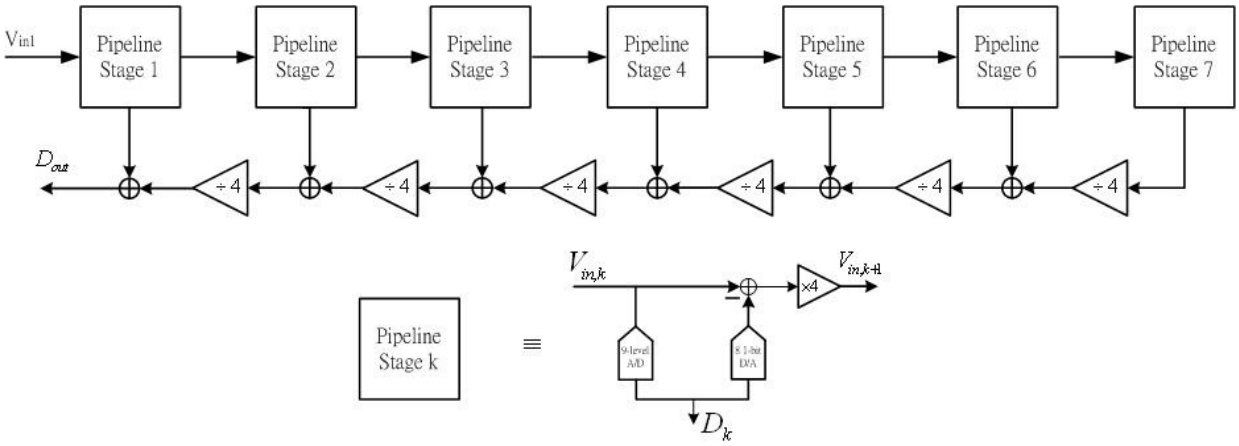


Fig. 1. Pipelined ADC Architecture.

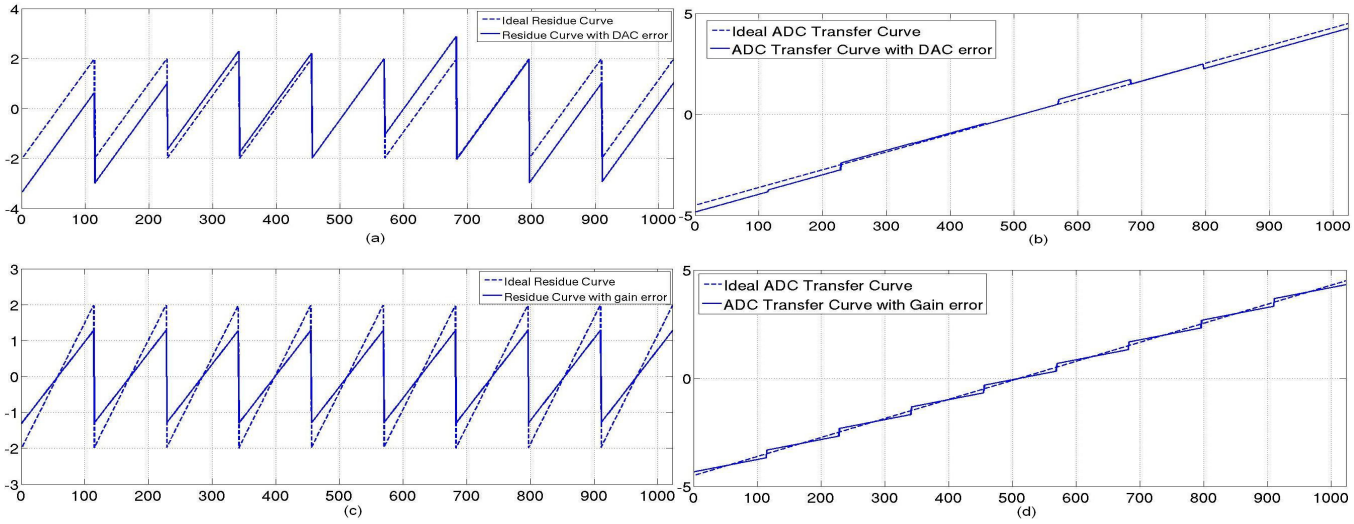


Fig. 2(a) Residue curve with DAC error. (b) ADC transfer curve with DAC error. (c) Residue curve with interstage gain error. (d) ADC transfer curve with interstage gain error

sub-ADC error and opamp offset, and is exploited by the calibration technique. For the brevity of the sequel, the step size Δ is normalized to 1.

## III. Effect of Sub-DAC and Interstage Gain Error

Pipelined ADCs are not sensitive to the sub-ADC error because they can be corrected by the digital error correction if redundancy is introduced in each of the pipeline stage [6]. However, the errors arising from the sub-DAC and the interstage amplifier make the residue transfer curve deviate from the ideal one so they can not be tolerated by the error correction. The sub-DAC error is mainly due to the process variation of the capacitors. They cause each linear segment of the residue transfer curve, and thereby the ADC transfer curve to be shifted up or down by static values, shown in Fig.2(a), (b). The major jumps or the discontinuities between each linear segment result in the missing code or large DNL error of the ADC. Obviously, if suitable values are added to each linear segment to shift them back to the ideal one, the sub-DAC error can be compensated. On the other hand, the interstage gain error is mainly due to the finite open loop gain of the opamp. The gain error changes the slope of each linear segment of the residue transfer curve, shown in Fig.2(c), (d). In the ADC transfer curve, the gain error also cause discontinuities between adjacent segments. Therefore, large gain error may result in missing codes as well. Similarly, it is straightforward to be observed that multiplying a proper number to each segment can compensate the gain error. Alternatively, adding appropriate numbers to each segment also linearizes the ADC transfer curve. Since the gain error is not corrected, the ADC appears to have an overall gain error. It is not a serious problem in many applications because the linearity of the ADC is the most concern.

## IV. Calibration Algorithm

The circuit detail of the MDAC is shown in Fig.3(a). Ideally the output is given by

$$V_{out} = V_{in}\frac{1}{\beta} + V_{ref}\frac{\sum_{j=1}^{8} m_j C_{sj}}{C_f + \sum_{j=1}^{8} C_{sj}}\frac{1}{\beta} \tag{4}$$

$$\beta = \frac{C_f}{C_f + \sum_{j=1}^{8} C_{sj}}$$

where $m_j$ is the input of the sub-DAC, it depends on the output of the sub-flash ADC according to the relationship shown in Fig.3(b).

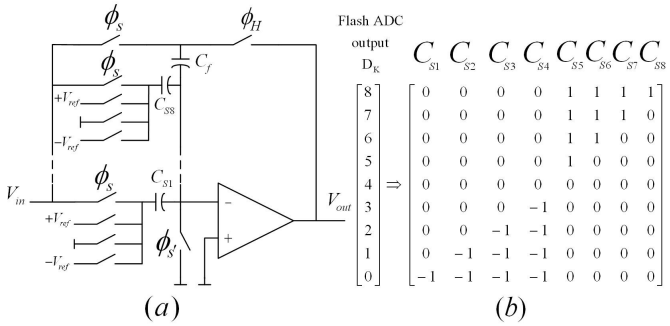


Fig. 3 Unit Capacitor MDAC. (b) DAC Configuration.

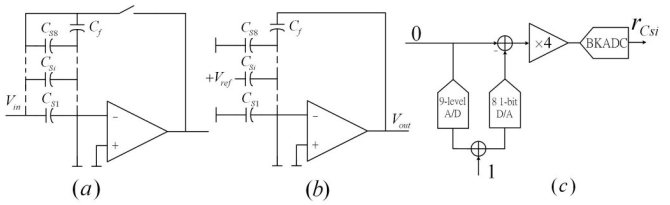


Fig. 4(a) Sampling phase. (b) Amplification phase. (c) Equivalent ADC model when doing calibration.

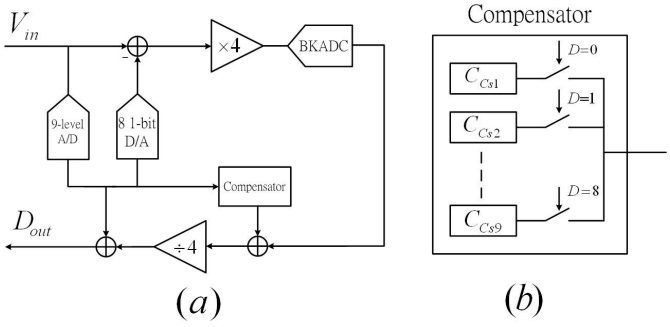


Fig. 5 Block Diagram of Calibration Circuit. (b) Details of Compensator.

To estimate the sub-DAC and gain error, as shown in Fig.4, in sampling phase, the input of the stage is connected to ground, and one of the sampling capacitors $C_{si}$ is enabled (connected to $+V_{ref}$) in the amplification phase. It is equivalent to force the input of the sub-DAC to be 1, and measuring the output of the sub-DAC by backend ADC. Note that the output of the sub-DAC is attenuated by the gain error. Therefore, the information of the gain error and single step size $\Delta_{Csi}$ due to the enabled capacitor $C_{si}$ are appeared at the output of the backend ADC, shown in Fig.4. Since $r_{csi}$ is the digital representation of the output of the MDAC, considering the finite opamp gain effect, it can be written by

$$\begin{aligned} r_{Csi} &= -G(1+\alpha_1)\cdot\Delta_{Csi} \\ \Delta_{Csi} &= V_{ref}\frac{C_{si}}{C_f + \sum_{j=1}^{8} C_{sj}} \\ G(1+\alpha_1) &= \frac{A}{1+A\beta} \end{aligned} \tag{5}$$

where A is the open loop gain of the opamp, the gain stage is modeled by $G(1+\alpha_1)$, and $\alpha_1$ is the gain error. In the absence of nonideal circuit behavior, $r_{Csi}$ is $-4\Delta$. Any deviation from the ideal value is the error arising from $C_{si}$ and the interstage gain, which is given by

$$\varepsilon_{Csi} = -4\Delta - r_{Csi} \tag{6}$$

Since the capacitor configuration of the sub-DAC varies from input to input. The 9-level sub-ADC indicates totally 9 different configurations. Therefore, there are 9 compensation values for different levels of input. The compensation value $C_{cs}$ is obtained by multiplying the matrix M in Fig.3(b) to $\varepsilon_{Cs}$.

$$C_{Cs} = M \cdot \varepsilon_{Cs} \tag{7}$$

Fig.5 shows the block diagram of the calibration circuit for the first stage. The output D[k] from the sub-flash ADC is used to determine which level the input is located in and select the corresponding $C_{csi}$ to compensate the error. For example, suppose the input is between $-4.5\Delta$ and $-3.5\Delta$, the corresponding flash ADC output is $-4\Delta$, which indicates the first level. In sub-DAC $C_{s1}$ to $C_{s4}$ are connected to $-V_{ref}$. The output of the backend ADC is given by

$$r_{DAC1} = G(1+\alpha_1)(V_{in} + \sum_{j=1}^{4}\Delta_{Csj}) \tag{8}$$

The compensation value is

$$C_{Cs1} = -\sum_{j=1}^{4}\varepsilon_{Csj} \tag{9}$$

After compensation, the digital output of the ADC is

$$\begin{aligned} D_{out} &= -4\Delta + r_1 + \frac{1}{4}(r_{DAC1} + C_{Cs1}) \\ &= V_{in}(1+\alpha_1) \end{aligned} \tag{10}$$

The above equation shows that the nonlinearity due to the sub-DAC and interstage gain error is corrected by simply adding the compensation value in (9). Furthermore, in finding the compensation value through (5)~(9), no multiplication and division is involved. In (10), since the slope of each linear segment is not changed, there is an overall gain error, which is equal to the interstage gain error. Fortunately, this linear gain error can be tolerated in many applications.

## V. Simulation Result

A behaviour model of the example pipelined ADC was built with various nonideal circuit effects. The proposed calibration was applied only in the first 3 stages. The backend stages were left uncompensated. The opamps through 1-6 stages were set to have an open loop DC gain of 50dB. A $10nV^2$rms white noise signal was added at the input of the residue amplifier to model thermal noise. The variation of the capacitors in the sub-DAC was modeled as the independent Gaussian distribution

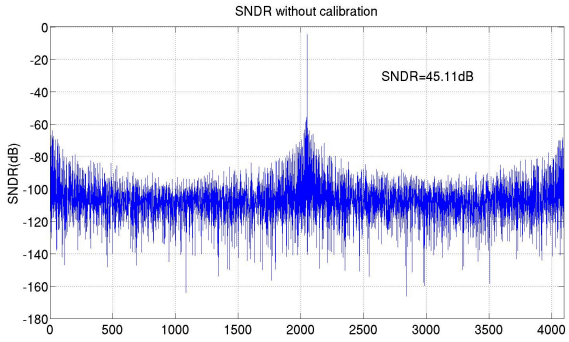


Fig. 6 Output FFT Spectrum before calibration.

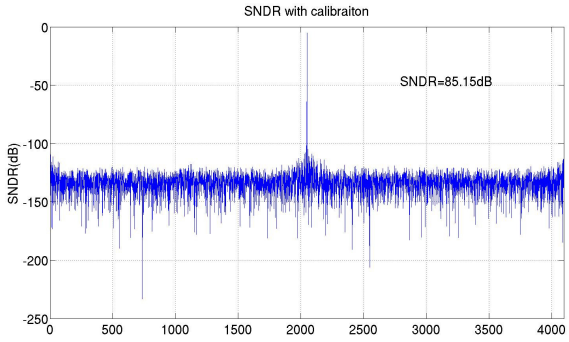


Fig. 7 Output FFT Spectrum after calibration.

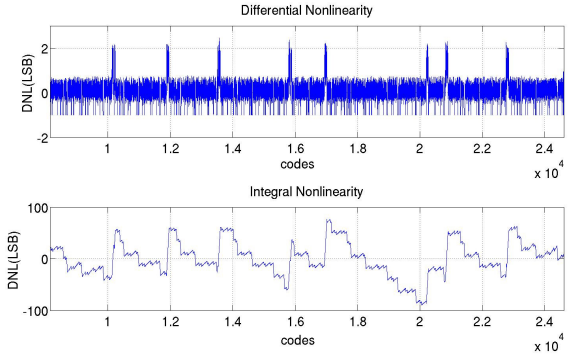


Fig. 8 DNL and INL before calibration.

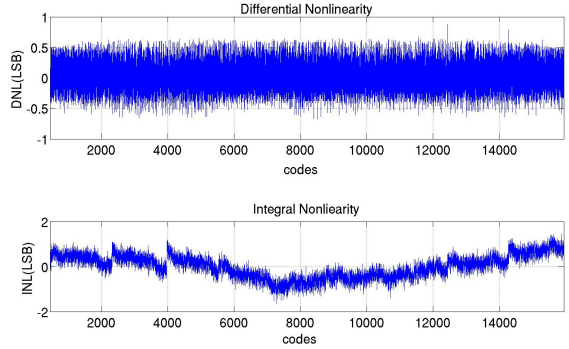


Fig. 9 DNL and INL after calibration.

with the standard deviation of 0.3%. The sub-ADC threshold errors were also modeled as the independent Gaussian distribution but with the standard deviation of 30mV. Coherent sampling is used to choose the input frequency to avoid the leakage in the FFT spectrum. Although the example ADC outputs 16-bit digital codes; the digital output is truncated to 14-bit word when simulating the differential nonlinearity (DNL) and integral nonlinearity (INL). Best fitting line method is used when testing INL.

Fig.6 shows the FFT spectrum of the output of the example ADC when the calibration is disabled, while Fig.7 shows the FFT of the ADC output when the calibration is enabled. The signal to noise and distortion ratio (SNDR) is limited below 50dB at the presence of both the interstage gain and sub-DAC error. If the interstage gain error is removed, the SNDR is limited below 65dB. Comparison of Fig.6 and Fig.7 indicates that the proposed calibration method improves the SNDR by approximately 40dB. Fig.8 and Fig.9 shows the DNL and INL plots for the example ADC without and with the calibration, respectively. Before calibration, the ADC exhibits poor linearity. At the 14-bit level, the max DNL is 2.47LSB while the max and min INL is 76.6 and -89.9LSB. There are totally 1465 missing codes. After calibration, no missing code is occurred and INL is bounded in ±2LSB. Fig.6~9 shows that significant improvements can be achieved with the proposed calibration method.

## VI. Conclusions

In this paper, a novel efficient digital calibration technique is proposed which compensates the errors arising from sub-DAC and interstage gain simultaneously. The calibration technique only employs the addition and subtraction in digital circuit, therefore the circuit complexity and power dissipation overhead are minimized. Simulation results show that the calibration technique improves the performance of the example pipelined ADC significantly.

## Acknowledgment

This work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT).

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