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NOVEL SOLUTIONS FOR ANTI-ALIASING AND ANTI-IMAGING FILTERING IN CMOS VIDEO INTERFACE SYSTEMS

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Abstract : This paper proposes novel solutions for anti-aliasing and anti-imaging filtering in video interface systems and which are based on multirate analog signal processing techniques. Various multirate switched-capacitor circuits are shown to be particularly suitable for implementing such systems and to lead to potentially more economical solutions than their digital counterparts, both with respect to power and silicon consumption.

1. Introduction

Video signal processing has become an important area of research mainly because of the rapidly expanding market of video equipment and the resulting need to produce cheaply and reliably high performance integrated circuits for such equipments. As the bulk of processing is inexorably and rapidly shifting to the digital domain, there is an increasing pressure to develop efficient circuits and systems to establish the interface between analogue and digital signals. For the interfacing from the analogue to the digital domains, such circuits usually comprise an anti-aliasing filter (AAF) followed by an analogue-digital (A/D) converter. The complementary interfacing from the digital to the analogue domains usually requires a digital-analogue (D/A) converter followed by an anti-imaging filter (AIF). Although there are alternative technologies for realising such interfacing circuits and systems [1-3] it is felt that the adoption of pure CMOS technologies is highly desirable not only to ensure full on-chip compatibility with the digital implementation of more complex signal processing functions, and thus allowing higher levels of integration, but also to save power and reduce the cost of manufacture.

It is abundantly recognised that the realisation of integrated AAF's and AIF's for video interface systems represents a rather difficult problem because of the need to provide simultaneously high precision and high speed of operation. Major efforts have been devoted worldwide to overcome the major obstacles arising in the realisation of such filters in analogue sampled-data form, and the solutions currently available range from high speed components [4] to architectures which can inherently achieve the required high precision [5]. Those architectures are basically based on traditional switched-capacitor (SC) filter structures and also employ the well known double-sampling technique [1,6] to increase the input sampling rate (in the case of the AAF), while maintaining the output sampling rate required for the digitization of the video signals. In such a solution, however, it is not possible to obtain a ratio between the sampling frequency and the maximum frequency of interest which is sufficiently high to allow reducing the order of the front-end continuous-time filter to a mere first order or even completely eliminate it. To achieve this goal it is necessary instead to adopt multirate analog signal processing techniques for designing AAF's and AIF's whose ratio between the input and output sampling frequency, respectively, and the maximum frequency of interest can be made very high.

In the first part of this paper we shall review the more traditional digital video interface systems and describe an alternative mixed signal analog/digital architecture based on multirate analog signal processing techniques. Then, in the second part, we shall present various circuit solutions which can be efficiently employed in such architectures.

2. Video Digital Systems

Video Codification Principles: Video images unlike those on printed paper, consist of light generated by the screen, rather than being reflected from a light source. For proper color image reproduction, a color is usually divided in the three basic HSB components, namely Hue, Saturation, and Brightness. The brightness portion of the image is the luminance signal (Y), and the combined hue and saturation information of the image gives the chrominance signal (C) which is comprises the signals C_R and C_B. On the other hand, the trio of colors generally accepted for standard video codification is composed by Red, Green, and Blue (RGB). Video coders are employed to convert the RGB type of signals into HSB signals [2], whereas video decoders perform the complementary function [3].

Standard Video Digital Interface System: New image services currently use digital coding and decoding of the video signals [2,3]. The general architecture of a standard video digital system, according to the CCITT [7], is presented in Fig.1. Due to the complex video signal characteristics the three equivalent coding paths, showed in the digital coder of Fig.1-a, need high amplitude selectivity and very stringent linear phase specifications. In typical coders all the burden is placed on fast A/D converters and on extremelly complex lowpass digital decimators [2], to simplify the realisation of the AAF. Recent implementations of the digital decimator alone at very high frequency required a large silicon area ($22mm^2$) and power consumption (2W) [8]. On the other hand, for the digital decoder presented in Fig.1-b the most difficult problems are mainly related to the complexity of the luminance filter. This is essentially due to the fact that in order to maintain compatibility with the monochrome standard [7], the luminance information of the image must be transmitted in roughly the same method independent of the chromination information. Since even obsolete monochrome receivers must be abble to reconstruct a satisfactory monochrome image from the color signal, the color signal must occupy the same bandwidth as the previous monochrome signal. That implies for the luminance filter a very high order and linear phase response [9]. Finally, since the chrominance filters are also complex and the D/A converters operate at the higher sampling frequency, this yields large silicon and power consumption.

3. Analog/Digital Video Interface System

Basic Principle: Since the adoption of traditional or even advanced analog techniques [9] do not solve the main problems encountered in the above digital system, a new architecture philosophy must be explored employing multirate analog signal processing techniques recently developped [10,11]. This led to the development of new multirate SC filtering circuits which operate with a multi-phase arrangement of switching waveforms instead of the traditional bi-phase. Traditional SC filters can also be employed in multirate signal processing systems, but it is usually desirable to design specialised multirate SC circuits which can take advantage of the processes of sampling rate reduction and sampling rate increase in order to reduce the speed requirements of the amplifiers [10, 11].

Multirate SC Circuits: Such specialised multirate SC circuits are known as decimators and interpolators, respectively for reducing and increasing the sampling rate, and their filtering functions are tailored to reject the unwanted alias and image frequency components associated with the signals sampled at the lower rate. FIR SC decimators [10,12] are particularly suitable for applications requiring multinotch stopband approximations and linear phase, as is the case of the three coding paths of the video coder presented above. IIR SC decimators [11,13] are more adequate for applications requiring wide stopband approximations, which implies that they can also be useful in the video coder but only if cascaded with appropriate equalizer circuits. IIR SC interpolators [14], on the other hand, can be extremelly useful in the decoding paths of the video decoder due to the selectivity needed for both the luminance and chrominance filters.

Analog Digital Interface Architecture: An alternative system architecture is proposed in Fig.2, which employs the type of multirate SC circuits described above. Such an architecture possesses some basic ideas that can simplify the video coder/decoder system, namely the relaxation of the speed requirements of the A/D and D/A converters, the simplicity or even the elimination of the digital filtering, and also the reduction of the complexity of the front-end continuous-time filters. The coder presented in Fig.2-a suggests that the speed of operation of the A/D converter can be reduced by a factor of M while eliminating the digital filtering. As mentioned above, both FIR and IIR SC decimators can be employed in the coding paths although FIR decimators may be preferable due to their linear phase response. In Fig.2-b, the proposed decoder architecture essentially differs from the digital one due to the change in the place of the D/A converter, which implies the use of an Analog Matrix Operator to convert HSB signals into RGB signals [9]. Also in this case, the D/A can be simplified in order to operate at a lower sampling rate while maintaining the simplicity of the AIF. The SC interpolators in this case should have IIR discrete-time transfer functions due to the selectivity required in both the luminance and chrominance paths. They must also be cascaded with proper equalizers in order to obtain linear phase responses.

4. Examples of Multirate Video SC Circuits

FIR SC Decimator: Fig.3 shows an example of an FIR SC decimator adequate for the video coder [12], with impulse response length of N=19 and whose input and output sampling frequencies are, respectively, $5F_S$=67.5MHz and F_S=13.5MHz. Such circuit is based on the ADB1 polyphase architecture where five polyphase filters are realised using four common blocks [10]. The sign of the impulse response coefficients defines the type of SC branch to be employed at the input of the four common blocks. The capacitance values of the input SC branches, on the other hand, are obtained from the magnitude impulse response coefficients. The resulting nominal computer simulated amplitude response is presented in Fig.4. The speed of the operational amplifiers is limited by the lower output sampling frequency at 13.5MHz thus yielding an important reduction of the power consumption when compared with traditional SC filters [10, 12].

IIR SC Decimator: Fig.5 shows a 5th. order elliptic lowpass IIR SC decimator [13] which may also be adequate for the video coder and whose input and output sampling frequencies are, respectively, $3F_S$=40.5MHz and F_S=13.5MHz. The amplitude response is tailored to obtain a passband ripple of 0.2dB, cut-off frequency of f_C=3.6MHz, and minimum 35dB rejection above 4.44MHz. The circuit is based on an N-th order building block architecture [13] and is implemented using a low selectivity input polyphase network together with a high selectivity recursive network. The resulting computer simulated amplitude response is presented in Fig.6. The speed of the operational amplifiers is also limited by the lower output sampling frequency at 13.5MHz.

IIR SC Interpolator: Fig.7 shows a 3rd. order Tchebyshev lowpass IIR SC interpolator appropriate for part of the video decoder chrominance interpolator indicated in Fig.2 [14]. The amplitude response possesses a passband ripple of 0.1dB and cut-off frequency f_C=2MHz, and the input and output sampling frequencies are, respectively, F_S=7.5MHz and $2F_S$=15MHz. Such circuit is based on the N-th order building block architecture presented in [14] and employs an active output multiplexer realised using a unity-gain buffer with a multiphase switching arrangement. The resulting computer simulated amplitude response is presented in Fig.8. The speed of the operational amplifiers is limited by the lower input sampling frequency at 7.5MHz).

Although the above examples of multirate SC circuits require more complex digital waveform generators than traditional SC filters [15] they may lead to considerable gains in the analogue circuitry, as well as in the resulting digital circuitry associated in the video system, namely with respect to the silicon area and power consumption.

5. Conclusions

Based on the principles of multirate analog signal processing techniques, this paper described alternative solutions for anti-aliasing and anti-imaging filtering in video interface systems which can be made highly competitive with respect to functionally equivalent digital architectures. Some examples of multirate switched-capacitor circuits were considered to illustrate the implementation of the proposed architecture, and which can efficiently reduce silicon and power consumption.

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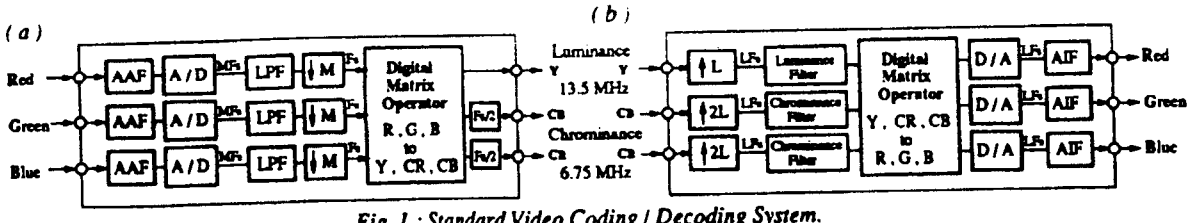


Fig. 1 : Standard Video Coding / Decoding System.
(a) Digital Coder. (b) Digital Decoder.

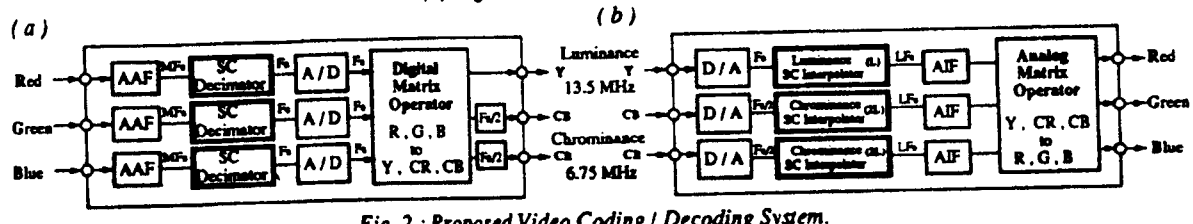


Fig. 2 : Proposed Video Coding / Decoding System.
(a) Mixed Analog/Digital Coder.
(b) Mixed Analog/Digital Decoder.

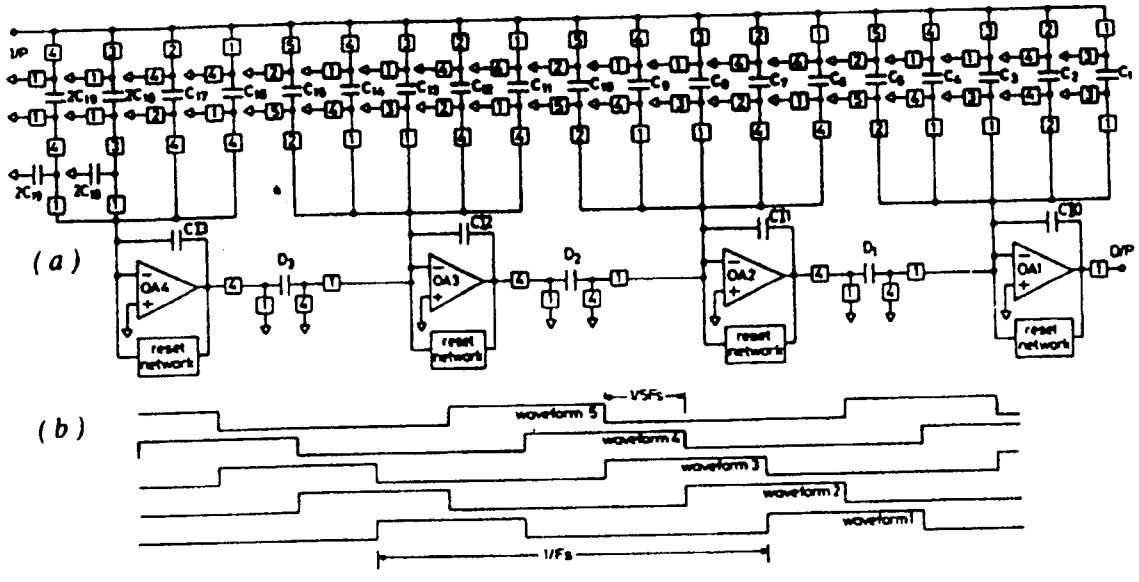


Fig. 3 : FIR SC decimator with sampling rate reduction from 67.5MHz to13.5MHz and N=19, for anti-aliasing filtering in CMOS Video Coders. (a) Circuit. (b) Switching waveforms.

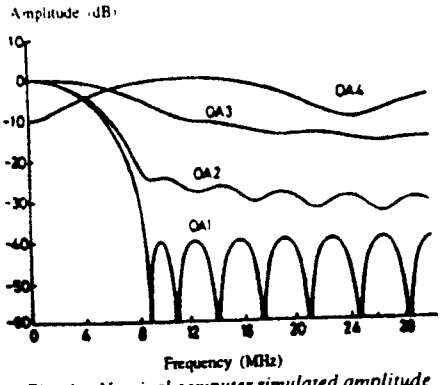


Fig. 4 : Nominal computer simulated amplitude response of the circuit in Fig.3.

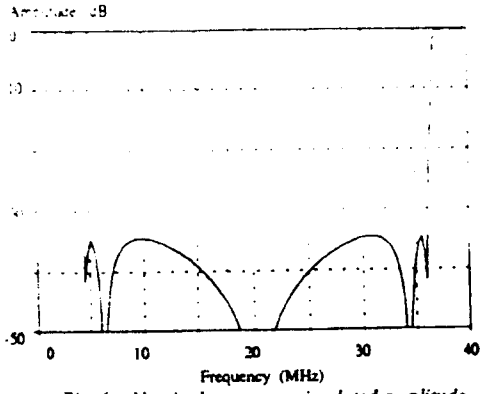


Fig. 6 : Nominal computer simulated amplitude response of the circuit in Fig.5.

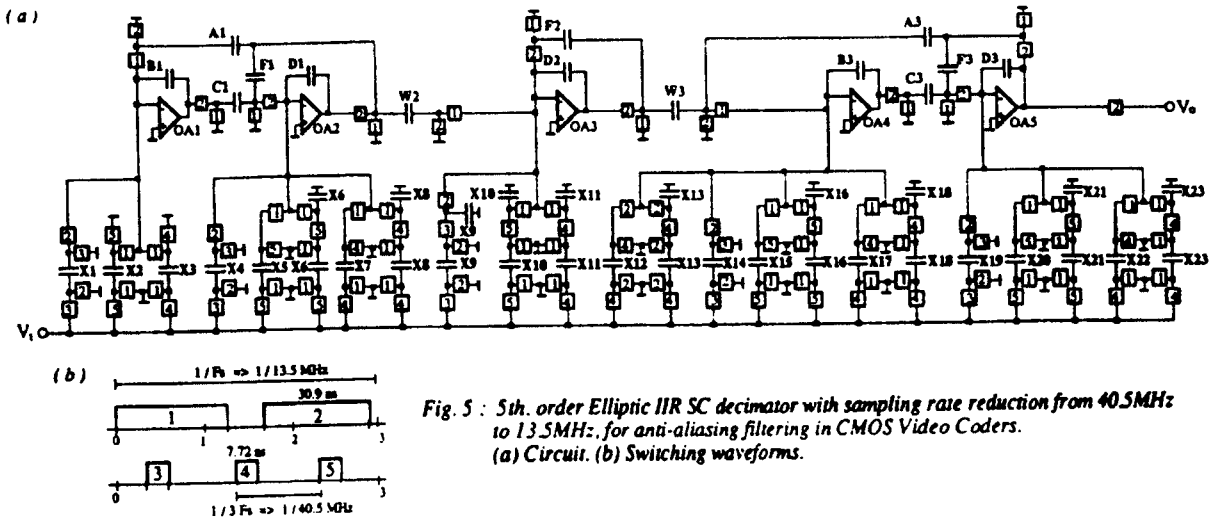
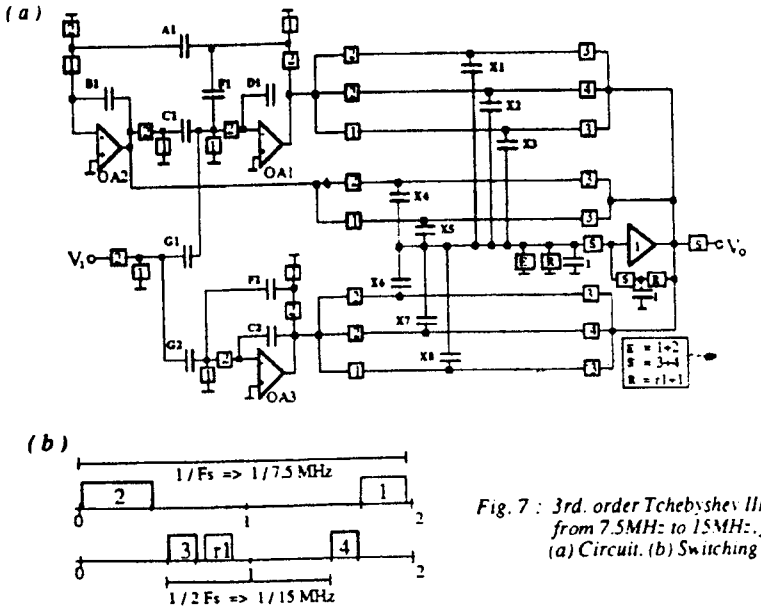


Fig. 5 : 5th. order Elliptic IIR SC decimator with sampling rate reduction from 40.5MHz to 13.5MHz, for anti-aliasing filtering in CMOS Video Coders. (a) Circuit. (b) Switching waveforms.



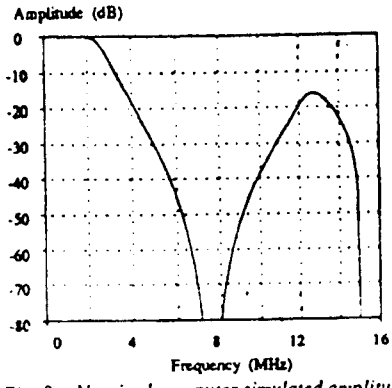


Fig. 8 : Nominal computer simulated amplitude response of the circuit in Fig.7.

Fig. 7 : 3rd. order Tchebyshev IIR SC interpolator with sampling rate increase from 7.5MHz to 15MHz, for anti-imaging filtering in CMOS Video Decoders. (a) Circuit. (b) Switching waveforms.