An 11b 60MS/s 2.1mW Two-Step Time-Interleaved SAR-ADC with Reused S&H

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***Abstract*—An 11b 60MS/s 2-channel two-step SAR ADC in 65nm CMOS is presented. The scheme shares the op-amp between channels for the residual generation and takes advantage of time interleaving for reusing the input S&H of the first stage. A reduction of the gain in the residual generator and sub-threshold operation enables the use of a power-effective, single-stage op-amp with 69dB-gain. The ADC achieves peak SNDR of 57.6dB while consuming 2.1mW from 1-V analog and 0.85-V digital supply, resulting in an FoM of 57fJ/step.**

I. Introduction

The technology scaling favors the design of ultra power efficient, moderate resolution and high-speed successive approximation register (SAR) ADCs [1]-[3]. The power effectiveness of traditional pipelined or two-step ADCs drops for 10+ bit and 50-100 MS/s specifications because of the power required by the op-amp(s). The problem becomes more evident with nanometer CMOS technologies because high-gain op-amps are difficult to design. However, high resolution and high-speed need amplification, and consequently, the use of op-amps become unavoidable. Published results show that with low or medium resolution (less than 10-bit) the SAR architecture obtains excellent figures of merit with conversion speeds around 50MS/s. However, when the resolution goes above 10-bit and the speed is several tens of MHz the power performances drop sharply, even because of the power needed by the reference voltage generator. Accordingly, sustaining the figure of merit at state-of-the-art levels become problematic.

This work addresses the problem of obtaining power effectiveness in the 10+ bit and 50+ MS/s regions. The used solution obtains the conversion in two-steps but uses 6-bit SARs instead than flash schemes because the SAR is much more power effective. The interstage gain is 8. Therefore, the

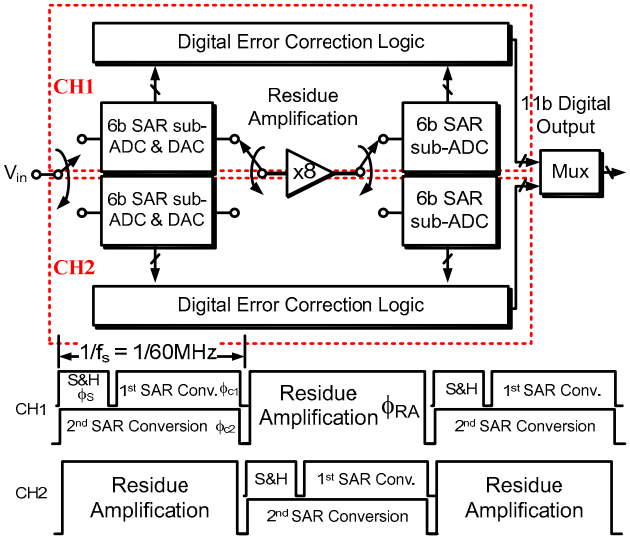

Fig. 1. The overall ADC architecture and timing diagram.

obtained low swing of the residual generator enables using a telescopic gain-boosted cascode, shared between time-interleaved paths. The digital error correction relaxes the 1st SAR requirements. All the above mentioned methods permit us to obtain a very low FoM, making the proposed scheme a valid and power effective alternative to single-step dynamic SAR ADC whose optimal region of operation is in the lower resolution and higher speed range.

II. The Proposed ADC Architecture

Fig. 1 shows the overall 11b 60MS/s ADC architecture that uses two interleaved two-step SAR ADCs sharing the same residue amplifier. The 1st stage converts the coarse 6b

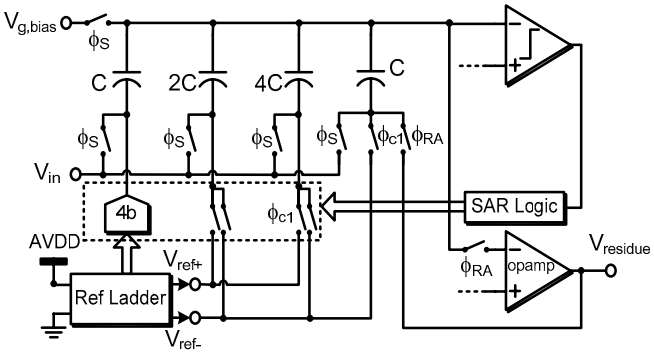

Fig. 2. The 1st-stage SAR followed with 8x residue amplification.

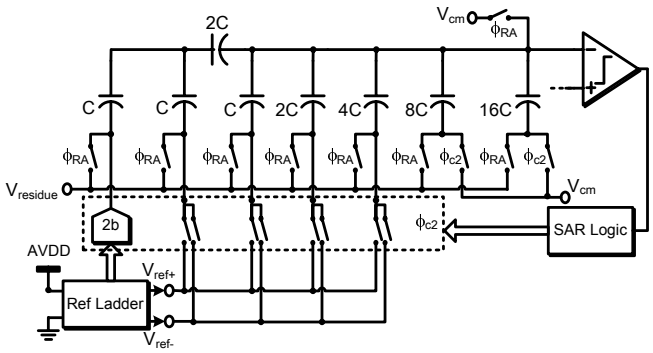

Fig. 3. The 2nd-stage SAR sub-ADC.

codes and generates the residue, which is amplified by 8 and it is passed to the 2nd SAR sub-ADC which converts 6b fine codes. The digital correction logic uses coarse and fine codes to obtain 11b. The $V_{ref} = \pm 500mV$ is generated by an on-chip reference ladder. Fig. 1 also shows timing diagram and clock phases.

The gain of the residue amplifier should be normally 32 to comply with the 6b of the 1st stage. However, the low feedback factor would lead to expensive requirement of high DC open loop gain and high op-amp's GBW. Moreover, high output swing in the op-amp would constrain the low-voltage op-amp architecture. A suitable trade-off is to use a gain of 8, which leads to an affordable request of 2nd-stage accuracy equal to 8b. The benefit is that the op-amp gain, the speed and swing requirements are all relaxed with respect to what the 32x amplification needs.

Fig. 2 shows the block diagram of the 1st 6b stage and the residue generator. An array of 8 unity capacitors and a 4b resistive ladder make the 6b DAC. A process-tracked biasing network generates $V_{g,bias}$ for setting the proper value of the input common-mode voltage. The DAC array is pre-charged (with bootstrapped switches) to the input signal during ϕ_S (specified in the timing of Fig. 1). Then, a 6b self-timing SAR converter works during the remaining time-slot ϕ_{C1}. At the end of the conversion the residue charge remains on the top-plate of the DAC array. That charge is integrated on a unity capacitance of the array that operates as a flip-around element for obtaining the 8x residual generation during ϕ_{RA}. The scheme shares the operational amplifier between the two time-interleaved paths. The time-interleaving enables a double use of the capacitive array: to perform the input sampling and the generation of the residual. Therefore, the signal sampled for coarse conversion is reused for the residual generation. This feature reduces the input capacitive load and avoids error caused by clock misalignment in sampling the input for the coarse and the fine conversions. Moreover, the use of time-interleave reduces the operating frequency in each path, but the path mismatches including offset, gain and timing will create problems. For improving performances, the S/H reuse allows the use of bigger unity capacitances that improve the matching.

The fine SAR conversion with self-timing operation occurs in a pipeline fashion while the first stage starts a new cycle. Fig. 3 shows the architecture of the 2nd stage sub-ADC. It is composed by a 4b capacitive and a 2b resistive array. The capacitors 8C and 16C are not part of the sub-ADC but perform a scaling by 4 of the references (±125mV) as required by the lower interstage gain, which is 8 and not 32. The used solution enables the utilization in the fine-bit DAC reference voltages that are equal to the one employed in the coarse-bit DAC.

A master clock of 60MHz generates various matched interleaved clock phases through a divider-by-2 low-skew clock generator. The self-timed SAR logic avoids the need of external fast master clock. All SAR loop utilized dynamic logics to enable high speed processing, with trade-offs of possible leakages that degrade the digital logic performance at low sampling frequencies.

The use of digital error correction relaxes the accuracy of the 1st stage sub-ADC decisions (including the ones related to the comparator offset, the noise and incomplete DAC settlings during the SAR's bit-cycling) from 11b to only 7b (7.8mV). Indeed, the 1st-stage operation is required to settle within the needed accuracy only at the end of the residue amplification phase. The time allocated for this phase is almost half of the clock period and the output voltage is within ±125mV; therefore, time-constant of the 1st stage ladder and specifications of the op-amp are not problematic.

The 1st-stage comparator calibrates the offset through an unbalanced capacitive loading technique [4]. Since the offset auto-zeroing for the op-amp would require an additional clock phase, the design obtains a 3σ offset of 4.5mV by using a large input differential pair operating in the sub-threshold region. The 2nd stage comparator offset is cancelled in the digital domain by interleavely subtracting the mean code.

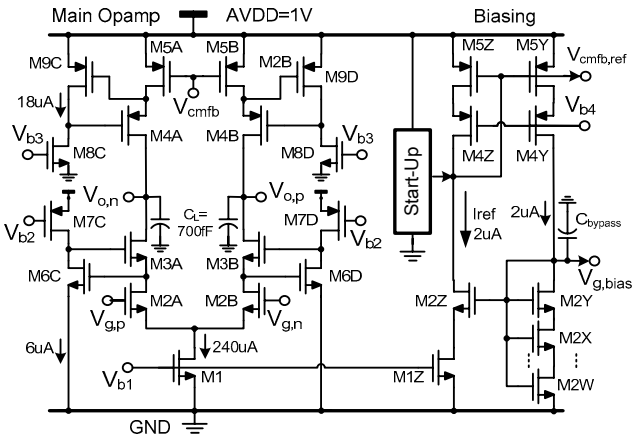

Fig. 4. Circuit schematic of the telescopic gain-boosting op-amp.

III. The Sub-threshold Opamp

Fig. 4 shows the circuit schematic of the single-stage op-amp along with its biasing circuit able to track process variations. The bias network also generates $V_{g,bias}$ for the proper setting the op-amp input common-mode. The start-up circuit ensures non-zero current in the bias network. Conventional op-amps designed in low-voltage nanometer CMOS technologies need to use two-stage architectures. This work, thanks to the reduced output swing, can use a telescopic configuration with a gain-boosting technique that enhances the gain. The used currents keep transistors in the sub-threshold, thus minimizing overheads and making possible a 1-V supply. Thanks to sub-threshold conditions, the V_{GS} of transistors M9C can be set quite close to the overdrive voltage V_{OD} of M5A. This feature, made possible by the sub-threshold operation and a nanometer technology, does not increase the headroom needed by the gain-boosted telescopic op-amp which was the case in older technology node. Since the op-amp gain is in the order of $(g_m r_o)^3$, the transistor lengths can be reduced significantly to alleviate the large aspect-ratio requirements of the sub-threshold transistors. The gain-boosting branches consume 48µA (that is 16% of 300µA the total current of the op-amp). The op-amp achieves 69dB gain, 440MHz GBW and 88° phase margin with β=1/8 with the use of standard-V_T transistors.

IV. Measurement Results

The prototype ADC was implemented in a 65nm standard CMOS process. Fig. 5 shows the die photograph whose core area is 0.21mm^2. The ADC has a full-scale input range of 1V_{pp} differential. Fig. 6 reports the static linearity. The DNL and INL are 0.39/-0.34 LSB and 1.4/-1.3 LSB, respectively, showing the expected 11b performance at low frequency. However, similarly to already published experimental results, dynamic limitations cause harmonic components as shown in the output spectrum of Fig. 7. The measured FFT plot with

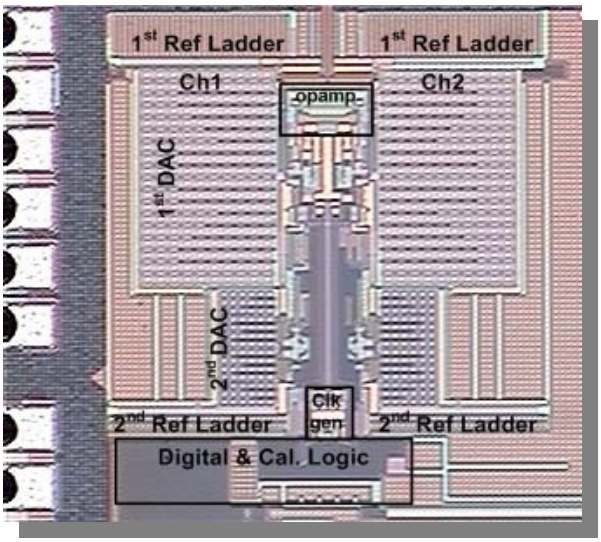

Fig. 5: Chip micrograph.

2.3MHz input and 60MHz sampling frequency indicates SNDR/SFDR/THD equal to 57.6/63/-61dB, respectively. As illustrated in Fig. 8, inputs in the 2-10MHz range show an SNDR of about 57dB. The SNDR drops at low f_s (Fig. 9) because of the leakage in the dynamic SAR logic. The expected limit is irrelevant because this design is for f_s > 50 MHz. The power consumption is 2.1mW with 1-V analog and 0.85-V digital supply. The analog power, including reference ladders (1.3mW), op-amp (300µW), and comparators (100µW), is 1.7mW. The digital consumed power is 0.4mW. The performance comparison of the ADC to the state-of-the-art designs is given in Table I.

V. Conclusions

This 11b 60MS/s time-interleaved two-step SAR ADC proposes and demonstrates various methods for achieving the specifications with very low power. Sub-threshold operation and a reduced output swing allow an effective design of the needed high-gain low-power op-amp. The design achieved a significant FoM of 57fJ/conv, comparable to state-of-the art fully-dynamic SAR ADCs.

Acknowledgment

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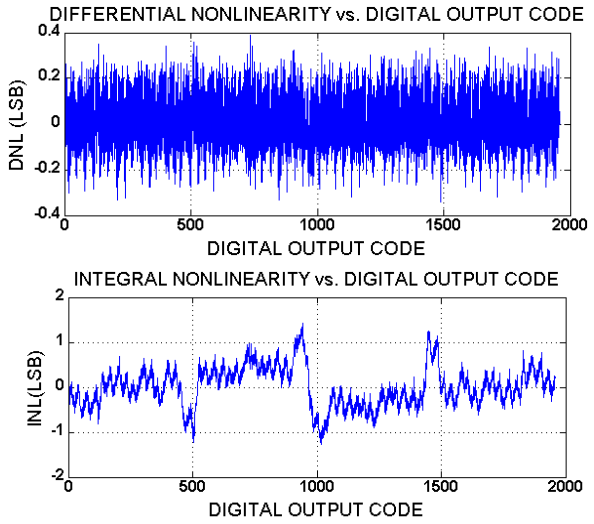

Fig. 6. Measured DNL and INL of the ADC.

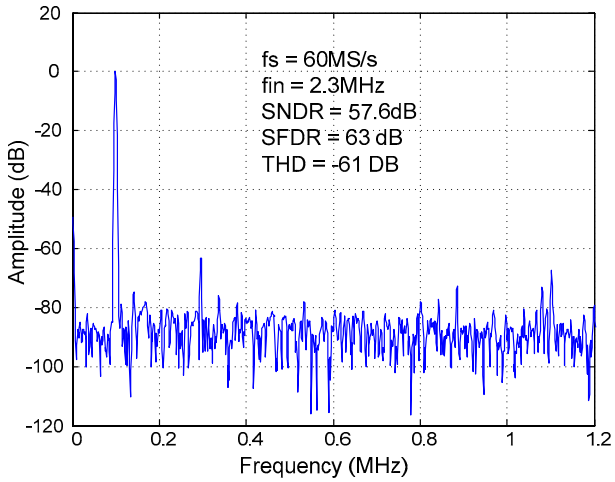

Fig. 7. Measured output spectrum of the ADC with f_s = 60MS/s (Output decimated by 25)

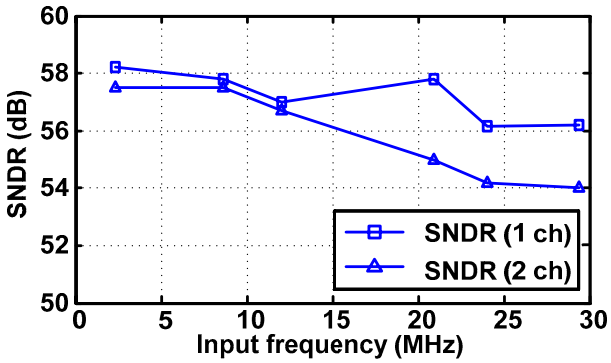

Fig. 8. SNDR vs. the input frequency.

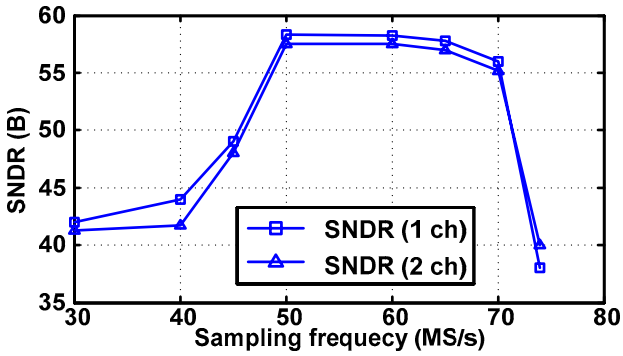

Fig. 9. SNDR vs. the sampling frequency.

TABLE I: Comparison to the state-of-the-art ADCs.

	[1] VLSI'09	[2] ISSCC'10	[3] JSSC'10	[5] ESSCIRC'09	[6] ISSCC'09	This Work
CMOS Technology	0.13 µm	65nm	65nm	65nm	90nm	65nm
Architecture	SAR	SAR	SAR	Algorithmic	Pipelined	TI-Two-Step
Opamp use	No	No	No	Yes	Zero-Crossing-Based	Yes
Resolution	10b	10b	10b	11b	12b	11b
Sampling Rate	50MS/s	50MS/s	100MS/s	20MS/s	50MS/s	60MS/s
Power	920µW	820µW	3mW	2.85mW	4.5mW	2.1mW
DNL (LSB)	0.88/-1	0.7	0.79/-0.27	0.37/-0.32	0.68/-0.4	0.39/-0.34
INL (LSB)	2.2/-2.1	0.82	0.86/-0.78	0.72/-0.64	2.7/-2.7	1.4/-1.3
SNDR	52.8 dB	56.9dB	56.6dB	60.4dB	62dB	57.6dB
ENOB	8.5	9.2	9.1	9.7	10	9.3
FoM (P/[2^{ENOB}*fs])	52fJ/step	30fJ/step	55fJ/step	167fJ/step	88fJ/step	57fJ/step