Parasitics Nonlinearity Cancellation Technique for Split DAC Architecture by Using Capacitive Charge-Pump

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***Abstract*— A voltage feedback charge-cancellation technique is proposed which prevents the conversion nonlinearity due to the parasitic effect of split DAC architecture in Successive Approximation Register (SAR) ADCs. A voltage feedback network operating as a capacitive charge-pump can efficiently detect and compensate the voltage error in each bit cycling, thus the conversion accuracy can be significantly improved. A 10b 80MS/s SAR ADC was demonstrated in 65nm CMOS technology. Simulation results show that the proposed charge-cancellation technique can improve the Effective Number of Bits (ENOB) from 8.5b to 9.6b and decrease the maximum DNL and INL from 3LSB to 0.5LSB and 1.65LSB to 0.74LSB, respectively, with only 100 µW power dissipation.**

I. Introduction

The split architecture of the DAC array became popular since it constitutes a very good alternative to the binary-weighted structure [1], especially for high-speed and medium-to-high resolution SAR ADCs because the binary-scaled array capacitance rises exponentially with the resolution, leading to a larger consumption of switching energy and settling time. However, since the split architecture suffers from the parasitic nonlinearity effect [2] it would be impossible its utilization in high-resolution applications.

The parasitic capacitance can be reduced by using additional layers to form metal-insulator-metal (MIM) capacitors [3]; however such additional layers will increase fabrication costs as MIM capacitors are rarely available in process options used in industry. Some digital calibration techniques [4][5] proposed recently can relax the parasitic nonlinearity effect by adjusting the size of the attenuation capacitor, as well as of an additional capacitive array in the DAC's internal node. But, in practice, the parasitic calibration requires also the comparator's offset voltage calibration within 1LSB, which is unnecessary in conventional single channel SAR ADCs and increases the difficulties for high-resolution implementation.

This paper presents a charge domain cancellation technique that significantly improves the conversion linearity by compensating the charge stolen by the parasitic capacitors. A voltage feedback network implemented by using the capacitive charge-pump is proposed which is robust to the process variation and allows very low power dissipation. The idea was implemented in a 10b 80MS/s SAR ADCs with 1-V supply voltage in 65nm CMOS technology. Considering 10% top-parasitic in each unit capacitor the Signal-to-Noise-and-Distortion Ratio (SNDR) can be improved from 53dB to 59.5dB and the maximum DNL and INL reduced from 3LSB to 0.5LSB and 1.65LSB to 0.74LSB, respectively. The total power consumption of the proposed calibration circuit is only 100µW which demonstrates the feasibility of the proposed structure.

II. Charge Compensation Technique

A. Parasitic nonlinearity effect in the split structure

The architecture of the n-bit SAR ADC is shown in Fig.1, consisting of a split capacitive DAC array, a comparator and SA control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. A split capacitive DAC array is primarily selected for its advantages of smaller array capacitance, fast DAC settling and power saving. The attenuation capacitor C_{atten} is used to separate the DAC into j-bit MSB and i-bit LSB binary-scaled sub-arrays. When compared with the binary-weighted structure, the MSB capacitor and the equivalent output capacitance can be reduced from $2^{n-1}C_0$ and 2^nC_0 to $2^{j-1}C_0$ and 2^jC_0, respectively, with C_0 being the DAC array unit capacitance.

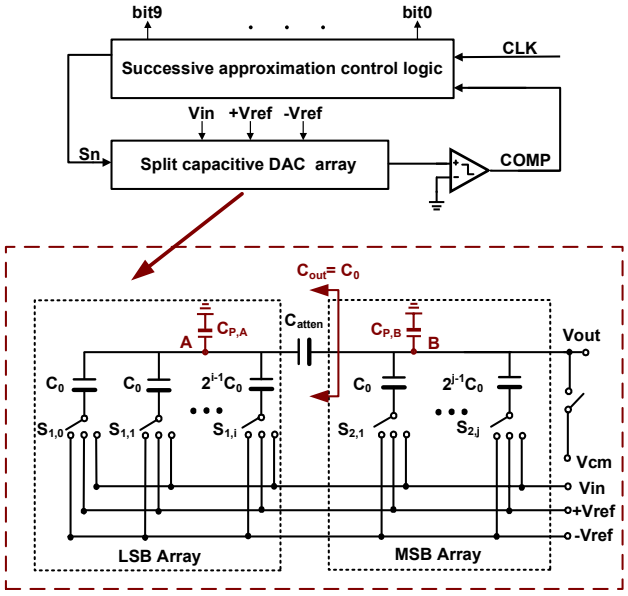

Fig.1. Overall SAR ADC architecture and the n-bit split DAC structure. (n=i+j).

One potential issue of the split architecture is its vulnerability to the parasitic effect [2], as illustrated in Fig.1, where the parasitic capacitance $C_{P,B}$ and $C_{P,A}$ on the nodes B and A are introduced by the bottom- and top-plate parasitic capacitance of C_{atten} as well as the top-plate parasitic capacitance of MSB and LSB array capacitors, and can be expressed as,

$$C_{P,B} = \alpha \cdot C_{atten} + \beta \cdot C_{Sum,MSB} \quad (1)$$

$$C_{P,A} = \beta \cdot C_{atten} + \beta \cdot C_{Sum,LSB} \quad (2)$$

where $C_{sum,MSB}$ and $C_{sum,LSB}$ are the total capacitance of the MSB and LSB arrays, and α, β represent the percentage of bottom- and top-plate parasitic capacitance of each capacitor, respectively. The analog output V_{out}, considering $C_{P,A}$ and $C_{P,B}$, can be calculated as

$$V_{out} = \frac{C_{atten}\left(\sum_{n=1}^{i} S_{1,n} 2^{n-1} C_0 + \sum_{n=1}^{j} S_{2,n} 2^{n-1} C_0\right) + \left(C_{Sum,LSB} + C_{P,A}\right) \sum_{n=1}^{j} S_{2,n} 2^{n-1} C_0}{C_{atten}\left(C_{Sum,LSB} + C_{Sum,MSB} + C_{P,B} + C_{P,A}\right) + \left(C_{Sum,LSB} + C_{P,A}\right)\left(C_{Sum,MSB} + C_{P,B}\right)} V_{ref} \quad (3)$$

where S_n equal to 1 or 0 is the ADC decision for bit n. As this equation shows the parasitic capacitance $C_{P,A}$ and $C_{P,B}$ in the denominator are completely uncorrelated in the bit decisions, then they will only cause a gain error and will not affect the linearity performance. However, the parasitic capacitance $C_{P,A}$ in the numerator contributes with code-dependent errors, which degrade the conversion linearity. A behavioral simulation of a 10-bit SAR ADC is presented in Fig.2, which illustrates the conversion sensitivity to the variation of $C_{P,A}$. From there it can be deducted that, if β varies within 5% good conversion linearity can still be ensured, but if β increases larger than 10%, the SNDR drops significantly. Typically, it happens after the layout routing when metal-oxide-metal (MOM) plate or fringe capacitors are used.

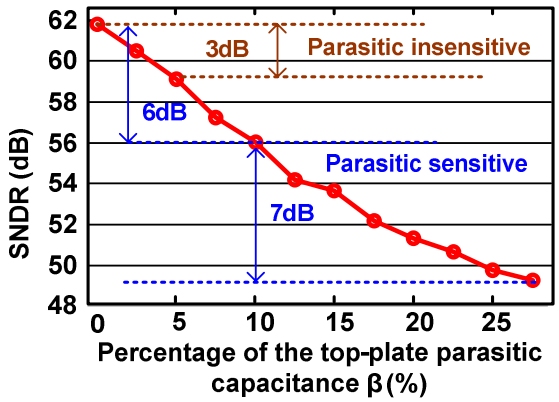

Fig. 2. Behavioral simulation of SNDR versus the percentage of the top-plate parasitic capacitance β.

B. *Feedback charge-cancellation*

The parasitic $C_{P,A}$ in the internal node A can be compensated by using the proposed charge-cancellation technique, which is demonstrated with a two bit capacitive DAC example, as shown in Fig.3(a). Initially, at the instant of time 0, all the array capacitors are reset to ground, producing a 0V at the DAC's output $V_{out}[0]$. Then, in Fig.3(b), the MSB capacitor is switched to a reference voltage V_{ref} and others are kept connected to ground. Ideally, the output of the DAC is 1/2 V_{ref}, but when the parasitic capacitance $C_{P,A}$ is

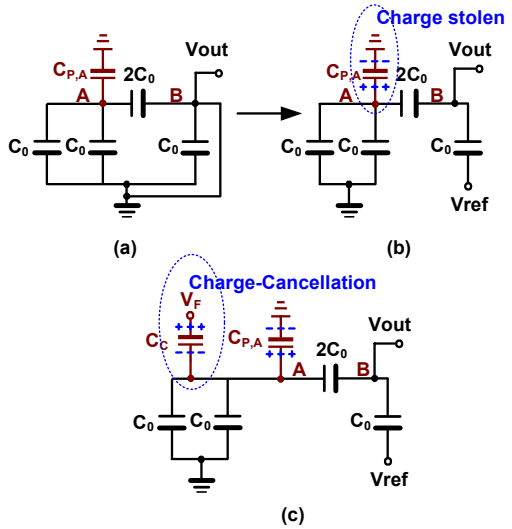

Fig.3. (a) Reset DAC array. (b) MSB transition.(c) Charge-cancellation can be achieved in node A when C_c is added.

included, a voltage error exists at the output $V_{out}[1]$ after the first bit transition. According to the charge conservation principle, $V_{out}[1]$ can be calculated as

$$V_{out}[1] = \frac{4C_0 + C_{P,A}}{8C_0 + 3C_{P,A}} V_{ref} \quad (4)$$

subtracting (4) from its nominal value, and the voltage error will become

$$V_{err} = \frac{C_{P,A}}{16C_0 + 6C_{P,A}} V_{ref}. \quad (5)$$

The V_{err} happening from (5) is caused by the charge stolen by $C_{P,A}$ at node A which can be represented as $(V_A[1]\text{-}V_A[0])C_{P,A}$. Theoretically, as shown in Fig.3(c), when a compensation capacitor C_c is applied to node A, with a feedback voltage V_F (V_F=k($V_A[1]$-$V_A[0]$), where k is the amplification factor that satisfied the following relationship:

$$(1-k)(V_A[1]-V_A[0])C_C + (V_A[1]-V_A[0])C_{P,A} = 0 \quad (k>1) \quad (6)$$

then, charge-cancellation in $C_{P,A}$ can be achieved. Qualitatively, (6) means that the charge injected from C_c is identical to that in $C_{P,A}$ but with the opposite polarity, as a result the voltage error at the DAC's output can be corrected.

Following the conceptual illustration above, a voltage feedback network is required to track and amplify the node voltage V_A after each bit transition and returning the result at the summing node of A. The amplification factor k relies on the capacitance of the compensation capacitor C_c, as defined in (6) to adopt the charge cancelling. The flexibility of the amplification factor k relaxes the design effort and it can be easily achieved through a capacitive charge-pump network, which will be discussed next.

III. Circuit Implementation

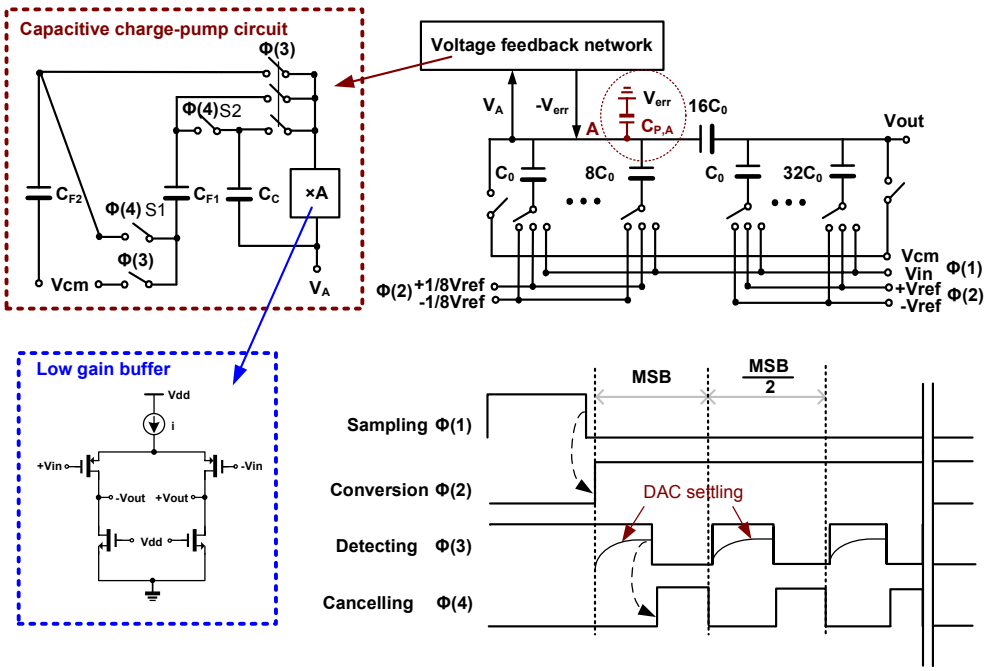

Fig.4. The split DAC array with proposed voltage feedback network.

According to the previous analysis the parasitic nonlinearity effect in the split DAC architecture can be suppressed by its internal node charge cancellation, thus a voltage feedback loop is required to track and amplify the node signal in each bit cycling. Here, we propose a charge-cancellation technique inspired in the use of capacitive charge-pump, to achieve the feedback voltage amplification. The charge domain feedback compensation is implemented in a 10 bit split DAC array, as shown in Fig.4, a voltage feedback network is placed in the DAC's internal node A, which comprises a low-gain buffer and a capacitive charge-pump circuit. The differential pair is selected to sense the error voltage for the feedback network. The differential input which connects to the output of the DAC will sample the internal node error voltage V_A to its output feedback capacitive network C_{F1}, C_{F2} and C_c. After the sampling, the capacitive network operates as capacitive charge pump to attain kV_A (k equals to $(A(C_{F1}+C_{F2})/C_{F1})$ at the top-plate of the C_{F1} to perform the charge-cancellation with the $C_{P,A}$. The differential pair functions as a low-gain buffer and the large feedback voltage succeeds in the voltage addition of C_{F1} and C_{F2}, which samples the V_A synchronously and then connects it in series. Consequently, the power dissipation for the voltage feedback loop can be minimized. To reduce the voltage swing in node A, which may degrade the linearity of the low gain buffer, a value of C_{atten} identical to $16C_0$ is used leading to a division by 8 of the LSB array reference voltage.

The switching timing diagram is also presented in Fig.4, in the sampling phase, the capacitors C_{F1}, C_{F2} and C_c in the feedback network are all reset to V_{cm} by the low-gain buffer. No initial charges are stored on feedback capacitors, thus V_{in} is successfully sampled onto the DAC array. The conventional conversion phase is divided into two clock phases: in V_A , detecting phase Φ3 and charge-cancellation phase Φ4. In Φ3, the DAC performs the charge-redistribution switching method that charges the MSB capacitor to $+V_{ref}$ and others to $-V_{ref}$, appearing a $-V_{in}+V_{err}$ at the top-plate of the DAC. Simultaneously, the low-gain buffer senses the node voltage V_A to the feedback loop capacitors C_{F1}, C_{F2} and C_c. Moreover, the bottom-plate of C_{F1} and C_{F2} are disconnected from the feedback network, while C_c plays the role of an additional compensation capacitor at the top-plate of LSB array as $C_{P,A}$. When its charge is not cleared absolutely, the conversion error will be enhanced. To insure that the sampled V_A only comes from the influence of the $C_{P,A}$, the reset procedure of C_c is necessary. During Φ4, both S_1 and S_2 are on and the bottom of C_{F2} is kept connected to V_{cm}, producing an expected compensation voltage V_F at the top-plate of C_c. The series combination of C_{F1} and C_{F2} leads to a larger V_A at top-plate of C_{F1}, instead of using any active circuit such as a source-follower to buffer the voltage to the compensation capacitor C_c, a passive charge sharing is made directly between C_{F1} and C_c, thus avoiding additional power dissipation.

The proposed charge-cancellation technique can successfully fix the DAC's conversion error with only coarse feedback network accuracy, allowing the process and mismatch insensitive advantages of the charge-cancellation method. As shown in Fig.5, the simulation results of a 10 bit SAR ADC were demonstrated where the proposed method is utilized to compensate 5% to 20% top-plate parasitics of the DAC array. The effectiveness of the charge-cancellation with the parasitic depends on $(1\text{-}k)C_c$ defined in (6), and with ±15% process variations on the $(1\text{-}k)C_c$, the SNDR degrades within 3dB. Furthermore, DAC's conversion linearity

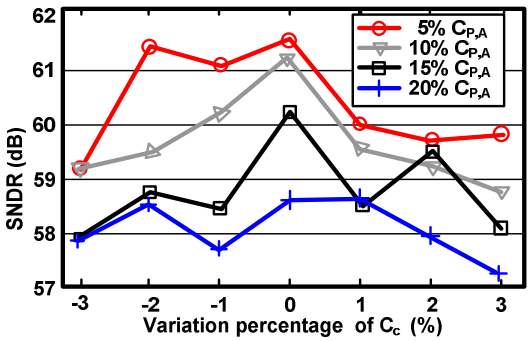

Fig.5. Simulation of SNDR versus the variation of $(1\text{-}k)C_c$ considering 5% to 20% parasitcs.

becomes less sensitive to the parasitic effect after the top-plate parasitics are compensated within 5%, as illustrated in Fig.2.

IV. Simulation Results

The proposed feedback charge-cancellation technique is verified in a 10-bit 80MS/s SAR ADC with a full-scale differential input range $0.8V_{PP}$ in a 65nm CMOS process. The capacitor is implemented as a low cost MOM capacitor instead of a higher quality MIM capacitor. In this design the 10fF unit capacitor with 10% top-plate parasitic is used. The compensation capacitor C_c is 10fF that requires 14fF C_{F1}, C_{F2} (C_{F1} = C_{F2}) to generate the sufficient feedback voltage for charge cancellation. Fig.6 compares the SNDRs with and without the proposed voltage feedback charge cancellation method where 5% to 20% top-plate parasitics are considered. Fig.7 also shows the corresponding 30-time Monte-Carlo mismatch simulations of the split DAC structure with 15% top-plate parasitics, where the ADC achieves a mean SNDR of 58.5dB. Fig.8 illustrates that the DNL and INL can be improved from +3LSB/-0.2LSB to 0.5LSB/-0.4LSB and +1.65LSB/-1.64LSB to +0.72/-0.74LSB, respectively. The total power consumption of the proposed feedback cancellation circuitry is only 100μW.

V. Conclusions

A voltage feedback charge-cancellation technique has been presented, which can remove the parasitic nonlinearity effect in split DAC array. The feedback network consists of a capacitive charge-pump circuit and a compensation capacitor that can successfully attain the charge-cancellation of the top-plate parasitics in the LSB array; hence solving the code-dependent nonlinearity in each bit comparison. Moreover, taking the advantage of charge domain cancellation, the technique can lower the array's sensitivity to the parasitic variation and release the stringent accuracy requirement for the feedback network design. As a result, the conversion linearity of the ADC can be greatly improved with only 100μW power dissipation from the charge-cancellation implementation.

Acknowledgment

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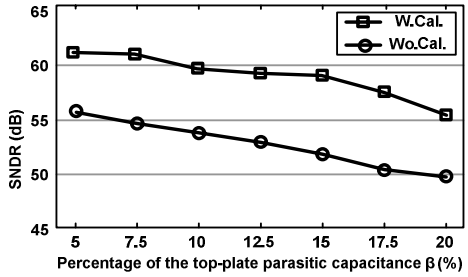

Fig.6. Simulation of SNDR versus β for split DAC structure. (w./wo. charge compensation method)

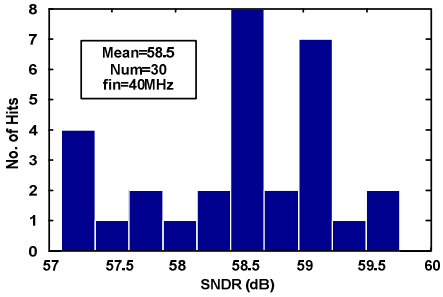

Fig.7. 30-time Monte-Carlo simulations of 10b SAR with split DAC and 15% top-plate parasitcs.

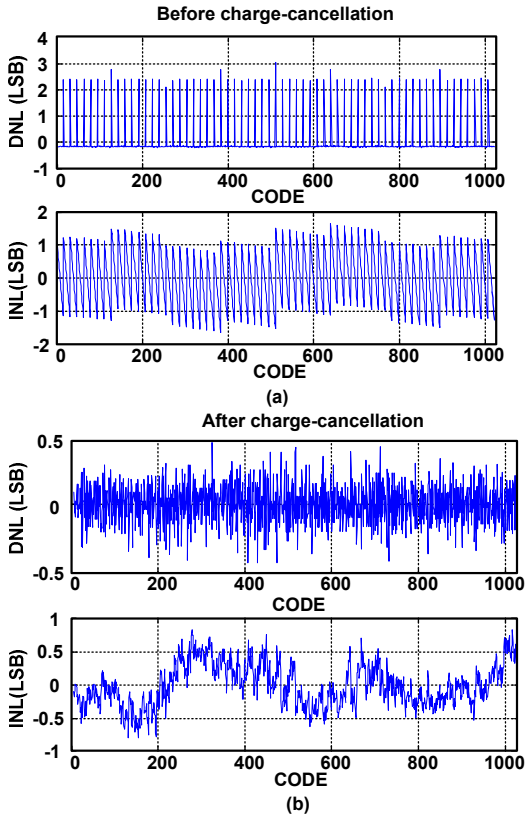

Fig.8. DNL and INL of 10b SAR with split DAC and 15% top-plate parasitics. (a) Before charge-cancellation. (b)After charge-cancellation