Level-Shifting Variable Current Charging Technique for High-Speed Comparator-Based Switched-Capacitor Circuits

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Abstract— **The utilization of variable current sources, in Comparator-Based Switched-Capacitor (CBSC) circuits, instead of the traditional constant current sources, reveals itself as one of the effective ways to increase speed while maintaining the accuracy. In this paper, a Level-Shifting Variable Current Charging Technique is proposed to implement variable current sources for CBSC circuits. The CBSC gain stage obtained with the proposed technique is applied to a 2-1 Cascaded Multi-Stage (MASH) $\triangle\Sigma$ modulator implemented in 90nm CMOS for WCDMA applications. Simulation results show that the modulator achieves 75 dB of dynamic range while consuming 2.7 mW.**

I. INTRODUCTION

Operational Transconductance Amplifiers (OTAs) are one of the major analog building blocks in several types of switched-capacitor circuits such as, pipelined-ADCs, sigma-delta modulators, and switched-capacitor filters, etc. The design of OTAs becomes increasingly challenging due to low intrinsic device gain introduced by deeply scaled CMOS technologies. A straightforward solution to increase the gain is to utilize a gain-boosted amplifier stage, but this approach deteriorates the dynamic range leading to low output swing. Another alternative would be to cascade several gain stages without losing voltage swing, but it can cause instability and will increase power consumption.

To address the challenges faced in scaled CMOS analog circuit design, a new class of comparator-based switched-capacitor circuit topologies has been proposed [1-2] where the opamp is replaced by a comparator and a current source. This combination allows the same charge transfer as an opamp-based implementation without the stability concern of a high-gain and a high-speed feedback loop. However, CBSC circuits suffer from the stringent trade-off between speed and accuracy in the conventional charging scheme [3-6]. The use of variable current sources proposed and demonstrated in [4] is an effective way to increase speed while maintaining accuracy in CBSC circuits. In this paper, an alternative implementation of variable current sources is proposed which can reduce the circuit complexity when compared with [4].

After this introduction a brief review of the conventional structure of CBSC circuits and corresponding operation will be described in section II. The CBSC gain stage with proposed level-shifting variable current charging technique will be presented in section III. In section IV a design example and its simulation results are presented. Finally, the conclusions will be drawn in section V.

II. CONVENTIONAL CBSC CIRCUITS

A. Operation Principle

The operation of a Sample-and-Hold (S/H) with the conventional CBSC circuit implemented in single-ended during its charge transfer phase and the corresponding timing diagram are depicted in Fig.1 (a) and (b), respectively. As mentioned in [1], the CBSC circuit detects virtual ground condition only at the zero crossing instant, rather than the opamp forces virtual ground condition for the entire charge transfer phase.

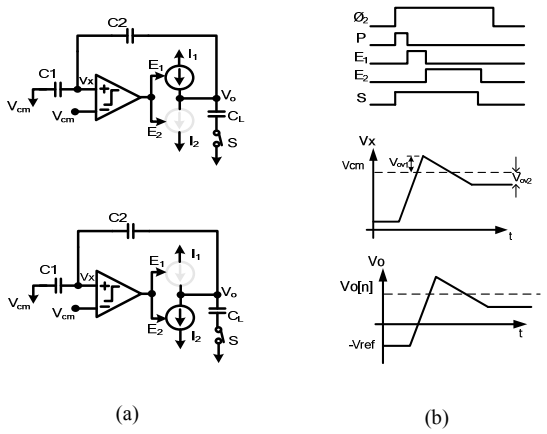


Figure 1: A S/H with the conventional CBSC circuit [1]. (a) Charge transfer circuit (b) Timing diagram

The short preset phase (*P*) ensures that the voltage V_x starts below the virtual ground condition V_{cm}. In the coarse transfer phase (E_1) a large current source I_1 is used to charge up the capacitors network (C_1, C_2 and C_L) and obtains a fast, rough estimate of the output voltage and virtual ground condition. In the fine transfer phase (E_2), a small current source I_2 is used to get a more accurate value for the virtual ground condition and the output voltage. When the comparator detects the second zero crossing the sampling switch S is opened. This defines the sampling instant and locks the sample charge on the load capacitance C_L.

B. Speed and Accuracy

In order to increase speed while maintaining accuracy, in [4] it has been proposed to use variable current sources instead of constant currents used in conventional CBSC circuits. The variable current source changes proportionally to the difference between the virtual ground V_x of capacitors network and the comparator's reference voltage. It is also proposed to use a differential amplifier with current-mirror load to implement this voltage-controlled current source (VCCS) [4]. In this paper, an alternative implementation of VCCS is proposed in which the differential amplifier from [4] could be eliminated such that the circuit complexity can be reduced.

III. PROPOSED LEVEL-SHIFTING VARIABLE CURRENT CHARGING TECHNIQUE

A. Circuit Description

The circuit schematic of a fully-differential CBSC gain stage with the proposed level-shifting variable current charging (LSVCC) technique and the corresponding timing diagram during the charge transfer phase are depicted in Fig. 2 and Fig. 3, respectively. The gain stage is mainly composed by four components: (i) Threshold Detection Comparator K_1, (ii) Voltage Level-Shifter (VLS), (iii) Variable Charging Currents ($M_{vcn1,2}$, M_p) and (iv) Common-Mode Feedback circuit.

The proposed topology includes two sub-phases in the entire charge transfer phase (Φ_{int}) instead of three when compared with conventional CBSC circuits. At the beginning, a brief preset phase Φ_p ensures the differential input voltage is always negative ($V_{inx} > V_{ipx}$), as depicted in Fig. 3. During the second sub-phase Φ_E, the negative input voltage V_{inx} is level-shifted by a voltage level-shifter to become the control voltage of variable current sources (M_{vcn1} and M_{vcn2}). M_{vcn2} is a replica of M_{vcn1} with identical channel length and also the current sink of a current mirror M_p. The output current of the current mirror M_p (i_{op}) will be tracking the current of M_{vcn1} (i_{on}) during the whole sub-phase Φ_E. The charging currents (i_{op}, i_{on}) are set to the largest values at the beginning of Φ_E and become smaller as the differential input approaches the common-mode level V_{cm}. When the comparator K_1 detects the zero-crossing ($V_{ipx} > V_{inx}$) its state changes from '0' to '1' to trigger a D flip-flop. As a consequence the sampling switch S is opened and locks the sample charge on the load capacitance (C_{Ln}, C_{Lp}). After such sampling operation, both charging currents will be turned off. The schematic of the comparator K_1 [5] is depicted in Fig. 4, it consists of three stages: an input pre-amplifier (M_1~M_5), a decision stage (M_6~M_{12}) and an output buffer (M_{13}~M_{17}).

B. Voltage Level-Shifter

The circuit schematic of a voltage-level shifter (VLS) is depicted in Fig. 5 and it operates in two-phases. During the first phase Φ_1, two different voltage differences are sampled onto capacitors C_1 and C_2, respectively. At the second phase Φ_2, the two capacitors are connected in parallel to form a floating voltage source. On the other hand, the diode-connected transistor M_{th} is intentionally biased in the sub-threshold region and hence its gate-source voltage (V_{thpi}) is almost equal to its threshold voltage (V_{th}). The voltage difference V_{sh} at the second phase can be derived by the charge conservation of two parallel-connected capacitors,

$$V_{sh} = \frac{2}{1+x} V_{cm} - V_{thpi} \tag{1}$$

where $AV_{DD} = 2V_{cm}$ and x is the ratio between C_1 and C_2.

C. Level Shifting Variable Charging Current

The level-shifting variable charging currents are simply implemented by NMOS transistors in the saturation region as depicted in Fig. 6. The drain current of a saturated NMOS device neglecting channel-length modulation is equal to

$$I_{D,n} = \beta_n \left(V_{GS} - V_{thn}\right)^2 \tag{2}$$

where $\beta_n = \frac{\mu_n C_{ox}}{2}\left(W/L\right)_n$ is the transconductance parameter. The gate voltage V_{ctrn} of the NMOS $M_{vcn1,2}$ is equal to

$$V_{ctrn} = V_{inx} - V_{sh} \tag{3}$$

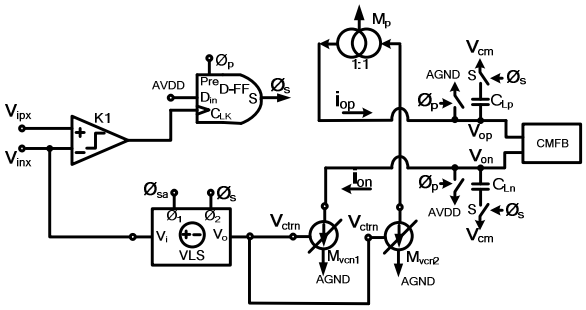


Figure 2: Circuit schematic of the CBSC gain stage with LSVCC Technique.

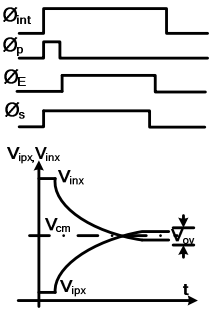


Figure 3: Timing diagram in the charge transfer phase with LSVCC Technique.

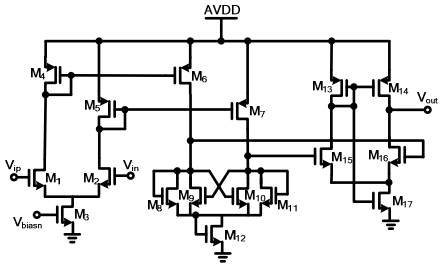


Figure 4: Circuit schematic of the threshold detection comparator K_1.

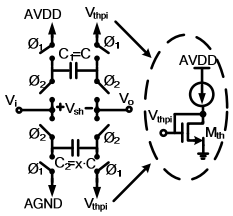


Figure 5: Circuit schematic of the Voltage Level-Shifter

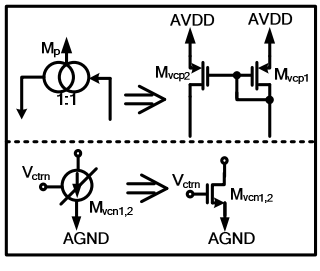


Figure 6: Level-Shifting Variable Current and Current Mirror.

Then, substituting (1) into (3) will lead to,

$$V_{ctrn} = V_{inx} - \left(\frac{2}{1+x} V_{cm} - V_{thpi} \right) \tag{4}$$

and similarly by substituting (4) into (2) the drain current of $M_{vcn1,2}$ will be equal to

$$I_{D,M_{Vcn1,2}} = \beta_n \left(V_{inx} - \frac{2}{1+x} V_{cm} + V_{thpi} - V_{thn} \right)^2 \tag{5}$$

Since M_{th} is the scaled-down replica version of $M_{vcn1,2}$ with identical channel length L, the threshold voltage of the transistor M_{th} will always track the threshold voltage of $M_{vcn1,2}$ and thus the threshold voltages from (5) will cancel themselves. As a result, the drain current of $M_{vcn1,2}$ is equal to

$$I_{D,Mvcn1,2} = \beta_n \left(V_{inx} - V_{dcsh} \right)^2 \tag{6}$$

where $V_{dcsh} = \frac{2}{1+x} V_{cm}$.

From (6), it can be derived that the charging currents vary with the input voltage (V_{inx}) of the gain stage. Besides, the dc level-shift V_{dcsh} predominantly determines the strength of the variable charging current and its quantity directly affects the speed and accuracy of the proposed CBSC gain stage. The current mirror is implemented by two PMOS transistors $M_{vcp1,2}$ as depicted in Fig. 6. The aspect ratios (W/L) of the two PMOS are set to be equal and thus their current will be the same when neglecting the channel-length modulation. M_{vcn2} is the current sink of the PMOS current mirror and it is also a replica of M_{vcn1}. Eventually, the current of M_{vcp2} will be tracking the current of M_{vcn1}.

D. Common-Mode Feeback

The common-mode feedback (CMFB) circuitry for fully-differential CBSC circuits has been proposed in [3]. However, it can not be applied directly into the proposed gain stage because the charging currents are not biased by a fixed gate-source voltage. The circuit schematic of the CMFB adapted to the proposed CBSC gain stage is depicted in Fig. 7, it is composed by two identical extra current branches connected to the output nodes of V_{op} and V_{on} and a switched-capacitor common-mode feedback (SC-CMFB) circuit.

The output common-mode voltage of the gain stage is firstly sensed by a SC-CMFB and its output voltage V_{contrl} either increases or decreases the current sink I_b. The net current between I_a and I_b will compensate the difference between the two charging currents of M_{vcn1} and M_{vcp2} in order to maintain a constant output common-mode. The power consumption in the extra CMFB circuit is very small since the current I_a and I_b are only used for correcting the small deviation in the common-mode voltage.

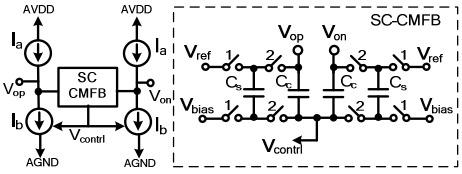
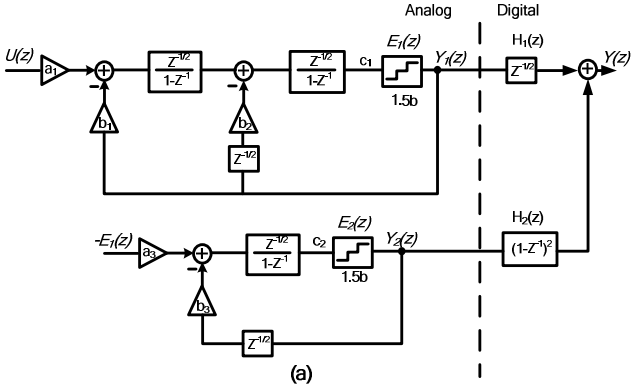


Figure 7: Common-mode Feedback circuit.

IV. DESIGN EXAMPLE

The CBSC gain stage with the proposed technique is applied to a 2-1 MASH $\Delta\Sigma$ modulator for WCDMA applications as a design example. The modulator's block diagram is shown in Fig. 8(a) [7], its coefficients after voltage scaling are $a_1= a_3=b_1=b_2= b_3=0.25$ and the gain of the two 1.5-bit quantizers are both equal to 4. The overall signal and noise transfer functions of the modulator are $STF(z)=z^{-3/2}$ and $NTF(z) = (1-z^{-1})^3$, respectively. The switched-capacitor implementation of the analog part of the modulator with the proposed CBSC gain stage is shown in Fig. 8(b), the digital filters $H_1(z)$ and $H_2(z)$ at the output of the modulator loops have been simulated with MATLAB.

The voltage amplitudes at the input terminals of the 1st integrator with the proposed gain stage (Int_1) during the charge transfer phase are shown in Fig. 9. There, it is shown that the operation of the proposed CBSC gain stage is consistent with the timing waveforms which are illustrated in Fig. 3. The transistor-level simulation results have been obtained with a CADENCE-Spectre simulator in 90-nm CMOS. The output spectra of the modulators with the proposed and conventional CBSC gain stages are both depicted in Fig. 10. They were computed via a 16384-point FFT with input signal amplitude of -5 dBFS and 24.414 kHz. The signal-to-noise and distortion ratio (SNDR) of the two modulators as a function of the input signal amplitude is depicted in Fig. 11. It shows that the peak SNDR of the



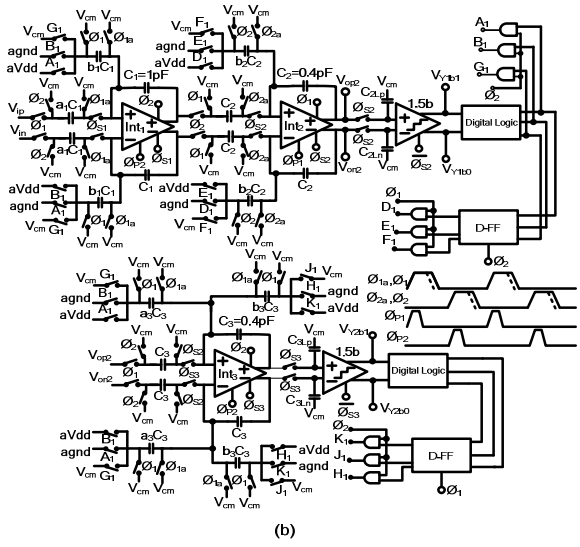


Figure 8: A 2-1 MASH $\Delta\Sigma$ modulator incorporated with the proposed CBSC gain stage.
(a) Block diagram (b) Switched-Capacitor Implementation and clocking scheme.

modulator with the proposed gain stage is approximately 6dB better than the modulator with the conventional. Moreover, the performance comparison between reported state-of-the-art ΔΣ modulators and the modulators with both proposed and conventional CBSC gain stages are summarized in Table 1.

Table I. Performance Comparison with reported ΔΣ Modulators of 2 MHz signal bandwidth

Parameter	Proposed CBSC	Convent. CBSC	[8]**	[9]**		[10]**
Signal BW (MHz)	2		1.92	1.92		1.92
OSR	20		10	12	16	16
Peak SNDR (dB)	70	64	64	65	77	60
DR (dB)	74	65	70	70	79	63
Power (mW)	2.8	5	4.3	3.5	7.4	3.2
*FOM (pJ/conv.)	0.27	0.97	0.86	0.63	0.33	1.02
Architecture	2-1 (3-level)		2-1 (5-level)	2-2 (3-level)		2 (7-level)
Supply (V)	1.2		1.2	1.2		1
CMOS Tech.	90nm		0.13µm	0.13µm		65nm

* $FOM = Pwr / 2 \cdot BW \cdot 2^{(SNDR-1.76)/6.02}$

** *mean experimental results*

V. CONCLUSIONS

A level-shifting variable current charging technique is presented to implement variable current sources for CBSC circuits to enhance the speed and also maintain the accuracy. This is achieved by level-shifting the input voltage of the CBSC gain stage that acts as the control voltage of the charging currents. This technique eliminates the need of operational amplifiers and, subsequently, can reduce circuit complexity and power consumption. Simulation results show that the performance of the modulator incorporated with the proposed CBSC gain stage is slightly better than state-of-the-art ΔΣ modulators.

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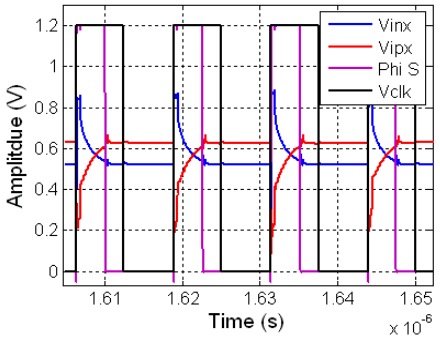

Figure 9: Voltage amplitudes at the input terminals (V_{ixp} and V_{ixn}) of the proposed CBSC gain stage (1st integrator) during the charge transfer phase.

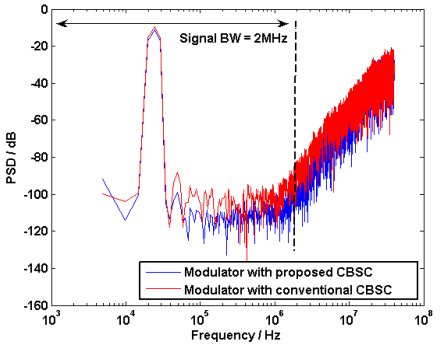

Figure 10: Simulated output spectra of 2-1 MASH ΔΣ modulators with the conventional and proposed CBSC gain stages.

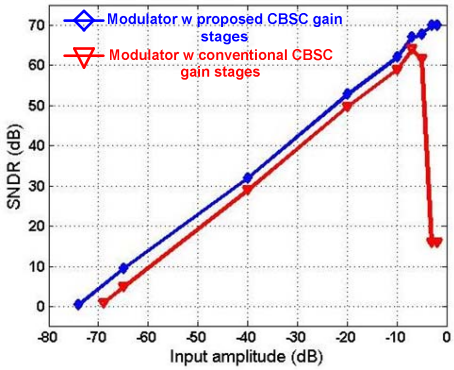

Figure 11: SNDR versus input signal amplitude of the modulators with the conventional and proposed CBSC gain stages.