A Threshold-Embedded Offset Calibration Technique for Inverter-Based Flash ADCs

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Abstract—**A threshold-embedded offset calibration technique for inverter-based Analog to Digital Converter (ADC) is presented. Different from the conventional approach, this work uses a ratio-scaled digital CMOS inverter to define the comparison thresholds, and an extra voltage-controlled resistor is adopted to calibrate the threshold error caused by random mismatch variations. Moreover, a folding flash architecture is employed to reduce the number of inverters by half, which optimizes calibration effort and conversion power. The proposed threshold calibration technique is verified in a 5-bit 800MS/s flash ADC in 65-nm CMOS technology. After the calibration, the post layout simulations (PLS) show that the Effective Number of Bits (ENOB) can be significantly improved from 3.8 bits to 4.7 bits with the total power dissipation of 1mW and achieving a competitive Figure of Merit (FoM) of 48fJ/conv. The area of the whole ADC is 0.04mm^2 only which included calibration circuits.**

I. Introduction

Recently, a new flash ADC architecture was presented in [1] with comparators formed by CMOS inverters, which achieves fully digital implementation with low design complexity in the flash ADC. Furthermore, the inverter-based flash ADC utilizes resistor arrays in series with the CMOS inverters to define the built-in thresholds of the comparators, which avoids the need for the usual separate reference ladder of conventional flash ADCs [2] . However, since the inverters and the resistor arrays suffer from random mismatch variations leading to threshold errors among comparators, the conversion linearity will be enormously degraded. Although this effect can be suppressed by increasing the size of the inverters and resistor arrays, this may consume extremely large power and depreciate the overall performance of the ADC. From the 6mW of measured power consumed by the ADC (working at 600MS/s) [2], most of it is being dissipated by the inverter array. Besides, under high sampling rate, the ENOB of the ADC drops drastically and its speed is limited by the self output loading of the inverter.

This paper presents a novel threshold built-in offset calibration technique used in the proposed inverter-based comparator, where thresholds are pre-defined by the sizing ratio between PMOS and NMOS transistors and the offset is calibrated by an extra voltage-controlled resistor. By eliminating the resistor arrays from [1], the threshold error, in this structure, is only caused by the random mismatch of the inverter, and this error can be detected and corrected by the proposed calibration scheme. A 5-bit 800MS/s folding flash ADC was designed in 65-nm CMOS process with the proposed threshold calibration. Post layout simulations (PLS) show that the SNDR being improved from 24dB to 30dB.

II. Inverter-Based Flash ADC Architecture

The folding architecture from [3] is utilized in this 5-bit flash ADC, which splits the MSB decision in the first step and leaving others 4bits in second steps, to reduce half the number of comparators compared with conventional flash architecture. The 5-bit folding flash ADC is illustrated by Fig. 1, which consists of sampling front-ends, two inverter-based comparison stages, a thermometer-to-binary decoder and a final decoder. During sampling, the positive and negative polarity inputs are sampled into capacitors C_{s1} and C_{s2}, respectively for folding purpose [3] . Since only C_{s1} is selected for the first stage MSB comparison, a dummy inverter is added at the C_{s2}'s top-plate to prevent the input gain mismatch between the C_{s1} and C_{s2}. During conversion, the first-stage inverter, which has middle threshold at the common-mode voltage V_{cm}, compares the sampled input signal in C_{s1}, and then produces "1" or "0" to enable one of the folding switches S1 or S2. These switches will determine the input signal polarity for the second stage. After that, the 15 inverters with different embedded triggering thresholds in the second stage perform the comparisons with the input signal simultaneously, and eventually the final decoder will produce the digital code by combining the 4 bit decisions with the MSB according to the input

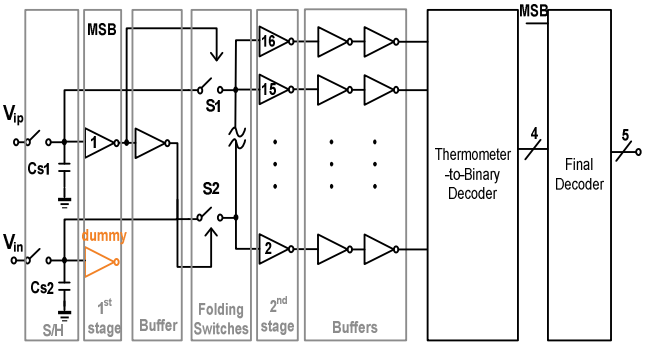

Fig. 1. The architecture of the 5-bit folding flash ADC.

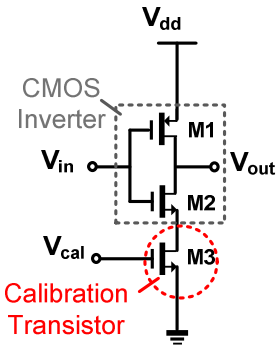

Fig. 2. Schematic of the proposed inverter-based comparator.

polarity.

This architecture has a folding factor of 2 as the conventional folding architecture [4], but with only dynamic power consumption, and it reduces the total number of inverters from 32 to 16 in 5-bit resolution for flash architecture which also reduces the calibration effort, power consumption and die area of the ADC. One of the potential problems of this single-ended architecture is the sensitivity to inductive substrate noise which is not so serious because the ADC resolution is only 5-bit and can be solved by careful layout technique such as guard ring and shields around critical analog components.

III. Circuit Implementation

A. Embedded Threshold

An open-loop amplifier with different switching points is used as embedded-reference comparator, which is presented in Fig. 2. The comparator is basically a CMOS inverter and its switching point (V_{sp}) representing the threshold of the comparator is defined as follows without considering the effect of M3 [5]:

$$V_{sp} = \frac{\sqrt{KP_n \frac{W_n}{L_n} \Big/ KP_p \frac{W_p}{L_p}} \cdot V_{THN} + (V_{dd} - V_{THP})}{1 + \sqrt{KP_n \frac{W_n}{L_n} \Big/ KP_p \frac{W_p}{L_p}}} \quad (1)$$

where KP_n ,KP_p and V_{THN}, V_{THP} are the transconductances and the thresholds of the NMOS and PMOS transistors respectively. From (1) it can be found that, as V_{THN}, V_{THP}, KP_n and KP_p are approximately constant, the V_{sp} of the inverter is only dependent on the W/L ratio between the PMOS and NMOS transistors. Through exact adjustment on the W/L ratio of M1 and M2, the desired V_{sp} of the inverter-based comparator can be easily attained. However, suffering from process and mismatch variation, KP_n, KP_p, V_{THN} and V_{THP} are deviated among the transistors which will lead to threshold errors. In order to calibrate this threshold error, an extra transistor M3 is introduced, as also shown in Fig. 2. The gate-controlled transistor M3, serving as a variable resistor that can be used to adjust the V_{sp} of the inverter according to the following expression [1]

$$V_{sp,cal} = V_{sp,org} + \frac{R_{M3} I_{on}}{2} \quad (2)$$

where I_{on} is the current drawn by the inverter and R_{M3} is the on-resistance of transistor M3. Moreover, the voltage error appearing at the original switching point $V_{sp,org}$ can be compensated by varying the resistance of M3 with a calibration range defined by $R_{M3}I_{on}$. In addition, to maintain the calibration range in each offset calibration of inverter, the size of M3 is identical to M2 which keeps $R_{M3}I_{on}$ in a constant range in each calibration.

B. Calibration scheme of the folding Flash ADC

A calibration scheme is proposed to resist the process and mismatch variation, as illustrated in Fig. 3, which comprises a fine reference ladder, a 16-to-1 multiplexer (MUX) with control logic, 16 sets of inverters with calibration logic and a coarse reference ladder. The circuit schematic of calibration logic and the signal behavior of the MSB inverter during calibration are shown in Fig. 4. Before starting the ADC conversion, the switching points of the inverters in the first and second stages need to be calibrated according to the accurate reference voltage levels supplied by fine reference ladder. The calibration begins from the MSB inverter, and its threshold level is adjusted according to the target threshold value which is selected by the control logic from the fine reference ladder and is pre-sampled onto the input capacitor C_s. Then, the calibration logic controls the gate voltage V_{cal} of M3 and varies from an initial (V_{cm}) towards V_{dd} or ground by an up/down counter through MUX tree with coarse reference ladder, which changes the resistance of the transistor M3 and allows the V_{sp} of the calibrating inverter to approach the sampled reference voltage. The up or down counting is determined by the output of the calibrating inverter which imposes the threshold error polarity. Once the switching of logic level in the inverter's output is detected, the calibration of the MSB inverter is finished. Subsequently, the threshold calibrations of the next 15 inverters are carried out along with the same procedure by proper reference voltages selected from the ladders, and the data conversion begins after all V_{sp} of the inverters are calibrated. It is important to note that the variation step of V_{cal} is defined by the coarse reference ladder which only requires monotonic voltage step for the threshold error correction. While taking the advantage of employing the folding architecture, only half of the reference levels are required when compared with the conventional flash architecture. Hence, the fine reference ladder is divided in 16 equivalent voltage segments from V_{dd} to V_{cm} and it will be powered off when the calibration is completed. This power off operation is achieved by disconnect the path from V_{dd}

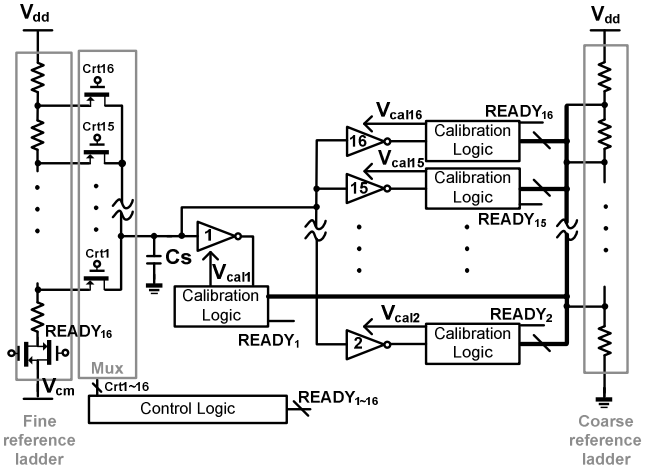

Fig. 3. Circuit schematic of the proposed calibration.

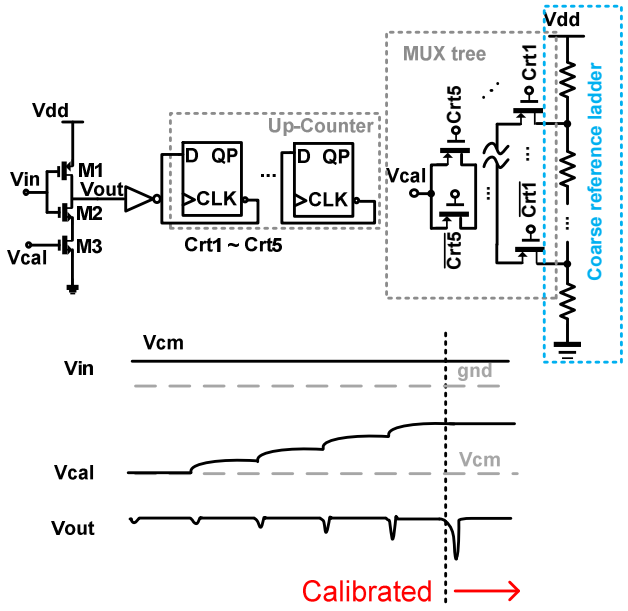

Fig. 4. Circuit schematic of the calibration logic (one set example) and signal behavior.

to V_{cm} via a transmission gate switch, as already shown in Fig. 3, which only introduces a constant voltage shift among the thresholds and have no effect to the conversion linearity. Besides, the calibration and control logics consume power only during the calibration, so the power consumption of the calibration during the active conversion is just from the coarse reference ladder which is very small.

One potential issue of the proposed threshold calibration technique is the charge-sharing effect between the sampling capacitor and the second-stage parasitic gate capacitance of 15 inverters. Since the sampled fine reference voltages need to be passed to all the inverters' input through the folding switch, this induces gain errors to the calibrated reference levels. If this gain error is kept constant before and after calibration, it will not cause any conversion nonlinearity. Nevertheless, while either one of the input transistors M1 or M2 is in the triode region during calibration, the gain mismatch due to large gate capacitance variation of those 2 transistors can greatly affect the conversion linearity. Although the gate capacitance variation of one transistor is small, when added together in a total of 30 transistors, from the second stage, it could become quite large. Thus, the initial voltage of V_{cal} is set to V_{cm} from the coarse reference ladder to keep all transistors in the saturation region. Fig. 5 exhibits an example of a charge sharing effect when M3 is working in different operation regions through controlling V_{cal} and the sampled input voltage of inverter is 690mV. From there, it is possible to conclude that the voltage variation on the sampling capacitor is much larger than the cases where M3 is saturated.

C. *Power and bandwidth analysis*

The bandwidth of the inverters is usually limited by the output loading capacitance, consisting of the gate capacitance of the next stage buffer and the junction capacitance from the NMOS and

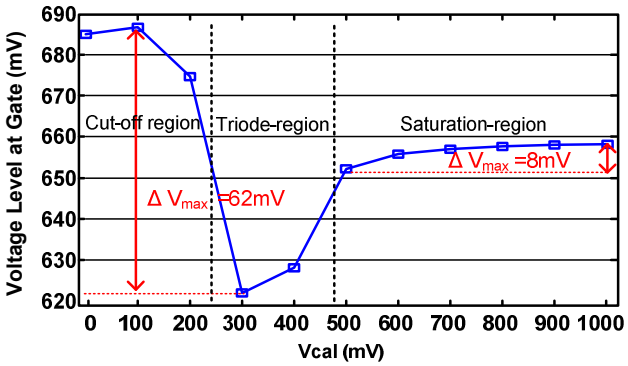

Figure 5. Gate voltage of inverter vs Vcal.

PMOS transistors of the inverter itself. In general, the output logic gate is designed with a small dimension and the ADC's bandwidth is dominated by the self junction capacitance of the inverter. Taking advantage of the calibration, the size of the inverter is greatly shrunk since no matching requirement is considered. When compared with the conventional non-calibrated one, this work improves the inverter bandwidth and thus enhances the conversion speed and reduces the power consumption. Instead of what is present in [1], the differences of bandwidths and delays among the inverters are resolved by moving the system into discrete time with sampling front-end. Furthermore, the CMOS inverter only consumes power when both the PMOS and NMOS transistors are turned on [6] , which is the case when the input of the inverter is near the V_{sp}. Since for every sampled input, there is only one inverter which is near the switching threshold, and there are no static current drawn in other inverters at the same instant of time. As a result, it saves a significant amount of power in the comparator array.

IV. Simulation Results And Comparison

The performance of the 5-bit folding flash ADC was verified with post-layout simulations using a standard 65-nm CMOS process. Fig. 6 shows the ADC core layout which occupies $0.04mm^2$ of active area only where $0.006mm^2$ is calibration circuits with comparators. The ADC operated with a 1V supply, 800M/s sampling rate and draws 1mW of power while the peak power consumption during the calibration operation is 14mW. The calibration operates with the same conversion rate of the ADC and performs before the ADC's conversion. The maximum calibration time is 640ns seconds which depends on the offset of each comparator. The SNDR of the ADC with and without calibration has been performed with 20 times Monte-Carlo simulations including process and mismatch variations, which are plotted in Fig. 7, showing improvements in the worst-case from 21dB to 27dB, and in the average SNDR from 24dB to 30dB.

Fig. 8 shows the differential and integral nonlinearities (DNL/INL) before and after calibration for the worst case (Monte-Carlo). The DNL and INL can be improved from +1.58/-1LSB to +0.35/-0.52LSB and from +1.74/-1.76LSB to +0.36/-0.41LSB, respectively. Finally, Fig. 9 presents the spectrum plot of the inverter-based flash ADC through a Monte-Carlo simulation with an input signal of 355MHz leading to an SNDR of 30dB. The ADC achieved an FoM of 48fJ/conv and Table I shows the performance comparison of this ADC to [1] and [7] .

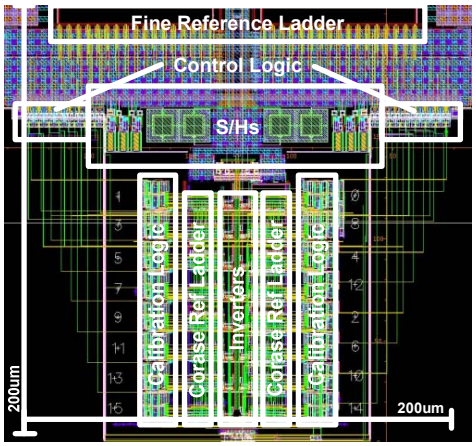

Fig. 6. ADC core layout.

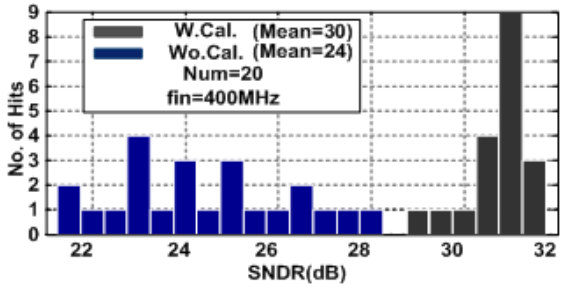

Fig. 7. 20 times Monte-Carlo SNDR before and after calibration simulations at Nyquist sampling rate. (Mean = 30 dB, 24dB)

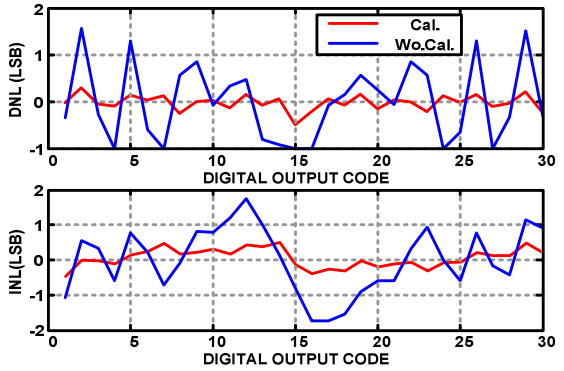

Fig. 8. IDN and DNL before and after calibration for the worst case of the Monte-Carlo simulations.

TABLE I. PERFORMANCE COMPARISON

	Conventional [1]	[7]	This work
Input range	420mV	/	800mV
Sampling rate	600MS/s	1.75G/s	800MS/s
Power	6.7mW	7.6mW	1mW
DNL (LSB)	+0.31/-0.25	-0.34/+0.38	+0.35/-0.52
INL (LSB)	+0.87/-0.61	-0.07/+0.39	+0.36/-0.41
ENOB @ Nyquiest	3.8bits	4.7bits	4.7bits
SNDR @ Nyquist	25dB	28.2dB	30dB
FoM @ Nyquist	800fJ/conv	1500fJ/conv	48fJ/conv
Supply	1.2V	1V	1V

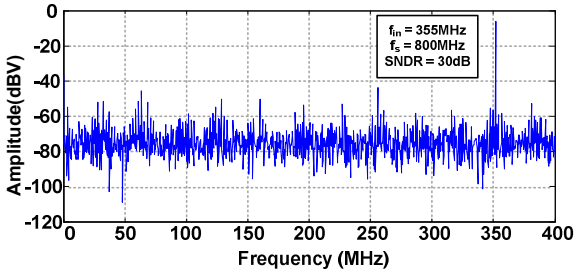

Figure 9. Simulated FFT spectrum of the ADC.

V. CONCULSIONS

A threshold pre-defined offset calibration technique is proposed and implemented in an inverter-based folding flash ADC which can reduce the power consumption and improves the SNDR significantly. This work utilizes ratio-scaled CMOS inverter to pre-define the threshold of the inverter-based comparators and adopts a voltage-control resistor for calibrating the offset in each comparator. Post-layout simulation results confirm that the ADC with the proposed calibration can work at 800MS/s with 1mW power in 4.7bits ENOB and achieve 48fJ/conv FoM. As technology continues to scale down, the random mismatch will greatly affect the performance of inverter-based comparator topologies, but the proposed calibration can enhance the potential performance of such architectures.

ACKNOWLEDGMENT

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