A Power Effective 5-bit 600 MS/s Binary-Search ADC with Simplified Switching

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***Abstract*—This paper proposes the design of a binary search ADC that uses two different techniques, namely, distributed-residue and folding. These can prevent signal dependent offset and reduce the switching network complexity. A 5-bit binary-search ADC applying such proposed techniques has been developed in 65 nm CMOS. It consumes 540 µW under 1V supply voltage at the operating frequency of 600 MS/s. The simulation results demonstrate that the design achieves a SNDR of 30.8 dB at Nyquist input frequency with a figure of merit (FOM) of 32 fJ/conversion-step.**

Keywords-- Analog-to-Digital Converter (ADC); Asynchronous binary-search ADC.

I. INTRODUCTION

Low resolution high-speed ADCs are widely used for wireless communication applications such as ultra wideband (UWB) systems. The advantages of flash [1] and SAR [2] ADCs have been adopted by the binary-search architecture [3] [4], thus achieving high-speed and low power requirements. Fig. 1(a) shows the block diagram of the conventional binary-search ADC [3]. Its operation principle is similar to what is utilized in SAR ADCs which approximate the sampled input and converts the digital code bit by bit. Comparing with the SAR architecture the binary-search scheme utilizes more comparators with prepared references but does not require a feedback loop to charge the capacitive DAC, which leads to a higher conversion speed than the SAR. Comparing with the flash scheme an N-bit binary-search ADC activates only N times the comparators for one sample's quantization which reduces drastically comparator's power consumption. Fig. 1(b) shows the modified binary-search architecture [4] that reduces the total number of comparators from 2^N-1 to 2N-1, for a requirement of N-bit resolution. However, this architecture exhibits two major drawbacks. First, the transition thresholds of the comparators are changing with the different input reference voltages, causing signal dependent offset. Second, the modified scheme reduces the exponential growth of the comparators at the cost of a massive increased complexity of the switching network in each bit stage, implying large power consumption from the reference ladder.

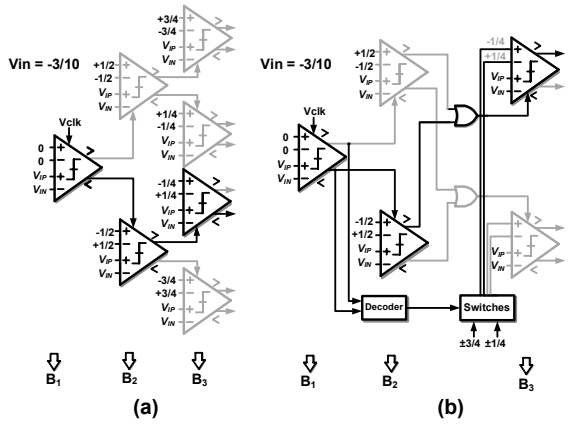

Figure 1. (a) Conventional binary-search architecture
(b) Modified binary-search architecture

In this paper a new binary-search scheme is proposed which employs a residue distribution technique to avoid the signal dependent offset errors, allowing the comparators to be digitally calibrated before the ADC operation. The folding technique is applied to reduce the total number of switches connected directly to the reference ladder, leading to less complexity and reduced power consumption.

II. PRINCIPLE OF OPERATION

Fig. 2 shows the N-bit block diagram of the proposed architecture, and it is composed of N bit-stages. Except the 1st stage, each bit-stage consists of two comparators with proposed switching networks. The ADC operates with the ayschronous scheme simliar to [4]. The n^{th}-stage comparator output generates the clock phase for the $(n+1)^{th}$ stage to achieve fast forward bit-quantizations, and it also determines the reference voltages in the $(n+2)^{th}$ stage required to switch beforehand.

The modified architecture [4] used the massive switch network with the threshold prediction technique to approach the sampled input at each bit-stage, but the predicted comparators' threshold voltages are always changed with the different sampled input voltage. Since different thresholds cause various transient states in the comparators' input

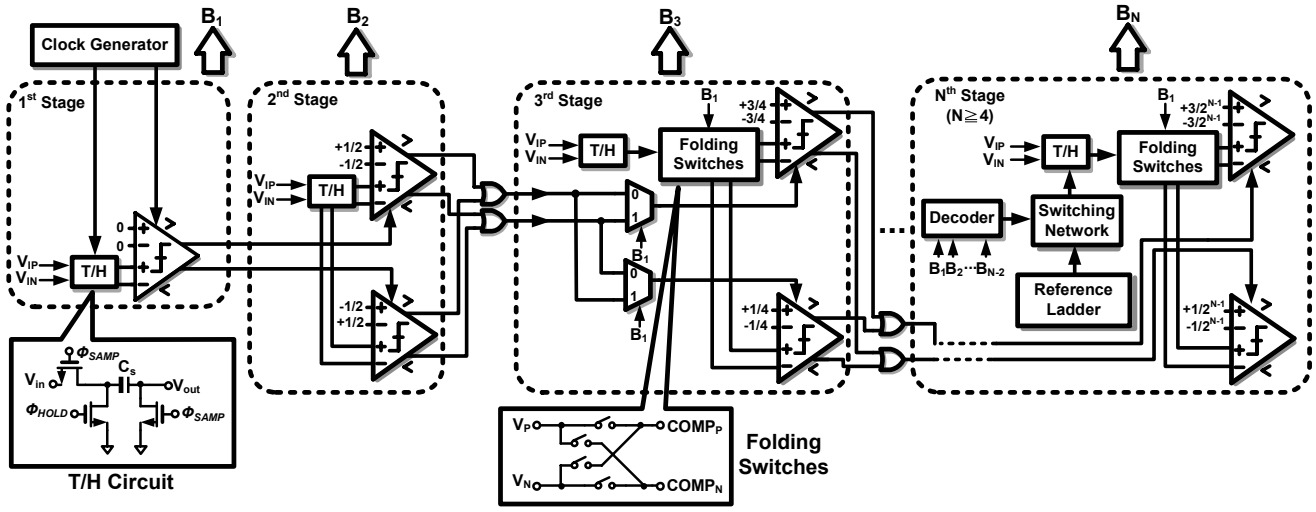

Figure 2. N-bit block diagram of proposed architecture

transistors, signal dependent offsets are inherent in the comparators, which cannot be calibrated. Differed from [4] the proposed ADC applies fixed threshold for each comparator input to approach the residue during the bit-quantization. Distributed T/Hs are employed at each stage instead of the global sampling capacitor, and the sampled input is stored at each bit-stage individually. While the n^{th}-stage generates a bit result, the appropriate reference voltage is connected with the bottom plate of distributed T/H to generate the residues through the switching network in the $(n+2)^{th}$ stage. As the residue is compared with the fixed threshold of the comparator, there is no signal dependent offset.

In addition, a folding switch technique is applied here to simplify the switching network of the binary-search ADC. If the differential input signal is inversely connected with the input of the comparator through the folding switch, then it is equivalent to connect with a threshold-inversed comparator. Note that the threshold voltage connected with the comparator is not inversed in fact, so it does not induce any signal dependent offset. In the proposed scheme, the fixed threshold comparators working with the distributed T/Hs and folded switches simplify the switching network but generate all the required threshold voltages during the quantization. For an example as shown in Fig. 3, the modified approach [4] uses the 4-bit switching network to select the thresholds, ±1/8, ±3/8, ±5/8 and ±7/8, for two comparators in the 4^{th} bit-stage. The proposed scheme only requires two fixed threshold (i.e. +1/8 and +3/8 in single-end) comparators, and the 2-bit switching network to choose the reference voltage ±1/2 and 0. By connecting the reference voltage at the bottom plate of the T/H to generate the residue, the equivalent thresholds of the comparators become (+1/8+0) = +1/8, (+3/8+0) = +3/8, (+1/8+1/2) =+5/8 and (+3/8+1/2) =+7/8. If the quantized MSB is '0', the positive thresholds are no longer useful. At this moment, the input signal can be folded, so that the negative thresholds, -1/8, -3/8, -5/8 and -7/8, comes up to the circuit. The complexity of the switching network is reduced because the folding operation provides the negative thresholds.

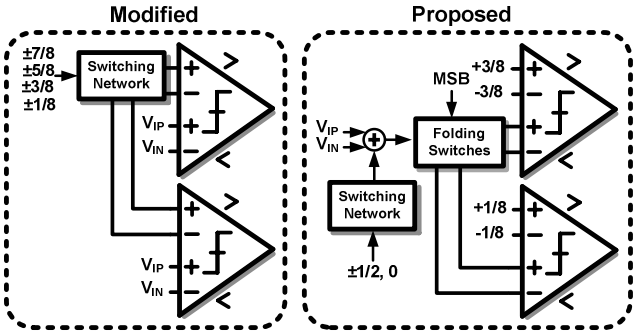

Figure 3. 4^{th} bit-stage of modified and proposed schemes

While the folding switches are turned on, charge sharing happens between the sampling capacitors and the input parasitic capacitance of comparators causing a gain loss error between the sampled input and threshold voltages in the comparator input pairs. A parasitic matching method [5] has been employed here to compensate the gain error mismatch causing by sampling the analog input and threshold voltages into the duplicate sampling capacitors. During the sampling phase Φ_S, all inputs of the comparator are connected to the common-mode V_{CM} in order to clear the memory effect. The capacitor, C_{S1}, shown in Fig. 4, samples the threshold voltages ($V_{P,N}$ and $V_{N,N}$). During the hold phase Φ_H, the bottom plates of C_{S1} are connected to V_{CM}, where the top plates of C_{S1} are connected to the reference inputs of the comparator. The capacitor, C_{S1}, has identical dimension and parasitic capacitances to compensate the gain loss error.

III. CIRCUIT IMPLEMENTATION

The following sub-sections describe the implemented circuits of the proposed techniques for a 5-bit binary search ADC.

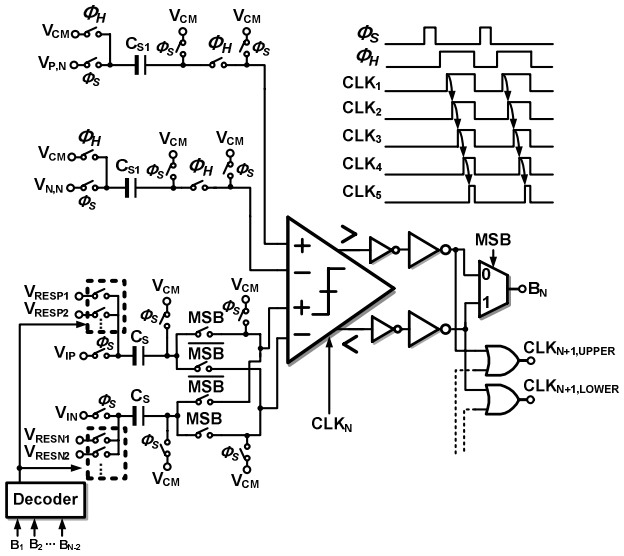

Figure 4. Implemented circuit of the N[th] stage, where N≥4

A. Asynchronous Clock Generation

The clock phases of the proposed binary-search ADC are shown in Fig. 4. The clock generator generates the sampling phase Φ_S, hold phase Φ_H, and the activating phase CLK_1 of the 1st stage comparator. The asynchronous logics of the following stages generate the remaining activating phases CLK_2 to CLK_5 of comparators during the conversion.

B. Switching Network

Fig. 4 shows the detail schematic of the N[th] bit-stage. The inputs signals, V_{IP} and V_{IN}, are sampled into the sampling capacitors C_S, during the sampling phase. The capacitance of the C_S is 40 fF, which is enough to make the kT/C noise negligible. All comparator inputs are connected with common-mode voltage V_{CM} to discharge the input parasitic capacitance and clear the memory effect while the C_S is sampling. During the hold phase, the top plates of C_S connect to the comparator inputs through the folding switches according to the MSB (B_1). If the MSB is '0', there should be a folding operation, so the top plates of C_S will be inversely connected to the comparator inputs, and the comparator outputs must be inverted to get the correct output bit result. Or otherwise, the MSB is '1', the top plates of C_S will be directly connected to the comparator inputs, and the bit result is achieved from the directed connection of the comparator output. Therefore, a MUX is placed at the output of the comparator and it is controlled by MSB. The bottom plates of C_S are connected to the reference voltages (V_{RESP1}, V_{RESP2}, …, V_{RESN1}, V_{RESN2}, …) to generate the residue according to the previous quantized bits B_1, B_2, …, B_{N-2}.

C. Dynamic Comparator

In binary-search ADC design, comparator is the main analog block. It must be power efficient because not all the comparators are operating all the times. Therefore, the comparator design should not consume any static power. The implemented four input dynamic comparator [6] is shown in

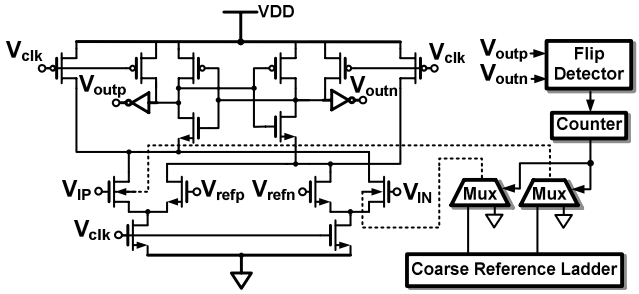

Figure 5. Comparator and offset calibration

Fig. 5. When the V_{clk} signal goes low, the memory of the comparator is cleared. The regenerative latch above the input pair forms a positive feedback loop, which converts the difference between the input and the reference signal into digital signal. The regenerative latch operates when V_{clk} signal goes high. Therefore, there is no static power wasted.

D. Comparator Offset Calibration

The mismatch of the input pair transistors causes unbalanced trans-conductance, *gm*. This unbalanced *gm* causes offset problem. Fig. 5 shows the block diagram of the offset calibration algorithm to balance the *gm* of the input pair [2]. During the calibration process, the differential inputs, V_{IP} and V_{IN}, must be set to the comparator's threshold, V_{refp} and V_{refn}. The flip detector determines the offset polarity at the beginning of the calibration by the comparator outputs, V_{outp} and V_{outn}. The polarity determines the outputs of multiplexers, MUX, to either connect to the coarse reference ladder or ground. The counter, together with the MUX, controls the reference voltage feedback to the comparator. The feedback voltage controls the biasing voltage of the higher *gm* transistor. An increase in the transistor's biasing voltage can slightly decrease *gm*. Thus, the counter counts up to increase the feedback voltage until the comparator outputs are flipped, which means the offset is minimized. Afterwards, the calibration result is stored into the counter, and the whole calibration circuit should be powered-off during normal ADC operation.

IV. Simulation Results

The proposed 5-bit binary-search ADC has been designed in 65nm CMOS with 1V supply. The simulation results demonstrate that the proposed binary-search ADC can operate with 5-bit at 600 MS/s consuming only 540μW. The analog part, digital part, and reference ladder consume 278μW, 118μW, and 144μW, respectively. Correspondingly, the SS, TT, and FF corner simulation results of the SNDR with noise are 31.62 dB, 31.69 dB, and 31 dB. The DNL is 0.524/-0.465 LSB and the INL is 0.272/-0.325 LSB, as shown in Fig. 6. Fig. 7 shows the FFT spectrum of the $1V_{p-p}$ input at Nyquist frequency. The SFDR is 43.02 dB. Fig. 8 (a) shows the SNDR versus input frequencies at the sampling rate of 600MS/s, and the ERBW is close to 3.1 GHz. On the other hand, Fig. 8 (b) shows the SNDR versus sampling frequencies at Nyquist input. The Monte Carlo Analysis of 100 iterations, with process and mismatch, is shown in Fig. 9. The average SNDR with noise is 30.8 dB. In the proposed architecture, with a defined Figure-

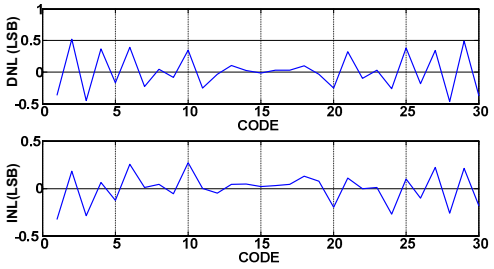

Figure 6. DNL/INL

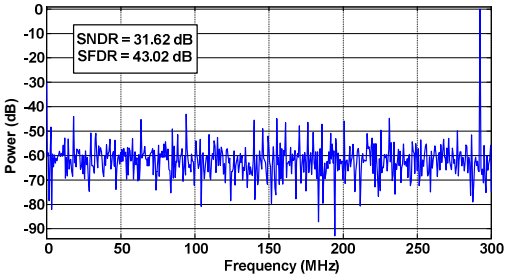

Figure 7. FFT spectrum for a 1 V_{p-p} Nyquist input signal (TT model)

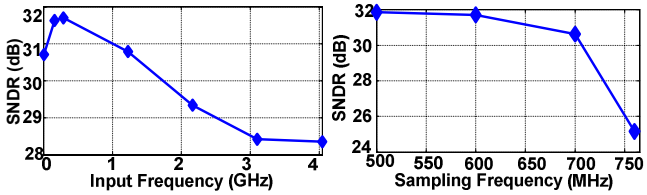

Figure 8. (a) SNDR versus input frequencies at f_S = 600 MS/s
(b) SNDR versus sampling frequencies at Nyquist input

of-Merit FOM=POWER/(2^{ENOB}·f_S), the value obtained is 32fJ/conversion. Table I shows the comparison with other state-of-the-art high-speed low resolution ADCs [1]-[5] [7] [8].

V. Conclusion

A 1-V 5-bit 600 MS/s asynchronous binary-search ADC designed in 65 nm CMOS has been presented. Using the distributed-residue technique the offset error can be calibrated by foreground calibration. The folding technique reduces the number of switches directly connected to the reference ladder. The simulation results demonstrate that the design consumes 540µW of power. It achieves a SNDR of 30.8 dB at Nyquist input frequency and the FOM is 32 fJ/conversion-step.

Acknowledgment

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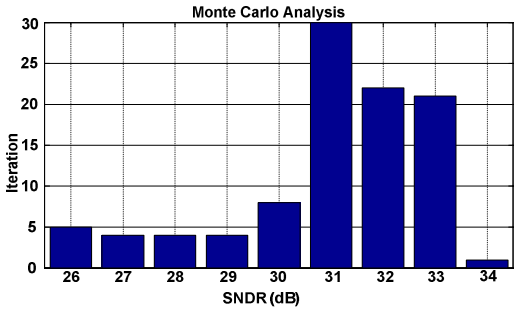

Figure 9. Monte Carlo Analysis

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART

	[1]	[2]	[3]	[4]	[5]	[7]	[8]	This work	
Technology	90	45	90	65	65	130	65	65	nm
Supply Voltage	1	1.1	1	1	1	1.2	1	1	V
Input Range	0.8	1	0.768	0.6	1	1.2	0.8	1	V_{P-P}
Resolution	5	7	7	5	4	6	5	5	bit
DNL	0.3	0.5	0.48	0.62	0.3	N/A	0.26	0.524	LSB
Sampling Rate	1750	2500	150	800	1000	1250	500	600	MS/s
SNDR @ Nyquist	28.5	34.3	39.7	26.92	23.7	27	26.1	30.8	dB
Power	2.2	50	0.133	1.97	0.43	32	6	0.54	mW
FoM	60	480	10.4	116	34	3050	750	32	fJ/step

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