A Voltage Feedback Charge Compensation Technique for Split DAC Architecture in SAR ADCs

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***Abstract*— A voltage feedback charge compensation technique is presented to prevent the conversion nonlinearity due to the parasitic effect of split capacitive DAC structure in successive approximation register (SAR) ADCs. The charge compensation is achieved by using an open loop amplifier that performs voltage feedback to the DAC array via a compensation capacitor, which is easy to be implemented with very low power dissipation. The technique is utilized in the design of a 10b 80MS/s SAR ADC in 65-nm CMOS technology. The simulation results show that the proposed charge compensation technique can improve the Effective Number of Bits (ENOB) from 8.3bits to 9.6bits and differential/integral nonlinearity from 3LSB/1.65LSB to 0.45LSB/0.74LSB respectively with only 300 µW power dissipation in the proposed charge compensation circuitry.**

I. Introduction

The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and subtract the reference voltage [1][2]. Usually a binary-weighted architecture is employed for better linearity, but as the resolution increases, the array capacitance raises exponentially with the resolution, which consumes large switching power, settling time and area. Especially, for high-resolution and high-speed applications a very low output impedance of the reference buffer is required to speed-up the DAC's settling, the buffer will draw extremely large static power from the supply rail which is also difficult to be achieved [3]. Therefore, the speed and power limitations of the binary-scaled structure keep it from being used in high-speed and high-resolution implementations.

Split DAC architecture has been popular for implementation of high speed SAR ADCs, but the parasitic nonlinearity effect prevents it from achieving high resolution [4]. The parasitic capacitance can be reduced by using additional layers to form metal-insulator-metal (MiM) capacitors [5]; however it increases fabrication costs as MiM capacitors are rarely available in process options used in industry. Another solution implies the calibration of the parasitic nonlinearity effect by adjusting the size of the attenuation capacitor. In practice, such tunable capacitor with very small calibration step size is difficult to be implemented, due to its highly sensitive dependency on the DAC's conversion accuracy which may destroy the defined binary-scaled ratios and lead to even worse conversion linearity.

This paper proposes a charge domain compensation method that significantly improves the conversion linearity by achieving the charge compensation with the top-plate parasitic capacitors, which is implemented by using an active voltage amplifier to sense and suppress the voltage error in each bit comparison, as presented in Sections II and III. The charge compensation approach was employed in both single split (SS) and dual split (DS) DAC structures, demonstrated in a 10b 80MS/s SAR ADCs in 65-nm CMOS. The simulation results in Section IV show that, with 15% top-plate parasitic in each unit capacitor, the Signal-to-Noise-and-Distortion Ratio (SNDR) can be improved from 51.8dB to 59.5dB (in SS) and 43.8dB to 54.8dB (in DS), respectively, which proves the DAC's high immunity to the parasitic nonlinearity when the charge compensation technique is used. The conclusion will then be drawn in Section V.

II. Charge Compensation Technique

A. Parasitic nonlinearity effect in split structure

The architecture of the n-bit SAR ADC is shown in Fig.1, consisting of a split capacitive DAC array, a comparator and SA control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. A split

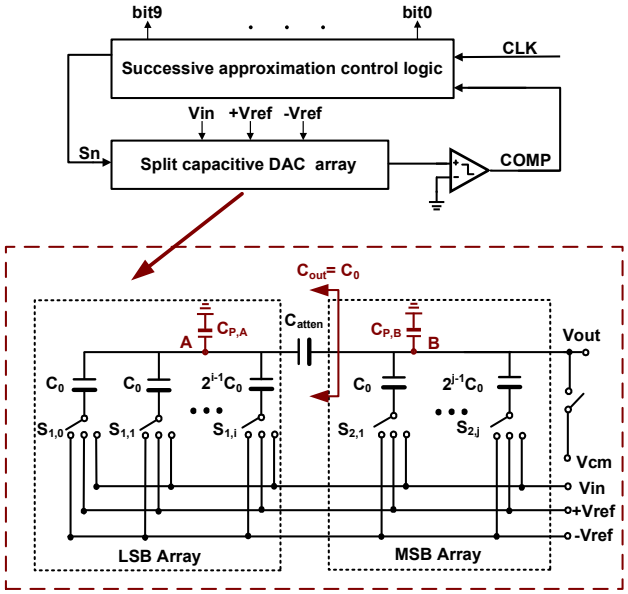

Fig.1. Overall SAR ADC architecture and the n-bit split DAC structure. (n=i+j).

capacitive DAC array is selected for the advantages of its smaller array capacitance, fast DAC settling and power saving. The attenuation capacitor C_{atten} is used to separate the DAC into j-bit MSB and i-bit LSB binary-scaled sub-arrays. When compared with the binary-weighted structure, the MSB capacitor and the equivalent output capacitance can be reduced from $2^{n-1}C_0$ and 2^nC_0 to $2^{j-1}C_0$ and 2^jC_0, respectively, with C_0 being the unit capacitor of the DAC array.

One potential issue of the split architecture is its vulnerability to the parasitic effect [6], as illustrated in Fig.1, where the parasitic capacitance $C_{P,B}$ and $C_{P,A}$ on the nodes B and A are introduced by the bottom- and top-plate parasitic capacitance of C_{atten} as well as the top-plate parasitic capacitance of MSB and LSB array capacitors, and can be expressed as,

$$C_{P,B} = \alpha \cdot C_{atten} + \beta \cdot C_{Sum,MSB} \quad (1)$$

$$C_{P,A} = \beta \cdot C_{atten} + \beta \cdot C_{Sum,LSB} \quad (2)$$

where $C_{sum,MSB}$ and $C_{sum,LSB}$ are the total capacitance of the MSB and LSB array, and α, β represent the percentage of bottom- and top-plate parasitic capacitance of each capacitor, respectively. The analog output V_{out}, considering $C_{P,A}$ and $C_{P,B}$, can be calculated as

$$V_{out} = \frac{C_{atten}\left(\sum_{n=1}^{i} S_{1,n} 2^{n-1} C_0 + \sum_{n=1}^{j} S_{2,n} 2^{n-1} C_0\right) + \left(C_{SumLSB} + C_{P,A}\right) \sum_{n=1}^{j} S_{2,n} 2^{n-1} C_0}{C_{atten}\left(C_{SumLSB} + C_{SumMSB} + C_{P,B} + C_{P,A}\right) + \left(C_{SumLSB} + C_{P,A}\right)\left(C_{SumMSB} + C_{P,B}\right)} V_{ref} \quad (3)$$

where S_n equal to 1 or 0 is the ADC decision for bit n. As this equation shows the parasitic capacitance $C_{P,A}$ and $C_{P,B}$ in the denominator are completely uncorrelated in the bit decisions, which will cause only a gain error and will not affect the linearity performance. However, the parasitic capacitance $C_{P,A}$ in the numerator contributes with code-dependent errors, which degrade the conversion linearity. A behavioral simulation of a 10-bit SAR ADC is presented in Fig.2, which illustrates the conversion sensitivity to the variation of $C_{P,A}$. From the plot it can be deducted that when β varies within 5%, good conversion linearity can still be ensured. As β increases larger than 10%, the SNDR drops significantly. Typically, it happens after the layout routing when metal-oxide-metal (MOM) plate or fringe capacitors are used.

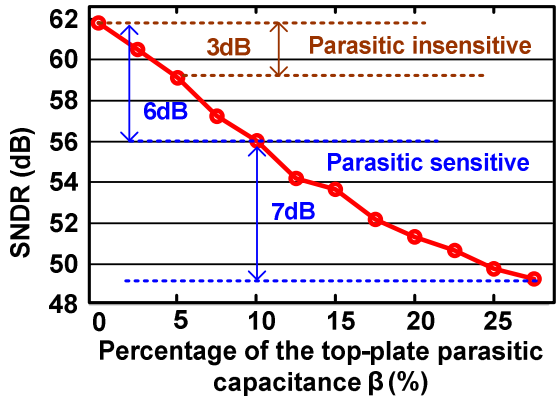

Fig. 2. Behavioral simulation of SNDR versus the percentage of the top-plate parasitic capacitance β.

B. *Feedback charge compensation*

The principle of the charge-compensation technique is demonstrated with a two bit capacitive DAC example, as shown in Fig.3(a). Initially at time 0, all the array capacitors are reset to

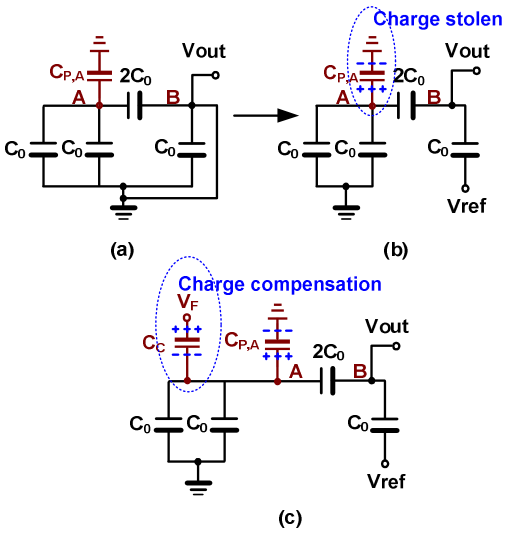

Fig.3. (a) Reset DAC array. (b) MSB transition.(c) Charge compensation can be achieved in node A when C_c is added.

ground, producing a 0V at the DAC's output $V_{out}[0]$. Then, in Fig.3(b), the MSB capacitor is switched to a reference voltage V_{ref} and others are kept connected to ground. Ideally, the output of the DAC is 1/2 V_{ref}, but when the parasitic capacitance $C_{P,A}$ is included, a voltage error exists at the output $V_{out}[1]$ after the first bit transition. According to the charge conservation principle, $V_{out}[1]$ can be calculated as

$$V_{out}[1] = \frac{4 + C_{P,A}}{8 + C_{P,A}} V_{ref} \quad (4)$$

subtracting (4) from its nominal value, and the voltage error will become

$$V_{err} = \frac{C_{P,A}}{16 + 2C_{P,A}} V_{ref}. \quad (5)$$

The V_{err} happening from (5) is caused by the charge stolen by $C_{P,A}$ at node A which can be represented as $(V_A[1]\text{-}V_A[0])C_{P,A}$. Theoretically, as shown in Fig.3(c), when a compensation capacitor C_c is applied to node A, with a feedback voltage V_F (V_F=$k(V_A[1]\text{-}V_A[0])$, where k is the amplification factor that satisfied the following relationship:

$$(1-k)(V_A[1]-V_A[0])C_C + (V_A[1]-V_A[0])C_{P,A} = 0 \quad (k>1) \quad (6)$$

then charge compensation in $C_{P,A}$ can be achieved. Qualitatively, (6) means that the charge injected from C_c is identical to that in $C_{P,A}$ but with the opposite polarity, as a result the voltage error at the DAC's output can be corrected.

Following the conceptual illustration above, a voltage feedback network is required to track and amplify the node voltage V_A after each bit transition and returning the result at the summing node of A. The amplification factor k relies on the capacitance of the compensation capacitor C_c, as defined in (6) to adopt the charge compensation. The flexibility of the amplification factor k relaxes the design effort and it can be easily achieved through an open loop amplifier, which will be discussed next.

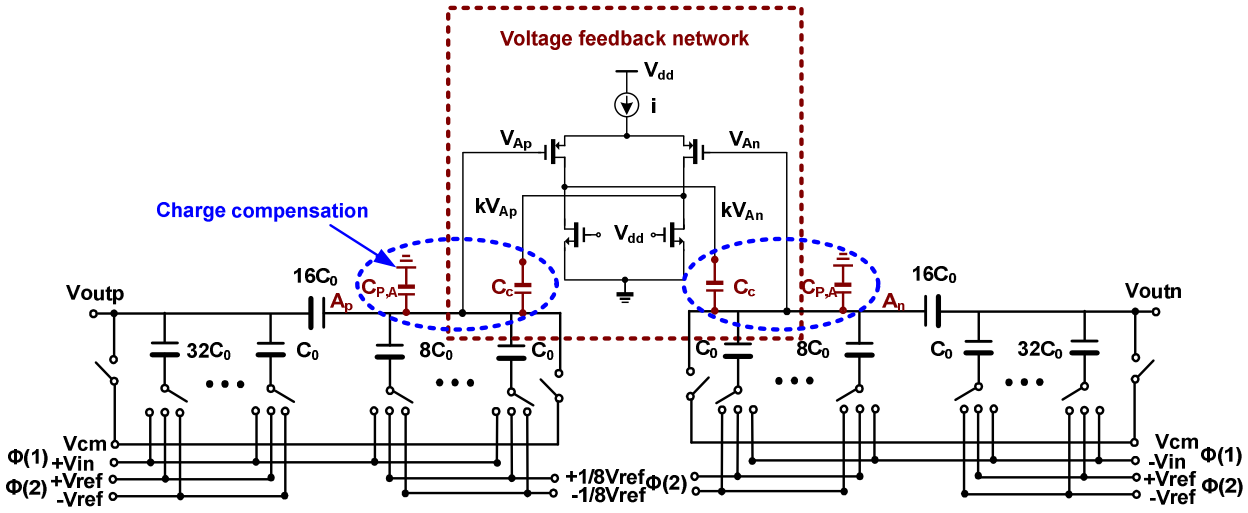

Fig.4. Differential SS DAC arrays with proposed voltage feedback network.

III. Circuit Implementation

The proposed charge compensation concept can be realized by applying an open loop amplifier and a compensation capacitor to the capacitive DAC as shown in Fig.4. The input differential pair connected to the internal nodes of the split DAC arrays can sense and amplify the internal nodes' voltages V_{Ap} and V_{An} to their output compensation capacitors C_c. The charge injected by C_c to the DACs' internal nodes can compensate the charge stored in the parasitic capacitors. Therefore, the conversion nonlinearity error due to the parasitics coupling can be corrected. The charge domain voltage feedback compensation is implemented in a 10 bit SS DAC array, and in order to minimize the voltage swing of V_A, C_{atten} is set equal to $16C_0$ and accordingly the reference voltage of the LSB array is divided by 8. In the sampling phase Φ(1), the input signals are sampled into to the differential DAC arrays of which the output nodes and the internal nodes are both reset to V_{cm}. In the conversion phase Φ(2), the differential DACs' internal node voltage V_{Ap} and V_{An} are continuously tracked and amplified to the bottom-plate of C_c through the feedback network and the comparator makes the decision after each bit settling. The ADC operates conventionally without any extra timing control to perform the charge compensation. The proposed method can also be simply utilized in a DS DAC structure which can dramatically reduce the array capacitance, whereas suffers the penalty of ever worse conversion linearity. As shown in Fig.5, the DAC array is symmetrically divided and the feedback networks are placed at the array's internal nodes. By rearranging the compensation capacitors in each internal nodes, charge compensations are attainable, thus allowing the DS architecture for high-linearity and high-speed applications.

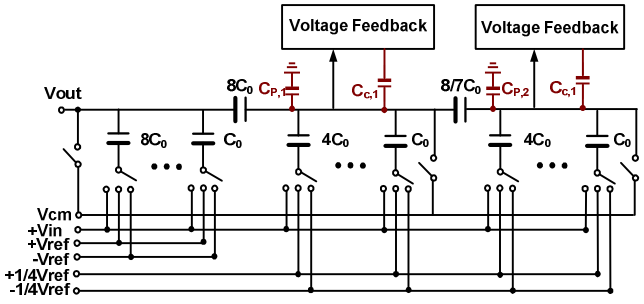

Fig.5. DS DAC array with the charge compensation method.

Considering the large voltage swing in the array's internal node, a PMOS input differential amplifier with triode-load is selected which allows the maximum output headroom for the feedback voltage generation. As mentioned, the charge compensation depends on the multiplication of the feedback factor (1-k) and the capacitance of C_c, therefore, a lower intrinsic gain with comparatively larger C_c is suggested to prevent the output swing saturation. In this design, the conventional gain-bandwidth trade-off is not critical, for the equivalent load capacitance equal to C_c // $C_{DAC,eq}$ is quite small, that allows the high-speed and low power realization for the feedback network design. ($C_{DAC,eq}$ is the output capacitance of the DAC array seen at node A and the required capacitance C_c for compensating 15% top-plate parasitic in each unit capacitor is only 30f, leads to only 6.6dB voltage gain in the amplifier)

The proposed charge compensation technique can successfully fix the DAC's conversion error with only coarse feedback network accuracy, allowing the process and mismatch variations insensitive advantages of the charge compensation method. As shown in Fig.6, the simulation result of a 10 bit SAR ADC were demonstrated where the proposed method is utilized to compensate 5% to 20% top-plate parasitics of the DAC array. The effectiveness of the charge compensation with the parasitic is depends on $(1\text{-}k)C_c$ defined in (6), and with ±15% process variations on the $(1\text{-}k)C_c$, the SNDR degrades within 3dB. That is because the DAC's conversion

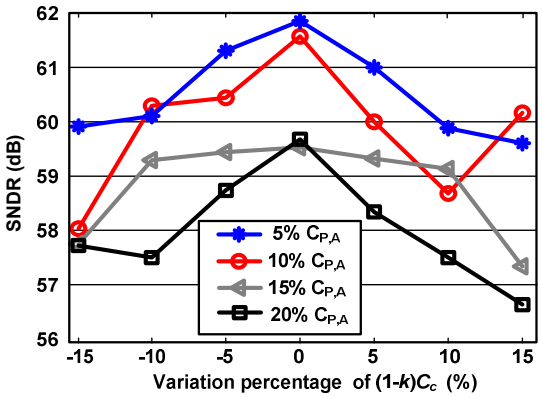

Fig.6. Simulation of SNDR versus the variation of $(1\text{-}k)C_c$ considering 5% to 20% parasitcs.

linearity will become less sensitive to the parasitic effect after the top-plate parasitics are compensated within 5%, as already illustrated in Fig.2.

IV. Simulation Results

The voltage feedback charge compensation technique is verified in both SS and DS DAC architectures in a 10-bit 80-MS/s SAR ADC with a full-scale differential input range of $0.8V_{PP}$ in 65-nm CMOS. The capacitor is implemented as a low cost MOM capacitor instead of a higher quality MiM capacitor that requires extra options. Fig.7 compares the SNDRs of both SS and DS structures with and without the proposed voltage feedback charge compensation method where 5% to 20% top-plate parasitics are considered. Fig.8 also shows the corresponding 20-time Monte-Carlo mismatch simulations of the SS DAC structure with 15% top-plate parasitics, where the ADC achieves a mean SNDR of 58dB. Fig.9 illustrates that the DNL and INL can be improved from +3LSB/-0.2LSB to 0.45LSB/-0.4LSB and +1.65LSB/-1.64LSB to +0.58/-0.74LSB, respectively. The total power consumption of the proposed feedback compensation circuitry is only 300μW.

V. Conclusions

A voltage feedback charge compensation technique has been presented, which can remove the parasitic nonlinearity effect in split DAC array. The feedback network consisting of an open loop amplifier and compensation capacitors that can successfully attain the charge compensation of the parasitic capacitors; hence solving the code-dependent nonlinearity in each bit comparison. Moreover, taking the advantage of charge domain compensation, the technique can lower the array's sensitivity to the parasitic variation and release the stringent accuracy requirement for the feedback network design. As a result, the conversion linearity of the ADC can be greatly improved with only 300μW power dissipation from the charge compensation implementation.

Acknowledgment

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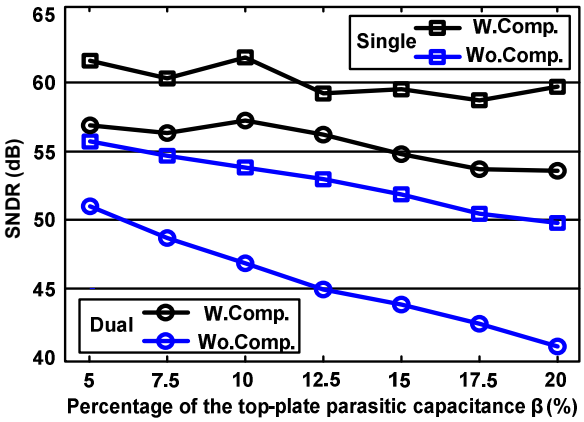

Fig.7. Simulation of SNDR versus β for both SS and DS DAC structure. (w./wo. charge compensation method)

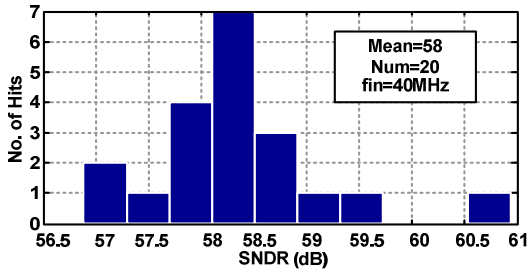

Fig.8. 20-time Monte-Carlo simulation of 10b SAR with SS DAC and 15% top-plate parasitcs.

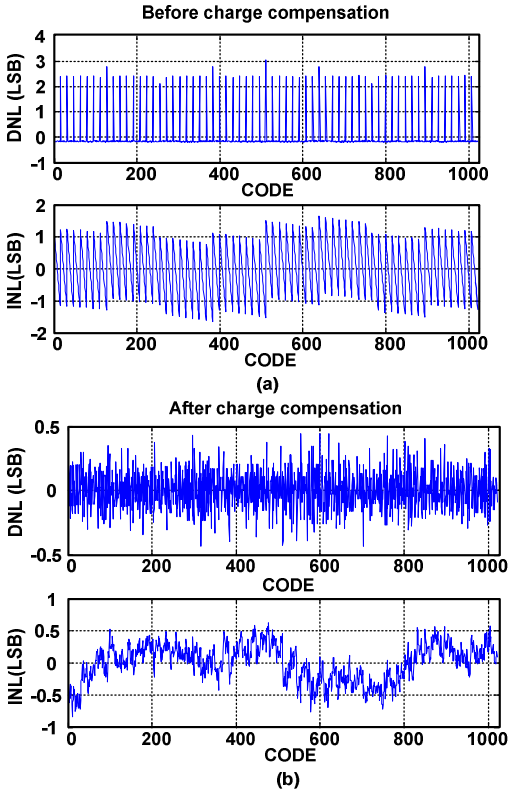

Fig.9. DNL and INL of 10b SAR with SS DAC and 15% top-plate parasitcs. (a) Before charge compensation. (b)After charge compensation