SC Biquad Filter with Hybrid Utilization of OpAmp and Comparator-Based Circuit

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***Abstract*—This paper proposes a differential switched-capacitor (SC) biquad filter exploiting a hybrid structure. The 1st active core is an operational amplifier (OpAmp) whereas the 2nd is an improved comparator-based circuit (CBC). The advantages of this new structure are justified by the reductions of power and transistor sizes. Optimized in a 65-nm CMOS process, when compared with a typical dual-OpAmp design, the proposed filter saves 19% power and 18% transistor area. The filter clocked at 40 MHz achieves 61.7-dB IM2 and 62.5-dB IM3 while drawing 2.23 mA from a 1.2-V supply. This hybrid SC biquad can gain further momentum for filters that request numerous biquads in cascade to attain higher selectivity.**

I. Introduction

Modern wireless systems such as mobile-TV tuners call for high-order baseband filters for channel selection [1]. For an 8th-order active-*RC* filter, 16 operational amplifiers (OpAmps) are required for both *I* and *Q* channels. Such a large number of OpAmp dominates the chip area and consumes significant amount of power. Entered into the sub-1V nanoscale regime, the strong channel-length modulation of fine linewidth devices and the significant reduction of voltage headroom deteriorate the area-power efficiency of OpAmps, rendering the classical OpAmp-based implementation of analog circuits no longer as efficient as it was in sub-micron scale technologies.

This paper proposes a novel differential SC biquad using a hybrid structure, attempting to halve the number of OpAmp, as shown in Fig. 1. The 1st active core is still an OpAmp whereas the 2nd is a power-and-area-efficient comparator-based circuit (CBC). It is made of a differential comparator controlling two current sources as shown in Fig. 2 [2]. It has been applied extensively in analog-to-digital converter design [3]. This work further extends the CBC structure to filter design with both new architecture and circuitry. The feasibility is validated through comparing the performances of the proposed hybrid SC biquad with a typical dual-OpAmp design.

II. Circuit Description

The schematic of the proposed hybrid SC biquad filter is depicted in Fig. 1. Its transfer function $H(z)$ is given by [4],

$$H(z)=\frac{V_o(z)}{V_i(z)}=\frac{K_3z^2+(K_1K_5-2K_3)z+K_3}{(1+K_6)z^2+(K_4K_5-K_6-2)z+1}. \qquad (1)$$

Architecturally, the key modification is that the 2nd active core is replaced by the CBC shown in Fig. 2.

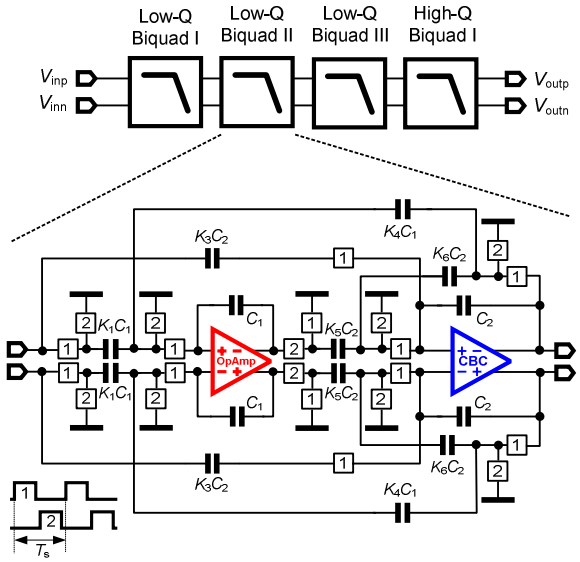

Fig. 1. Proposed SC biquad with a hybrid use of OpAmp and CBC.

OpAmp-based SC circuits are typically 2-phase networks with a sampling phase 1 and a charge transfer phase 2 (Fig. 1), which correspond in Fig. 3 to Φ_1 and Φ_2, respectively. Differently, the operation of the CBC entails 3 phases for successful operation, i.e., the sampling phase Φ_1, preset phase Φ_P and charge-transfer phase Φ_{2d}. The last two in conjunction correspond to the transfer phase Φ_2 of OpAmp-based circuits. The operation of the CBC in each clock cycle is depicted in Fig. 3.

The charge phase Φ_1 where the input voltage is being sampled is equal to that of an OpAmp-based SC circuit. In the preset phase Φ_{2P}, the output $v_{out,p}$ is preset to GND and the output $v_{out,n}$ is preset to VDD within a time duration of $t_{\theta 2P}$. This imposes that the input $v_{in,p}$ would be higher/larger than $v_{in,n}$, as represented in Fig. 3. When Φ_{2P} ends, the switches controlled by those phases are opened and the output load capacitors start to be charged linearly since Φ_{2d}. When the two input voltages of the comparator cross each other, the comparator stops the current sources and the output voltage becomes constant (and equal to that in the OpAmp-based SC circuit). Due to the finite response time of the comparator the output currents cannot be stopped instantaneously, with a time delay of $t_{d,c}$, leading to an output voltage error. However, if the response of the comparator is fast enough, that error can be minimized. The output voltage levels will then depend on the initial capacitors charge, which determines the output load capacitance charging time.

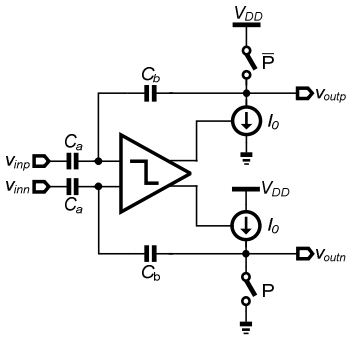

Fig. 2. Comparator-based circuit (CBC).

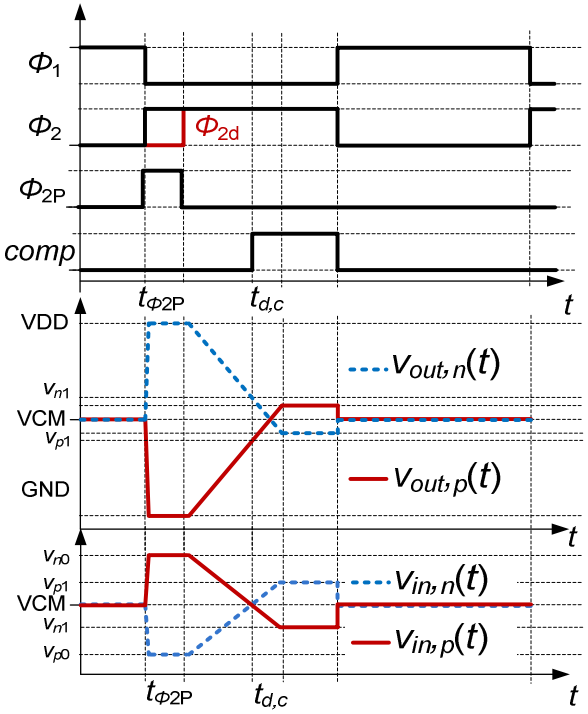

Fig. 3. Operation of the CBC in each clock cycle.

The use of two CBCs in one biquad is not recommended because of their different time responses in each cycle. In other words, when one of the CBC stops while the other is yet to be finished (and due to capacitive coupling between both outputs), the circuit that is charging will change the output of the circuit that had already stopped. By simulation, we determined that the best solution implies the replacement of the second OpAmp by a CBC. This observation also depends on the capacitor ratio set in the design.

III. Circuit Implementation and Sizing Methodology

The schematic of the OpAmp employed in this work is depicted in Fig. 4. It consists of a folded-cascode differential topology with gain boosting. The input is implemented with PMOS transistors to reduce noise. Bias and common-mode feedback circuits are not represented for simplicity. Detailed design and sizing consideration are omitted as they are extensively addressed elsewhere [5]. The focuses of this work

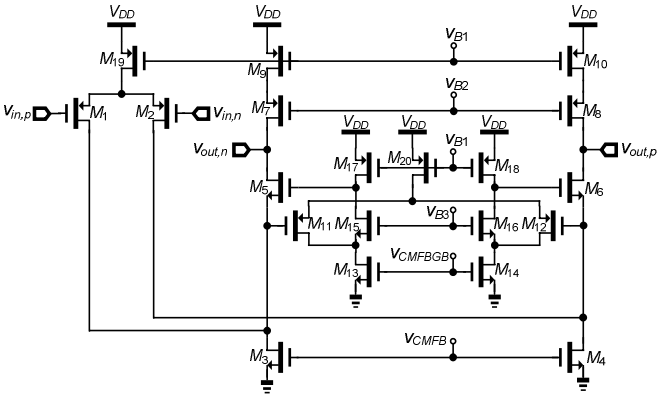

Fig. 4. Gain-boosted folded cascode differential OpAmp.

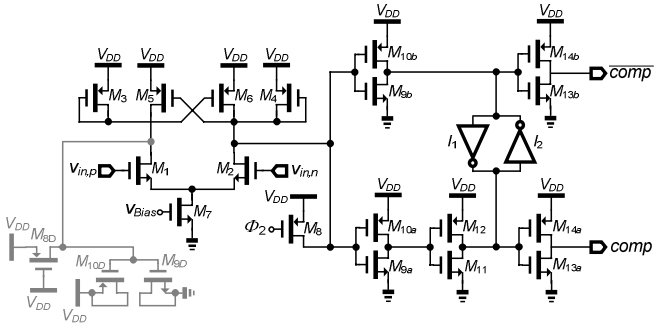

Fig. 5. Comparator schematic (dummy grey-colored part is for load balance).

are put on the design of the proposed comparator and current sources as shown in Fig. 5 and 6, respectively. New circuit design techniques are proposed next:

A. Comparator:

The comparator consists of a pre-amplifier and a positive feedback decision circuit followed by a sequence of inverter buffers to amplify the input difference to a rail-to-rail signal. In [6], the pre-amplifier and the positive feedback are implemented with NMOS transistors, connected through PMOS current mirrors. However, this implementation is not power efficient due to the different current paths of both circuits. To save power, the feedback circuit is implemented with PMOS transistors placed over the NMOS transistors of the pre-amplifier. The comparator is switched-off during the sampling phase for further power reduction. The input transistors use minimum length to minimize the input parasitic capacitance. The positive feedback uses minimum-length transistors and has an optimized ratio of 1:6 between the transistors M_3 and M_5, account the tradeoff between speed and hysteresis of the comparator. Inverters I_1 and I_2 effectively equalize the delay and improve the duty-cycle balancing of the final outputs.

B. Current Mirror:

Figure 6 shows the current sources of the proposed CBC. It features three main components: the wide-swing cascode current mirrors, the current switches (controlled by *comp* and $\overline{comp}$) and the preset phase switches (controlled by *P* and

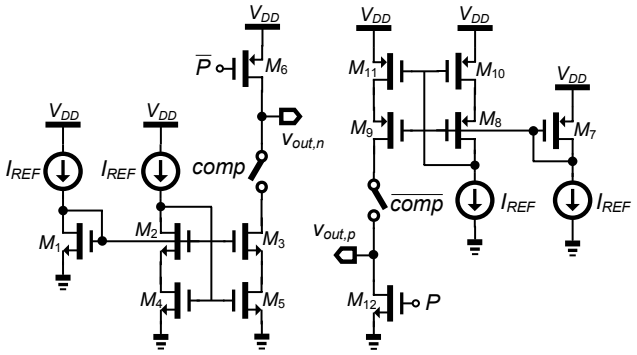

Fig. 6 Current sources of the proposed CBC.

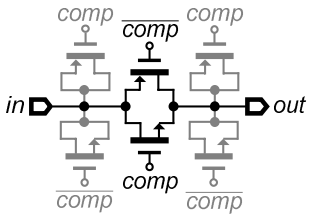

Fig. 7 Clock-feedthrough compensated current switch.

$\overline{P}$). Both current sources use high swing current mirrors, due to the large variation expected for output voltages and the importance of ensuring a constant current along that output voltage variation. Also, finite output resistance of the current mirror degrades the linearity. Their sizing is critical to ensure symmetrical current and output resistance of the differential branches for minimizing the output offset voltage. Both of them are sized with a bigger device size with non-minimal gate length to improve the matching of the current mirroring.

C. Preset Switches:

The preset switches (M_6 and M_{12}) exploit large transistors with minimum length to ensure a minimal channel resistance. This is a critical sizing since both current sources are turned on during the preset phase, to ensure that they have settled before the starting of the charge transfer phase. Otherwise, if current sources were just turned on after the preset phase, the current settling would occur during the charge transfer phase, leading to asymmetrical charging of the output load, resulting in error output voltages. Both transistor switches are clock-feedthrough compensated to reduce further the undesired output voltage variation asymmetries due to parasitic charge injections.

D. Current Switches:

The current switches, represented in Fig. 7, are both equal to improve symmetry. They are implemented with MOS transmission gates with clock feedthrough compensation. By using this structure, it is ensured that both switches have the same resistance and capacitance, improving the circuit symmetry. All transistors have minimum gate length to minimize the channel resistance. It was also studied that the possibility of implementing these switches inside the current mirrors; but this approach revealed itself to be less efficient with longer response time.

The required current value of the current sources needs to take into account several parameters before being estimated. It is necessary to know the output load capacitance C_{load}; the maximum charge time available T_C; the preset time $T_{\Phi 2P}$; the charge transfer time $T_{\Phi 2}$; and the comparator response delay time $T_{d,C}$. An estimate of the output load capacitance can be determined by analyzing Fig. 2, and is given by,

$$C_{load} \approx \frac{K_1 K_4}{K_1 + K_4} C_1 + \frac{K_3 + K_5 + K_6 + 1}{(K_3 + K_5)(K_6 + 1)} C_2 \ . \qquad (2)$$

The maximum charge time, T_C, is given by,

$$T_C \approx T_{\phi 2} - T_{\phi 2p} - T_{d,C} \ . \qquad (3)$$

Finally, the required DC current value is,

$$I_{DC} \approx \frac{C_{load}}{T_C} \Delta V \ . \qquad (4)$$

where ΔV is the maximum allowable swing, i.e. V_{DD}. It is assumed that the output voltage may swing between V_{DD} and GND.

TABLE I. PARAMETERS OF THE BIQUAD FILTER (FIG. 1).

Parameter	Value	Parameter	Value
K_1	0.455	K_5	7.292
K_3	1	K_6	6.359
K_4	0.455		
C_1	1 pF	C_2	0.75 pF

IV. IMPLEMENTATION AND SIMULATION RESULTS

The hybrid SC-biquad architecture was explored in a 1.2-V 65-nm CMOS process. Its specification is referred to one of the four biquads from an 8th-order filter for a DVB-H mobile-TV tuner [1]. The wanted –3-dB cutoff frequency (f_c) is 4 MHz, Q-factor is 0.52 and the sampling frequency (f_s) is set to 40 MHz. K_1, K_4 and K_5 are tuned to optimize the biquad behavior, since it is possible to change their values without affecting the biquad transfer function (1). The current sources values are calculated with the following assumptions: preset time equal to 5% of the clock period, i.e., 1.25 ns; (pessimistic) comparator response delay time of 2 ns; and estimation of an output load capacitance of 2 pF. Using (4), the DC current value is 250 µA. Finally, the switches from Fig. 1 are of minimum length and all have a W/L of 20/0.06 in order to minimize its resistance. All switches controlled by phase Φ_2 are implemented with transmission gates. Switches connected to the comparator input are implemented with clock-feedthrough compensation for parasitics cancelation.

The current sources of both circuits: OpAmp and CBC are switched off during the sampling phase Φ_1 for power savings. The OpAmp features a DC gain of 55 dB and a gain bandwidth product (GBW) of approximately 450 MHz, consuming an RMS current of 1.14 mA (considering power-down, and excluding biasing circuits). The pre-amplifier consumes a static current of 150 µA, and each current mirror is tuned to 250 µA. In power-down mode, the comparator

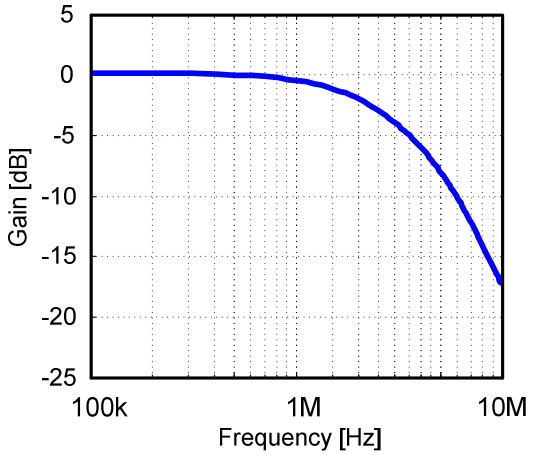

Fig. 8 Baseband amplitude response of the hybrid SC biquad at f_s= 40 MHz.

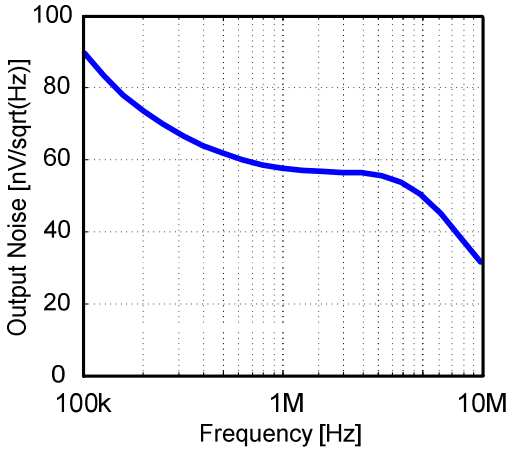

Fig. 9 Baseband noise response of the hybrid SC biquad f_s= 40 MHz.

consumes just 120 μA_{RMS}, and the two current sources together draw 400 μA. The inverters for buffering the comparator outputs were optimized to draw 200 μA_{rms}. These values again exclude the bias circuits. This totalizes a current consumption of 720 μA_{rms} for the CBC. The simulated comparator response time is 900 ps.

The baseband frequency and noise responses are shown in Figs. 8 and 9, respectively. With a cutoff frequency of 4 MHz, the achieved rejection at 10 MHz is 17.5 dB. The output noise voltage density at 1 MHz is 57 nV/√Hz.

It is of interest to compare the performances of the proposed and conventional biquads. Based on the same architecture and OpAmp, their simulated performances are summarized in Table II. The proposed low-*Q* biquad achieves 19% of power saving comparing with a typical dual-OpAmp design. For the area efficiency, the proposed CBC employs much smaller number of transistor (and size) than its OpAmp counterpart. The net area of transistors for the dual-OpAmp design is 3142.2 μm^2, but is reduced to 2583.0 μm^2 for the OpAmp-CBC hybrid design, resulting in 18% of transistor-area savings.

TABLE II. PERFORMANCE COMPARISON OF PROPOSED AND CONVENTIONAL SC BIQUAD FILTERS.

	Conventional OpAmp + OpAmp	Proposed OpAmp + CBC
IM_2	120 dB	61.7 dB
IM_3	74.9 dB	62.5 dB
Output Noise at 1 MHz	62 nV/√Hz	57 nV/√Hz
Power	2.74 mW	2.23 mW **(saved 19%)**
Net Area of Transistors	3,142 μm^2	2,583 μm^2 **(saved 18%)**
Capacitor Area	10,724 μm^2	10,724 μm^2
Total Area	13,866 μm^2	13,307 μm^2 **(saved 4%)**
Sampling Frequency	40 MHz	
-3dB Cutoff Frequency	4 MHz	
Technology	65-nm CMOS	
Order	2^{nd} (Q = 0.52)	
VDD	1.2 V	

V. CONCLUSIONS

A novel differential SC biquad filter with a hybrid use of OpAmp and comparator-based circuit (CBC) has been presented. The key advantages of replacing the 2nd OpAmp by a CBC are lower power consumption and smaller numbers of transistor and size. The linearity performance, due to the asymmetry operation of the CBC, is less competitive when comparing it with the traditional pure OpAmp-based design. Nevertheless, as verified in 65-nm CMOS, the achieved 61.7-dB IM2 and 62.5-dB IM3 are highly acceptable metrics for typical wireless applications. Due to its power (19% saving) and area (18% saving) efficiencies, this hybrid biquad can gain further momentum for filters that request numerous biquads in cascade to attain higher selectivity.

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