Comparator-Based Successive Folding ADC

U-Fat Chio, Hou-Lon Choi, Chi-Hang Chan, Si-Seng Wong, Sai-Weng Sin, Seng-Pan U, R. P. Martins

Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/en/lab/ans_vlsi/index.html)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail: alpha.ufc@ieee.org

***Abstract*—A 4-bit 1-GS/s ADC with a comparator-based successive folding (CSF) architecture is presented. Residue pre-charging and successive folding techniques are proposed for the CSF ADC to enhance quantization speed and achieve less complexity, leading to high power efficiency. Simulation results show that the ADC obtains a SNDR of 23.7 dB at Nyquist input frequency and consumes 430 µW from a 1 V supply in 65 nm CMOS, yielding a FOM of 34 fJ per conversion step.**

I. INTRODUCTION

Power effective high-speed low resolution ADCs are demanded in wireless communication applications such as UWB receivers. For a long time, flash architecture [1] is often the preferred choice as it achieves the highest sampling rates, by quantizing sampled analog input to the digital output in one transition period of parallel comparators without feedback between conversions. However, energy per conversion of flash ADC is growing exponentially while increasing the resolution, leading to be applicable in relatively low resolution (4 to 6 bit). Successive approximation register (SAR) ADC quantizes N bit by approaching feedback residue in DAC during N transition periods of single comparator, so it is generally chosen for low speed, high resolution application [2]. Accordingly, energy per conversion of SAR ADC is linearly proportional to the resolution.

To review the state-of-the-art in low resolution ADC design, several remarkable results with distinct ADC architectures were reported recently which yield low power consumption at high sampling frequency, and they always adopt the advantage of SAR ADC. The time interleaved SAR ADCs [3]-[5] had been proposed to reach speeds of 500 to 600 MS/s. The binary search ADC [6] offers the highest speed at 800MS/s. The multi-bit/step SAR ADC [7] achieves a 1.25G/s sampling rate and the highest speed of its single-channel is 625MS/s. The speed of folding ADC [8] is up to 1.75G/s. There is a common feature between them, which is to reduce number of activated comparators at each code conversion period, but operating in high speed. In other word, all of them attempt to make the energy per conversion approximately being linearly proportional to the resolution in order to enhance the power efficiency in contrast with the flash ADC.

In addition, ADC designed with efficient area and less complexity is one of significant considerations. For example, [6] simplifies the conventional binary tree connected comparators [9] from exponential branches into two comparators per bit-conversion stage, and it utilizes reference-range prediction technique to pre-charge reference voltages in data quantization path, keeping the merit of high power efficiency at high speed operation. As a result, 2^N-1 number of comparators required in the conventional N-bit ADC is reduced to 2N-1 in the modified topology. Besides the diminished area, the reduction of comparators means that the cost wasted on mismatch compensation or calibration is also reduced.

In this paper, a new comparator-based successive folding ADC architecture is reported. The proposed CSF ADC achieves high speed by residue pre-charging technique. Furthermore, successive folding technique is presented to apply only one comparator for each bit-conversion stage by co-operating with the folding switches. N comparators are employed for N-bit resolution application without any operational amplifier, thus achieving less complexity as well as high power efficiency which the energy per conversion is linearly proportional to resolution.

II. OPERATING PRINCIPLE

Fig.1 shows the circuits of a 2-bit flash ADC and a 2-bit folding ADC [8] with a range from -1 to +1. Three comparators are demanded in the 2-bit flash ADC as there are

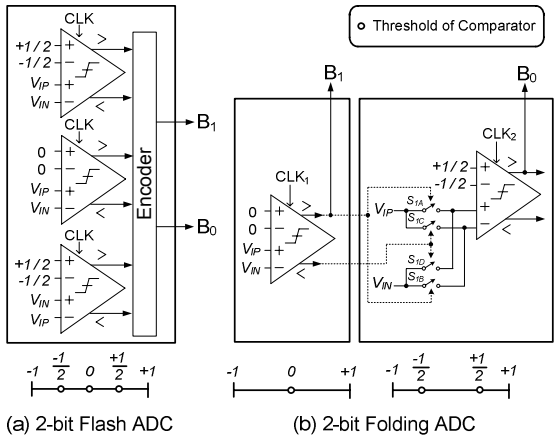

Figure 1. (a) 2-bit flash ADC and (b) 2-bit folding ADC with a range from -1 to 1.

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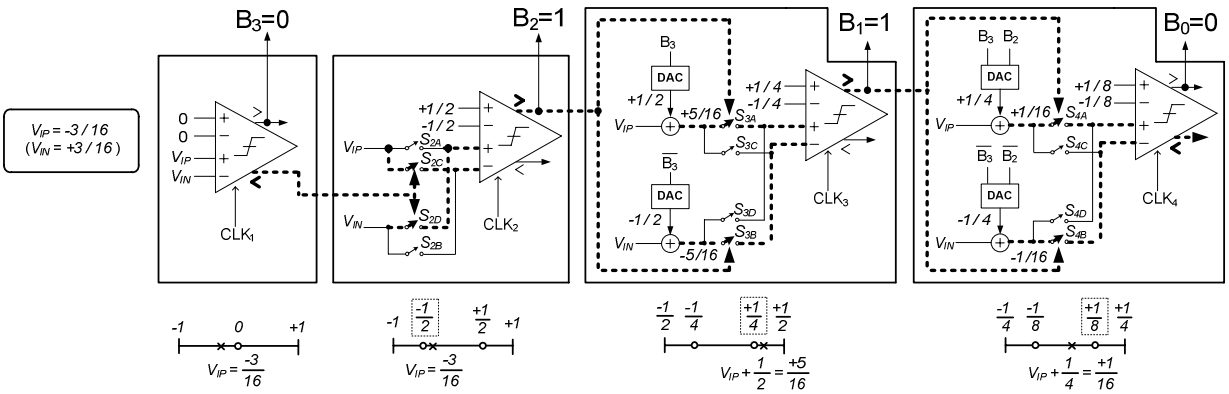

Figure 2. Operation of a 4-bit successive folding ADC, with -3/16 input on a +1 to -1 range (dashed lines indicate active path).

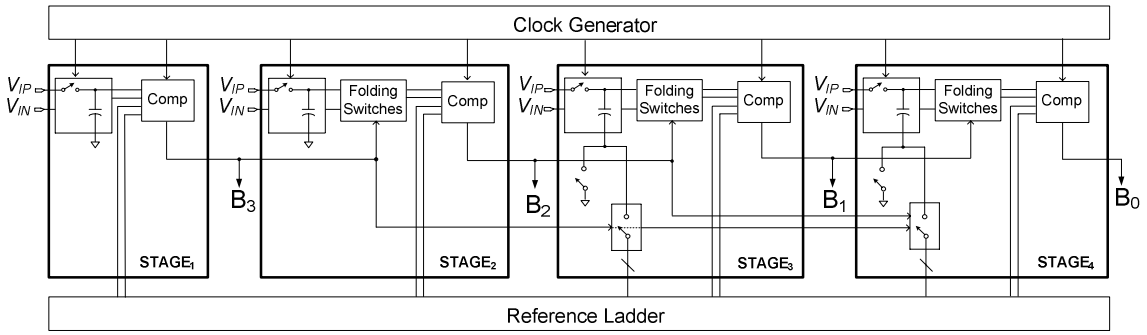

Figure 3. Implemented architecture of proposed 4-bit successive folding ADC.

3 thresholds -1/2, 0 and +1/2 to divide 4 sub-ranges, i.e. -1 to -1/2, -1/2 to 0, 0 to +1/2 and +1/2 to +1. The implement of differential comparator leads the first and the third thresholds being generated from same references -1/2 and +1/2, while the differential inputs are connected with the comparator inversely.

The 2-bit folding ADC quantizes the sampled input by two bit-stages. MSB B_1 is quantized by middle threshold (which is 0) comparator at first stage and the result of B_1 determines the connection between differential inputs V_{IP}, V_{IN} and the second bit-stage comparator. If B_1=1, then switches S_{1A} and S_{1B} turn on, so the threshold of second-stage comparator is equivalent to +1/2. Whereas B_1=0, then S_{1C} and S_{1D} turn on, and the threshold of the comparator is equivalent to -1/2. B_0 is quantized after the connection has been settled. Note that all switches keep turn-off before B_1 is quantized to avoid leakage from sampled input to the comparator. As a result, the folding ADC omits half amount of comparators in second stage to compare with the flash ADC. However, if resolution is more than 2-bit, number of activated comparators in traditional folding ADC [8] also grows exponentially with the resolution.

The operating principle of proposed CFS ADC is to extend the concept of folding [8], but combine with the characteristic of SAR ADC, which quantizes the prepared residue to the digital output bit by bit based on binary search algorithm. Fig. 2 illustrates an operation example of a 4-bit CFS ADC with a range from -1 to 1, where differential sampled inputs V_{IP}=-3/16 and V_{IN}=+3/16 are applied to the ADC. Threshold of first stage comparator is 0, which is the unique stage with immovable input connection. After MSB B_3 is quantized to 0 by the decision of first comparator, there are two actions in next two bit-stages processing at same time: *1) Switches S_{2C} and S_{2D} turn on, and then differential sampled inputs are inversely connected with second-stage comparator, so the threshold of second-stage comparator is equivalent to -1/2. 2) The differential residues +5/16 and -5/16 are produced in third stage.* At the second bit quantization B_2 is equal to 1, and there are two actions in third and fourth bit-stages simultaneously: *1) Switches S_{3A} and S_{3B} turn on, and then differential residues are directly connected with third-stage comparator, so the threshold of third-stage comparator is equivalent to +1/4. 2) The differential residues +1/16 and -1/16 are produced in the fourth stage.* At the third bit quantization B_1 is equal to 1, *which leads to switches S_{4A} and S_{4B} turn on. So, the threshold of fourth-stage comparator is equivalent to +1/8.* B_0 is equal to 1 by the fourth bit quantization. Eventually, digital output code "0110" has been quantized by 4 bit-steps.

The presented successive folding technique could apply to higher resolution application. As there is only one comparator for each bit-conversion, N comparators are employed for N-bit resolution application. Compare to [6], the CSF ADC utilizes less number of comparators but maintains the linear energy-per-conversion with resolution.

III. Implemented Architecture

The implemented architecture of the CSF ADC consists of 4 bit-stages, a reference ladder and a clock generator as shown in Fig.3. Every bit-stage is composed by passive sampling capacitors, comparator and folding switches (excluding the first bit-stage). The bit-stages sample input signal and quantizes output bits following the proposed CSF principle.

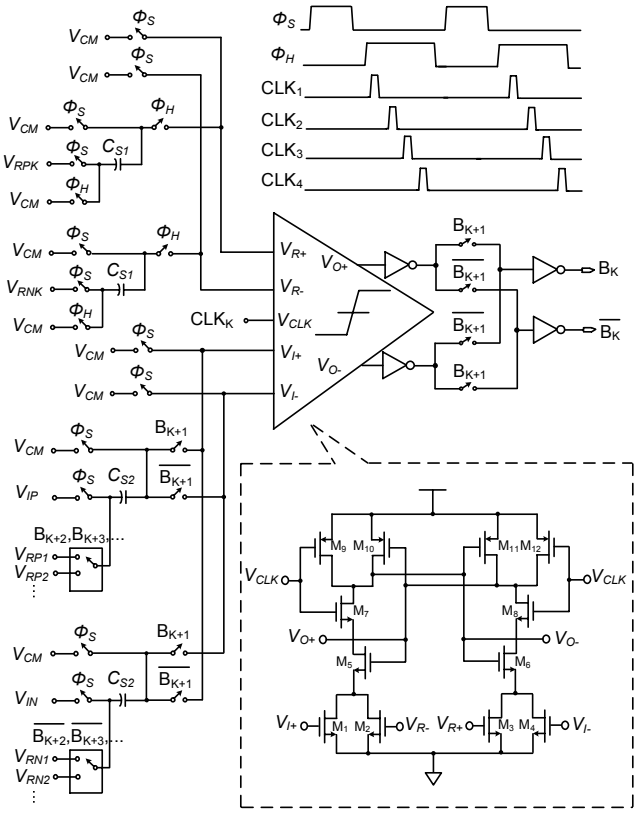

Figure 4. Switching network of K-th bit-stage.

The reference ladder provides reference voltages to the comparators and produces residue by subtraction with the sampled input in the passive sampling capacitor. The clock generator controls sample and hold phases, Φ_S and Φ_H, as well as trigger phases CLK_1 to CLK_4 of the comparators. The clock phases are shown in Fig. 4. The following sub-sections describe detail of implemented circuits.

A. Comparator

In order to achieve higher power efficiency, a four input Lewis-Gray dynamic comparator [10] has been chosen for implementation, as shown in Fig. 4. Two differential input pairs M_1, M_2 and M_3, M_4 are connected with the differential reference voltage V_{R+}, V_{R-} and sampled input V_{I+}, V_{I-} respectively. The trigger phase V_{CLK} clears the memory in regenerated output nodes V_{O+}, V_{O-}. It controls M_7, M_8 to connect the current branches of the comparator from power supply to ground. Thus, there is no static power wasted during the reset mode. As M_5 and M_6 separate the input pairs and M_7, M_8, the kickback effect produced by the V_{CLK} can be diminished during the regeneration mode.

B. Switching Network

Fig. 4 shows the switching network of K-th bit-stage. Φ_S and Φ_H are two non-overlapping clock phases operating at the proposed CSF ADC. While Φ_S is high, differential reference voltages V_{RPK}, V_{RNK} and analog inputs V_{IP}, V_{IN} of the bit-stage are sampled into the sampling capacitors C_{S1} and C_{S2} respectively. At the same time, all inputs of the comparator are connected to a fixed common-mode voltage V_{CM}, to clear the memory effect. While Φ_H becomes high, bottom plates of C_{S1} are connected with V_{CM} right away, and their top plates are connected to the inputs V_{R+} and V_{R-} of the comparator. On the other hand, top plates of C_{S2} become open and their bottom plates are connected with suitable reference voltages (V_{RP1}, V_{RP2}, …, V_{RN1}, V_{RN2}, …) provided by the reference ladder to generate the residue by the fore quantized bits $B_{K+2,}$ B_{K+3}, …. After the preceding bit B_{K+1} has been quantized, the top plates of C_{S2} connect with the inputs of comparator directly or inversely depended on B_{K+1}.

While the bit-stage comparator is activated by CLK_K and connected with the input sampling capacitor C_{S2}, the charge sharing happens between the sampling capacitor and the input parasitic of comparator, causing a gain lost. In order to compensate the gain lost of sampled input, the sampling capacitors C_{S1} and C_{S2} are designed to have same capacitance, and the switches connected to the top-plates of C_{S1} and C_{S2} are chosen to have same dimension. Finally, the reference voltages of the bit-stage suffer from the same gain as the sampled input even if charge sharing effect.

There are folding switches located at the output of the comparator. If the comparator connects with the input sampling capacitor inversely, the decision of the comparator will be inversed, hence the output folding switches also inverse the comparator output to keep the next bit-stages can obtain the correct data.

IV. Speed Considerasion

Timing definition of proposed CSF ADC is shown in Fig. 5. The settling times of the folding switches, residue pre-charging, and comparator regeneration are defined as τ_F, τ_R, and τ_L respectively. While CSF ADC is operating, activated $STAGE_K$ comparator triggers the subsequent folding switches in $STAGE_{K+1}$ and pre-charges the residue in $STAGE_{K+2}$. If $\tau_R <= \tau_F + \tau_L$ is satisfied, the latency of each bit-conversion is determined only by τ_F, the settling time of the folding switches, and exactly it is the settling time of charge-sharing occurring at the connection between sampling capacitor and the input parasitic capacitance of the comparator, as long as the residue stored in the capacitor has already settled. In SAR ADC, each bit-quantization should be processed after the residue being settled in whole capacitive DAC array, so its quantization speed is low. The residue-charging technique applied in proposed CSF ADC, leads bit-conversion latency only being the transient parasitic settling time, therefore the speed of CSF ADC could increase drastically in contract with SAR ADC.

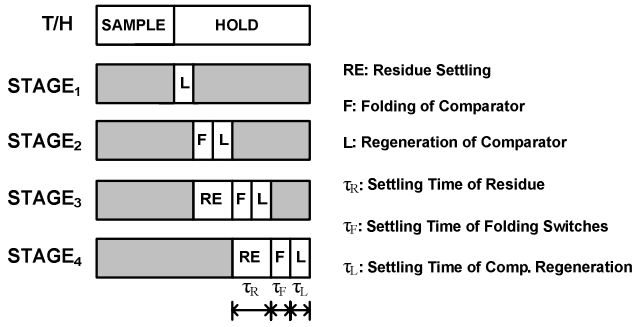

Figure 5. Timing definition of CSF ADC.

V. Simulation Results

The proposed CSF ADC has been designed in 65 nm CMOS technology. The simulation performance shows that the proposed ADC is functional up to 4-bit 1-GS/s with 1 V supply. Total power consumption is only 430 μW, while the analog and digital sections consume 290 μW and 140 μW, respectively. DNL is 0.3/-0.29 LSB and INL is 0.25/-0.23 LSB, as shown in Fig.6. Fig. 7 shows the FFT spectrum for a 1 V_{p-p} Nyquist input signal, and the peak SNDR/SFDR is 23.7/31.6 dB. Fig. 8(a) and Fig. 8(b) illustrate the SNDR versus input frequency and sampling frequency f_S respectively, and the curves show that ERBW is about 2 GHz. The Figure-of-Merit (FOM), defined as FOM=POWER/(2^{ENOB}·f_S), leads to a competitive value of 34 fJ/conversion. Table I shows performance summary and comparisons with the state-of-the-art in high speed low resolution ADC designs [1][3]-[8], and the results indicates that the overall performance of the CSF ADC achieves significant improvement.

VI. Conclusions

The 1-V 4-bit 1-GS/s comparator-based successive folding ADC designed in 65 nm CMOS process has been presented. The proposed ADC applied residue pre-charging and successive folding techniques to enhance overall performance. In the design, N comparators quantize N-bit code with transient bit-conversion latency, thus achieving high speed, less complexity, and high power efficiency.

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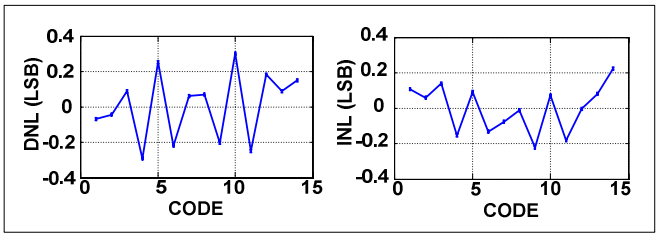

Figure 6. DNL/INL.

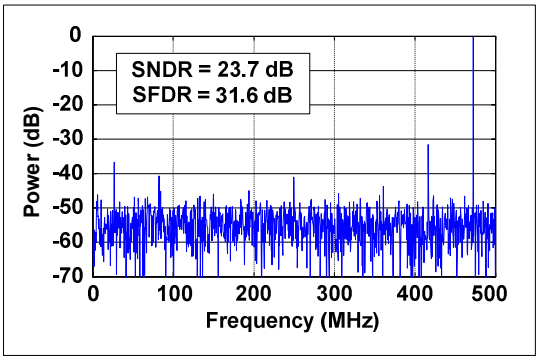

Figure 7. FFT spectrum for a 1 V_{p-p} Nyquist input signal.

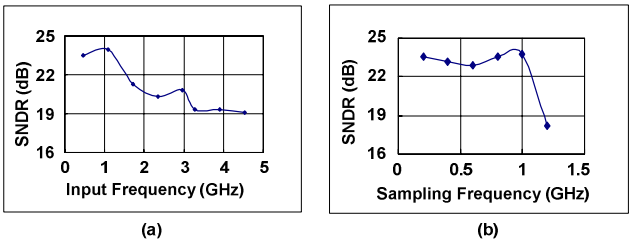

Figure 8. (a) SNDR versus input frequencies at f_S =1 GS/s. (b) SNDR versus sampling frequencies at Nyquist.

TABLE I
Performance Summary And Comparisons

	[1]	[3]	[4]	[5]	[6]	[7]	[8]	This work	
CMOS Process	90	130	180	65	65	130	90	65	nm
Resolution	4	6	5	5	5	6	5	4	bit
Speed	1.25	0.6	0.5	0.5	0.8	1.25	1.75	1	GS/s
Peak DNL	0.2	0.5	0.39	0.26	0.56	N/A	0.3	0.3	LSB
SNDR @Nyquist	23.8	32	20.2	26.1	26.9	27	28.5	23.7	dB
Power	2.5	5.3	7.8	6	2	32	2.2	0.43	mW
Supply Voltage	1.2	1.2	1.8	1.2	1	1.2	1	1	V
Input Range	0.2	N/A	0.8	0.8	1	1.2	0.8	1	V_{p-p}
FOM	160	220	1100	750	116	3050	60	34	fJ/step

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