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On-Chip Small Capacitor Mismatches Measurement Technique using Beta-Multiplier-Biased Ring Oscillator

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***Abstract*—** An on-chip capacitor mismatches measurement technique is proposed. The use of a beta-multiplier-biased ring oscillator improves the measurement sensitivity by over 6 times with respect to the state-of-the art. Experimental results using a 90 nm CMOS and thick-oxide transistors are presented. The method enables the measurement of capacitors with mismatches being as small as σ=0.04% only, and the minimum measurable capacitance can be as small 4.3fF. The results also demonstrated that better matching can be achieved with low-density capacitors.

Keywords: Capacitor mismatches measurement, ring oscillator, beta multiplier and constant gm.

I. INTRODUCTION

Accurately matched capacitors are crucial components in analog circuit designs, e.g. in Switched-Capacitor (SC) filters [1] and data converters [2]. Characterization of the mismatches in capacitors becomes important for designers in order to develop high resolution designs.

Capacitor mismatches can be measured in voltage mode [3], [4] but this technique suffers from the voltage buffer inaccuracy and kT/C noise due to the analog nature of the measurement [5], especially with small capacitors. A more accurate approach based on the frequency measurement of the ring oscillator was presented which converts the capacitance to frequency, allowing the mismatches measurement in frequency form [5]. This paper presents a high sensitivity capacitor mismatches measurement technique based on the ring oscillator biased with the beta-multiplier. The capacitor mismatches are converted to frequency mismatches with a higher sensitivity factor when compared with the method proposed in [5], which significantly increases the resolution and repeatability of the measurement. Following the Introduction this paper contains also: Section II describing the principle of the proposed capacitance to frequency conversion method based on current controlled inverters biased with beta-multiplier. Section III presenting the measurement setup and respective results, as well as the comparison with previous work. Conclusions are drawn in Section IV.

II. PROPOSED MISMATCHES MEASUREMENT TECHNIQUE

The implementation from [5] utilized a three-stage ring oscillator in differential operation, thus providing totally six inverter output nodes for loading with six pairs of capacitors-in-test. Switching of each pair of capacitors produces a shift in the overall oscillation frequency which is related to the capacitor mismatches as (for small amount of mismatches):

$$\Delta f / f = \alpha(\Delta C / C) = (\Delta C / C) / 6 \qquad (1)$$

Since totally six pair of capacitors must be used in order to have fully-balanced loaded ring oscillator, as a result, the capacitance mismatches in each pair are converted into frequency mismatches with a maximum sensitivity factor of only α=1/6 in ideal situations and this sensitivity factor will be further reduced in the presence of parasitics capacitance in the test structure. Therefore, it is desirable to raise this sensitivity factor that, in turn, increases the resolution of the measurement, subsequently making the results more immune to various types of measurement errors.

The ideal sensitivity factor can be increased to α = 1 by using the proposed ring oscillator structure, shown in Fig. 1. The oscillator utilizes three stages of differential current-

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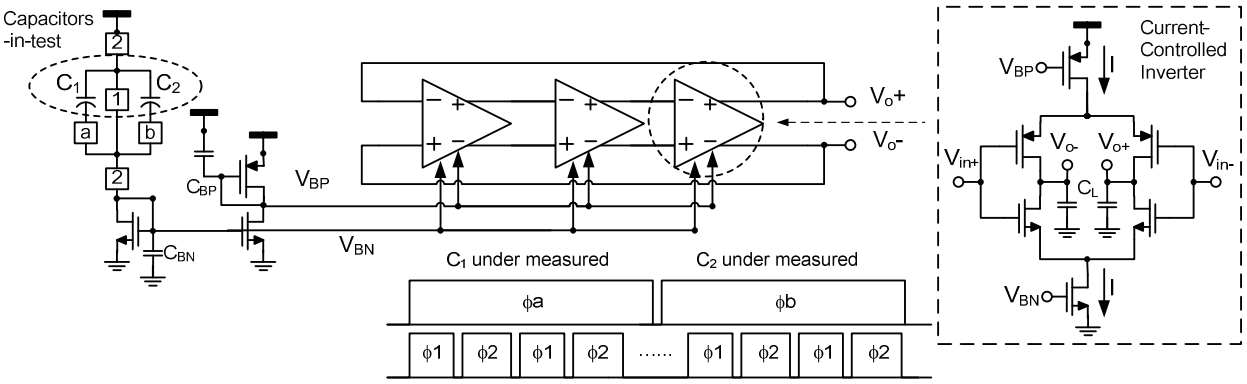

Fig. 1: Proposed capacitor mismatches measurement technique by ring oscillator with current-controlled inverters

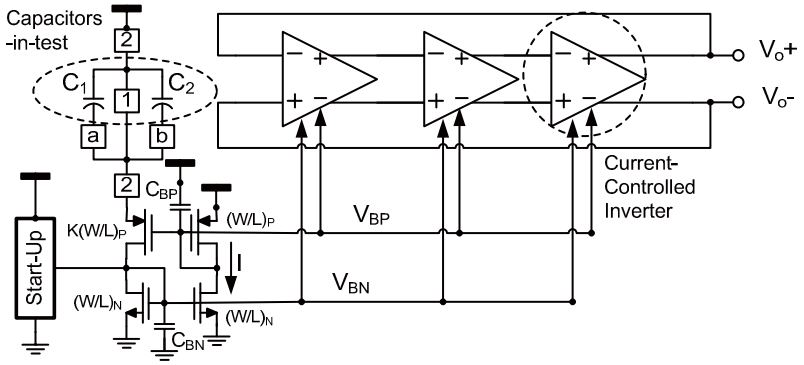

Fig. 2: The proposed beta-multiplier-biased ring oscillator (sensitivity $\alpha = 2$).

controlled inverters. The oscillation frequency is proportional to I / C_L where C_L is the load capacitor of the inverter's output and I the controlling current which depends on the switched-capacitors C_1 and C_2 under the mismatch test, driven by non-overlapping clocks $\phi 1$ and $\phi 2$. Switches a and b are used to decide which capacitors C_1 or C_2 will be utilized in the generation of the current. When the switch a turns off and b turns on, the capacitance mismatches between C_1 and C_2 will be propagated directly to the current mismatches of all inverters simultaneously and thus the oscillation frequency also exhibits the same amount of percentage shift (i.e. $\alpha = 1$). Notice that the capacitor C_L is only used to set the nominal oscillation frequency, but not the capacitor under mismatch test. C_{BN} and C_{BP} are bypassing capacitors used to filter the spikes in the SC circuit.

Notice that $\alpha = 1$ is the maximum theoretical sensitivity factor that can be achieved if the transformation between capacitance to frequency is linear. With the use of beta multiplier biasing (also known as constant-g_m biasing) technique, the ideal sensitivity factor can be further boosted to 2, as shown in the proposed circuit diagram of Fig. 2. The switched-capacitors behaved like a resistor in the beta-multiplier, and it can be shown that the bias current I is related to the capacitor C_n (n = 1 or 2) as follows:

$$I = \frac{2(f_{clk} C_n)^2}{\mu_p C_{ox} (W/L)_P} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \qquad (2)$$

where μ_p, C_{ox}, and f_{clk} are the mobility of holes, unit oxide capacitance and clock frequency of switched-capacitors C_n, respectively, and $(W/L)_P$ and K are defined in Fig. 2 also. With small mismatches the oscillation frequency mismatches can be derived as:

$$\Delta f / f = \Delta I / I \approx 2(\Delta C / C) \qquad (3)$$

revealing that the beta multiplier boost the ideal sensitivity to $\alpha = 2$ because of the quadratic transformation. The sensitivity factor is reduced in practice due to various non-idealities in the circuit, e.g. the channel-length modulation (and as a result the current source in the inverter will enter triode region during oscillation, thus reducing the effective current), as well as the parasitic capacitance in the SC circuits (from switches, as well as top and bottom plate

parasitics of the capacitors). Similarly to the measurement procedures from [5] the value of the sensitivity factor should be determined from layout-extracted simulations prior to the measurement.

It is worth to note that, small capacitors are sensitive to layout systematic mismatches, namely the one caused by the parasitics associated to the routing of the measurement circuits (e.g. associated with the clocks and control signals of the switches *a*, *b* in Fig. 2). Only 0.043fF of imbalance parasitic coupling can lead to 1% of systematic mismatches in 4.3fF capacitors. Fully balanced parasitics can be possible with careful and extensive shielding, but this will increase the overall capacitive loading of the measurement circuit which will dramatically decrease the sensitivity factor α and thus reduce the measurement accuracy. In fact, systematic mismatches (which are extractable from layout) will only create an overall measurement offset but not affecting the measurements of random mismatches (which are the most important to be measured since they cannot be extracted by CAD tools).

III. Measurement Results

Six sets of beta-multiplier-biased ring oscillators with six pairs of various capacitor structures were fabricated in a 90nm CMOS process using 2.5V thick-oxide transistors. Fig. 3 shows the die microphotograph that includes the six circuits with a total active area of 0.08mm^2. Six pairs of capacitors were fabricated including Plate (two plates of metal), Fringe and MiM (Metal-insulator-Metal) ranging from 4.3 ~ 50fF. Table 1 compares the result of our measurements with the one obtained by reference [5]. The clock frequency of the SC circuit is set in order that the oscillation frequency is in the range of 6-10MHz. Each pair of measurement circuit consumes 1.5~1.7mW depends on the sizes of the capacitors and clock frequencies. The sensitivity factors for all capacitor pairs are extracted from post-layout simulations in order to obtain correct

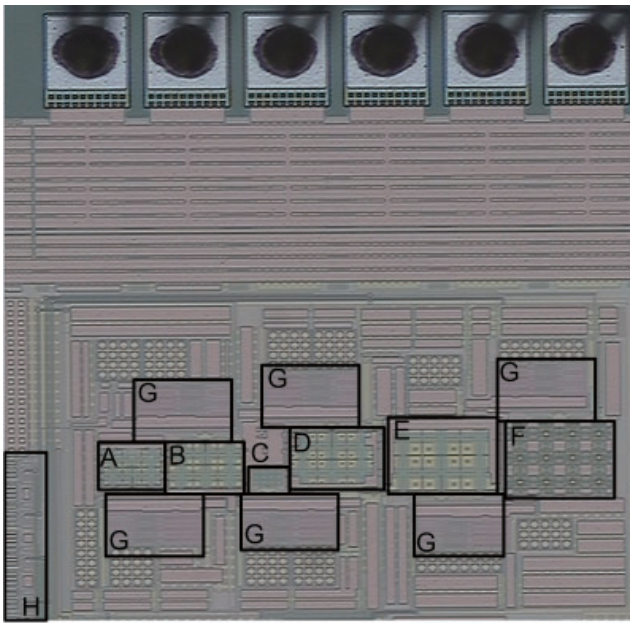

Fig. 3: Chip micrograph. Legend: A–4.3fF plate; B–10fF plate; C–10fF finger; D–20fF plate; E–40fF plate; F–50fF MiM; G–beta multiplier and ring oscillator; H–Clock generator and digital control.

mismatches measurements. The sensitivity factor is increasing from 0.53 to 1.23 with the capacitance, as the parasitics in the SC circuits degrade the sensitivity in small capacitors. The sensitivity factor "saturates" at 1.23 for larger capacitors, which is limited by the non-idealities in the ring oscillators as discussed previously. Even with such degradation over 6-fold improvement in the sensitivity factor is observed (α=0.53@4.3fF) compared with the implementation from [5] (α= 0.088@7.7fF).

The oscillation frequencies are measured using a 12-digit frequency counter (with gating time of 2s to average out the circuit and measurement noise) to obtain accurate

TABLE I
Mismatches measurement results for different types of capacitors and comparison with previous work

	This Work						Ref. [5]			
Legend (Fig. 3)	A	B	C	D	E	F				
Type	Plate	Plate	Fringe	Plate	Plate	MiM	Sandwich	Sandwich	Fringe	Fringe
Capacitance (fF)	4.3	10	10	20	40	50	7.7	15.4	23	49
Cap Area (μm x μm)	9x9	13x13	3x4	17x17	23x23	5x5	10x10	15x15	10x10	15x15
Sensitivity α	0.53	0.84	0.89	1.21	1.21	1.23	0.088	0.11	0.112	0.137
fclk (MHz)	200	95	115	70	50	40				
fout (MHz)	6.6	6	5.9	6.7	10	8.6				
$\sigma(\Delta C/C)$ %	0.24	0.09	0.25	0.04	0.05	0.15	0.1	0.09	0.18	0.31

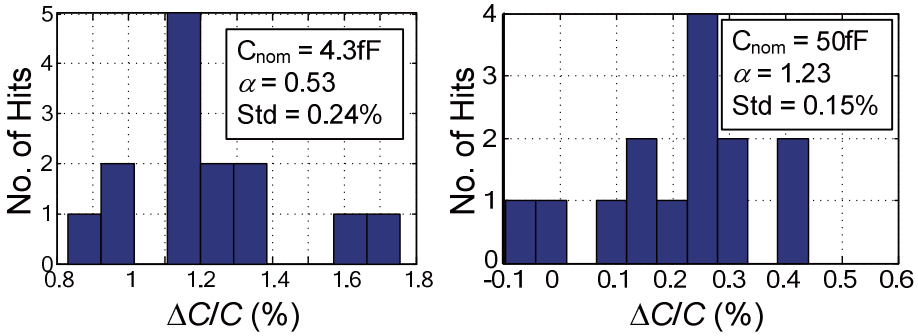

Fig. 4: Mismatches histogram of 4.3fF plate and 50fF MiM capacitors

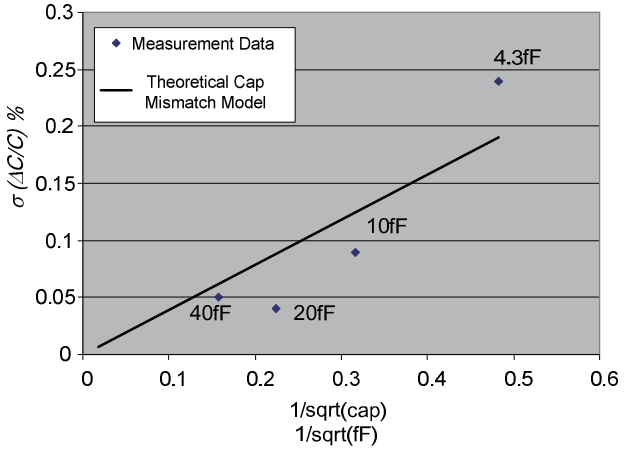

Fig. 5: Measured capacitor mismatches versus capacitance.

measurements. Each type of capacitor mismatches were measured over 14 packaged chips and the standard deviations were evaluated as shown in Table 1. As a result of increased measurements sensitivity mismatches as small as σ=0.04% could be observed. Fig. 4 illustrates the mismatches histogram of 4.3fF plate and 50fF MiM capacitors. Fig. 5 shows a plot of the measured mismatches versus 1/sqrt(capacitance) and the results demonstrated a better match with the theoretical mismatch model when compared with the results from [5], showing that increased sensitivity leads to improved predictability of the proposed capacitance mismatches measurement technique.

The results of Table 1 show that high-density capacitors (e.g. Fringe and MiM capacitors) suffer from larger random mismatches than the low-density capacitors (Plate). Indeed, small-area capacitors are more sensitive to non-uniform microscopic etching during chip fabrication. Moreover, it appears that for high-resolution applications metal plate capacitors are one of the best alternatives although trade-offs related with larger area need to be considered.

IV. CONCLUSIONS

This paper presented a high sensitivity capacitor mismatches measurement technique based on the beta-multiplier-biased ring-oscillator. By using the beta-multiplier, the ideal sensitivity can be increased from 1/6 to 2 compared with the previous work, while in practical experimental results the observed improvement is increased by 6-fold. The improved sensitivity brings advantages to the capacitor mismatches measurements, making it more immune to noise and exhibiting increased repeatability.

ACKNOWLEDGMENT

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