A Modified Charging Algorithm for Comparator-Based Switched-Capacitor Circuits

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Abstract— **This paper presents a modified charging algorithm for fully-differential comparator-based switched-capacitor (CBSC) circuits by utilizing an additional comparator to compare a variable differential threshold rather than detecting the zero crossing during coarse (E_1) transfer phase. The large overshoot in the coarse phase can be eliminated such that it relaxes the stringent trade-off between speed and accuracy, which exists in the conventional CBSC circuits. A 1.2-V Sample-and-Hold circuit implemented in 90nm CMOS process is used to demonstrate the effectiveness of this concept.**

I. INTRODUCTION

The scalability of MOSFET devices is one of the main reasons for the dominance of CMOS technology in today's semiconductor market. However, the scaled CMOS technologies introduce low intrinsic device gain which becomes one of the most challenging problems in analog and mixed-signal circuits design. To increase amplifier's gain, although the utilization of a gain-boosted amplifier stage is a straightforward solution, it has the disadvantage of reducing output voltage swing. Another alternative would be to cascade several gain stages without losing voltage swing, but it can cause instability and also increases power consumption.

Recently, a reported methodology [1]-[2] described the utilization of comparator-based switched-capacitor (CBSC) circuits to replace the op-amp in sampled-data systems. The combination of a comparator and a current source realizes the same charge transfer as an opamp-based implementation without the stability concern of high-gain and high-speed feedback loop. However, the conventional CBSC circuits suffer from the stringent trade-off between speed and accuracy [1-6]. In this paper a modified charging algorithm is proposed to increase the speed while maintaining the accuracy of CBSC circuits, and its efficiency is demonstrated with a circuit simulation in 90nm CMOS.

After this introduction a brief review of conventional CBSC circuits' structure and operation will be described in section II. The proposed modified charging algorithm will be presented in section III. In section IV, a design example and its simulation results are presented. Finally, the conclusions will be summarized in section V.

II. CONVENTIONAL CBSC CIRCUIT

A. Operation Principle

The operation of a Sample-and-Hold (S/H) with the conventional CBSC circuit during its charge transfer phase and the corresponding timing diagram are depicted in Fig.1 (a) and (b), respectively. As mentioned in [1], the CBSC circuit detects virtual ground condition only at the zero crossing instant, rather than the opamp forces virtual ground condition for the entire charge transfer phase. The charge transfer phase of the conventional CBSC circuit is mainly divided into three sub-phases: a preset phase (P), a coarse charge transfer phase (E_1), and a fine charge transfer phase (E_2) [1].

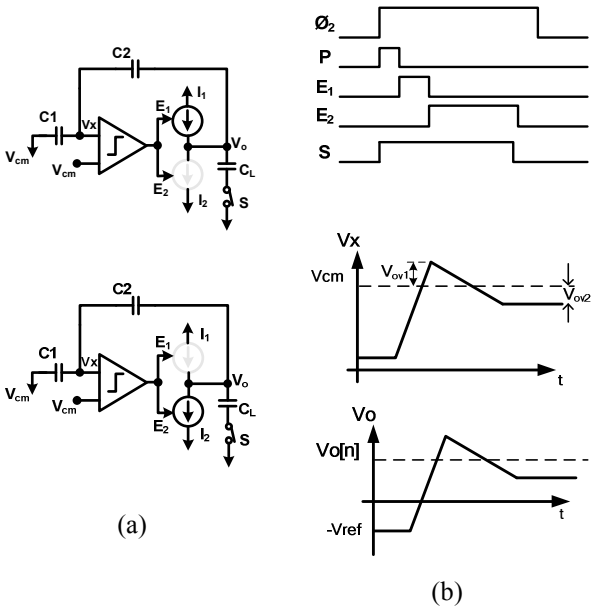

Fig. 1: A S/H with the conventional CBSC circuit. (a) Charge transfer circuit (b) Timing diagram

The short preset phase (P) ensures that the voltage V_x starts below the virtual ground condition V_{cm}. In the coarse transfer phase (E_1) a greater current source I_1 is used to charge up the capacitors

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network (C_1, C_2 and C_L) and obtain a fast, rough estimate of the output voltage and virtual ground condition. In the fine transfer phase (E_2), a smaller current source I_2 is used to discharge the capacitors network and recover from the coarse phase overshoot. It is also used to get a more accurate value for the virtual ground condition and the output voltage. When the comparator detects the second zero crossing, the sampling switch S is opened. This defines the sampling instant and locks the sample charge on the load capacitance C_L.

B. Speed and Accuracy

As derived in [2] the equivalent opamp based open-loop gain A_o and the input referred offset voltage V_{os} for CBSC circuits are given by

$$V_{os} = \frac{\beta \cdot I_{2o}}{C_E} t_d \quad \text{.....(1)}$$

$$A_o = \frac{C_E R_o}{\beta \cdot t_d} \propto \frac{1}{I_{2o}} \quad \text{.....(2)}$$

C_E is the net capacitance that the current source I_2 is charging, t_d is the comparator delay, R_o is the finite output resistance of the current source I_2 and β is the feedback factor of the capacitors network. From the equations (1) and (2), the performance of CBSC circuits will be degraded when the magnitude of the fine phase current increases.

Fig. 2 illustrates the stringent trade-off between speed and accuracy presents in the conventional CBSC circuits. When its operation speed is increasing the coarse transfer phase current I_1 and the overshoot V_{ov1} will also increase. In order to recover from the large overshoot V_{ov1} and, to guarantee that the fine transfer phase finishes before the end of the operation period, the fine phase current I_2 should increase leading, consequently, to a reduction in accuracy. Therefore, the large overshoot V_{ov1} is the main barrier to increase speed while maintaining accuracy in the conventional CBSC circuits.

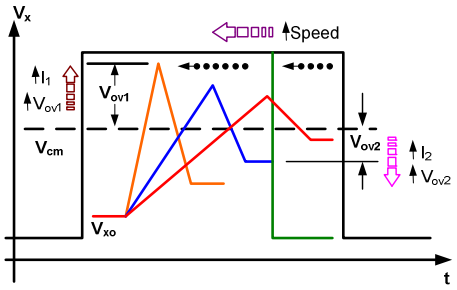


Fig. 2: Relationship between speed and accuracy in conventional CBSC circuits.

III. MODIFIED CHARGING ALGORITHM

The circuit schematic of a CBSC gain stage with the proposed modified charging algorithm implemented with a fully-differential topology [3],[7] and the corresponding timing diagram during the charge transfer phase are depicted in Fig. 3 and Fig. 4 respectively. As compared to the circuitry of conventional CBSC circuit, an additional comparator (K_1) [5] with a variable differential threshold voltage (V_{cp_tr}) is utilized. Moreover, both coarse (I_1) and fine (I_2) phase currents operate in the same direction.

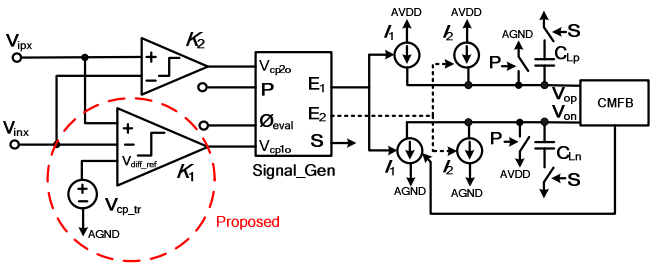


Fig. 3: *Modified charging algorithm* – Circuit schematic of the CBSC gain stage.

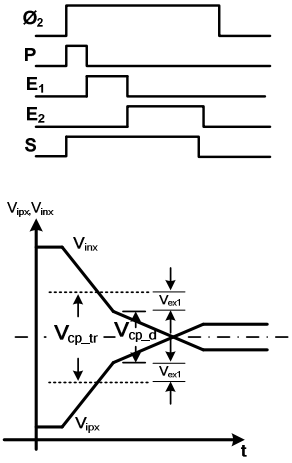


Fig. 4: *Modified charging algorithm* – Timing diagram in the charge transfer phase.

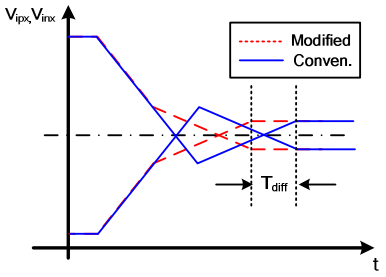
The proposed algorithm includes three sub-phases in the entire charge transfer phase: a preset phase (P), a coarse transfer phase (E_1) and a fine transfer phase (E_2). A brief preset phase (P) ensures that the differential input voltage is always negative ($V_{inx} > V_{ipx}$), as depicted in Fig. 4. When the coarse transfer phase begins, the current I_1 charges V_{op} and discharges V_{on}, respectively, until the comparator K_1 detects that the differential input (V_{inx}-V_{ipx}) is lower than its differential threshold voltage V_{cp_tr} , and changes its state turning off the current I_1. The delay of the comparator K_1 and the high ramp rate of current I_1 generate the excess voltage V_{ex1} so that the fine transfer phase begins at a smaller voltage level V_{cp_d}, as indicated in its timing diagram. The magnitude of the differential threshold V_{cp_tr} must be adjusted to guarantee the differential input will not cross each other at the end of the coarse phase. In the fine transfer phase, a smaller current I_2 continues to charge (discharge) the output until the comparator K_2 detects the zero crossing ($V_{ipx} > V_{inx}$). The comparator K_2 changes its state to turn off I_2 and the sampling switch S is also opened. This defines the sampling instant and locks the sample charge on the load capacitance $C_{L,p,n}$.

In the proposed algorithm, by comparing to a non-zero differential threshold rather than detecting a zero-crossing during the coarse transfer phase, the large overshoot V_{ov1} which limits the speed or accuracy in the conventional algorithm can be eliminated. Without the need to recover from the large overshoot generated in the end of coarse transfer phase, it eases the fine transfer phase current to satisfy both requirements of speed and accuracy.

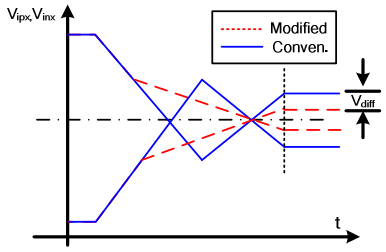
Fig. 5 (a) and (b) illustrate the comparison between conventional and proposed algorithms for CBSC circuits during the

charge transfer phase with two different circumstances: (a) is same accuracy and (b) is same operation speed.

For the case (a), the comparison is based on the following conditions in both algorithms: i) the slew rate during coarse (E_1) transfer phase is equal; ii) the fine transfer phase (E_2) starts at the same voltage level; iii) the slew rate during fine (E_2) transfer phase is equal. The conditions for case (b) are same as that of case (a) except the slew rate during the fine phase is not equal for both algorithms. As a result, either a faster operation speed or higher accuracy could be obtained when the proposed modified algorithm is adopted.



(a) Same accuracy



(b) Same operation speed

Fig. 5: Comparison of the performance between conventional and proposed algorithms with two circumstances: (a) Same accuracy (b) Same operation speed

IV. DESIGN EXAMPLE

A. *Sample-and-Hold*

A fully-differential S/H is depicted in Fig. 6. Its CBSC gain stage incorporates with both conventional and proposed modified algorithms. The capacitors network include C_1 =$C_{Lp,n}$ =1pF and C_2 =2pF.

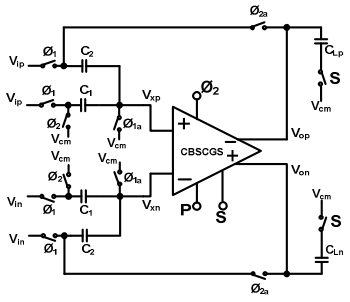


Fig. 6: An S/H incorporating the conventional and modified CBSC circuits.

In this case, the comparison between the two algorithms is under the circumstance of same operation speed. The voltage amplitudes at input terminals (V_{xp} and V_{xn}) of the CBSC gain stage incorporated with both algorithms during the charge transfer phase is depicted in Fig. 7. The transistor-level simulation result (Fig. 7) is obtained by CADENCE-Spectre simulator 90nm CMOS technology. Both cases of the coarse phase current are equal, but the fine phase current of the proposed algorithm is approximately 4x smaller than the conventional. A comparison of S/H features when incorporating either the conventional or the modified charging algorithm is summarized in Table 1. The output spectrum of S/H circuit with the proposed algorithm is depicted in Fig. 8. The simulation result is tested with an input signal of *fin* = 13.75 MHz and 0.6-Vpp differential swing. The output spectrum shows a THD of -68.3 dB and it is evident that the proposed algorithm can be adopted in switched-capacitor circuits to provide better than 10-bit linearity.

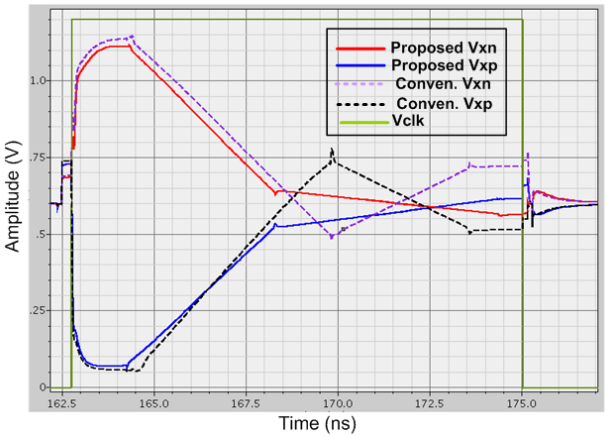


Fig. 7: Voltage amplitudes at the input terminals (V_{xp} and V_{xn}) of the CBSC gain stage incorporated with proposed and conventional algorithms during the charge transfer phase.

Table 1: Comparison of the S/H features with conventional or modified charging algorithms

S/H Features	Charging Algorithm	
	Conventional	Modified
Operating frequency	40 MHz	40 MHz
Coarse phase current	400 µA	400 µA
Fine phase current	200 µA	45 µA
Residual input voltage (V_{xp} - V_{xn}) at the beginning of fine transfer phase	236.5 mV	110.7 mV (*)
Overshoot V_{ov2} at the virtual ground (V_{xp} - V_{xn})	206.3 mV	51.8 mV

(*) – The differential threshold voltage is 320 mV.

B. *Effect of Process Variation*

The overshoot voltage $\left(V_{ov} = \frac{I_{ch}}{C} t_d\right)$ and the slew rate $\left(\frac{I_{ch}}{C}\right)$ depend on three parameters: the charging current source, the

net capacitance the current is charging and the comparator delay. Under process variation, the charging current is insensitive to it but the capacitance and the comparator delay both vary widely. Therefore, the performance of CBSC circuit can be affected significantly by process variation. In the proposed algorithm the variation of the excess voltage V_{ex1} in the coarse transfer phase is clearly a reason for concern, because a too large excess voltage could cause the residual differential input to cross each other in the end of the coarse phase. The variation of the charging speed during the fine phase is another issue to be addressed because the decreased slew rate may lead to the incompletion of the fine transfer phase before the end of the operation period.

The comparison of CBSC circuits' performances (voltage amplitude) with modified algorithms, using a typical circuit model or under process variation is summarized in Table 2. Under process variation the combination of 'min' (capacitor) and 'SS' (transistor) would cause the fastest slew rate and the largest comparator delay, hence the largest overshoot in the coarse phase could be obtained. On the other hand, the combination of 'max' and 'FF' would lead to the slowest charging speed and the largest residual input voltage for the fine transfer phase. Therefore, these two extreme combinations are more considerable under process variation.

As it can be extracted from Table 2 the fine transfer phase current is slightly increased to 70 µA under the effect of process variation, but it is still 3x less than the conventional. Besides, the proposed algorithm's overshoot V_{ov2} in the worst case is about 130 mV less than the conventional.

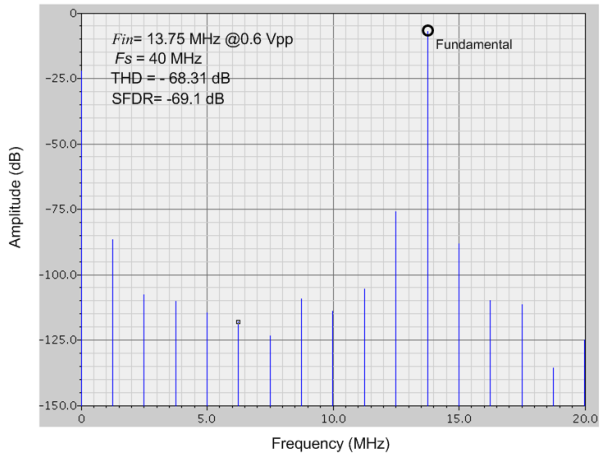


Fig. 8: Output spectrum of the S/H circuit with the proposed algorithm.

V. CONCLUSIONS

A modified charging algorithm for comparator-based switched-capacitor circuits has been presented. In contrast with the detection of zero crossing during coarse transfer phase as in the conventional algorithm, the proposed algorithm utilizes an extra comparator to detect a non-zero differential threshold in order to eliminate the large overshoot generated at the end of the coarse phase. In consequence it significantly enhances the capability of charging current in the fine transfer phase satisfying both requirements of speed and accuracy. The simulation of the S/H circuit, in 90nm CMOS, shows that the fine phase current of the proposed algorithm is about 4 times less than the conventional under the same operation speed, demonstrating the effectiveness of this algorithm.

Table 2: Comparison between typical model and under process variation.

Charging Algorithm	Modified			Conventional
Operating frequency	40 MHz	40 MHz	40 MHz	40 MHz
Coarse phase current	400 µA	400 µA	400 µA	400 µA
Fine phase current	70 µA	70 µA	70 µA	200 µA
Capacitor Model	min	typ	max	typ
Transistor Model	SS	TT	FF	TT
Residual differential input at the beginning of fine phase	58.6 mV	110.7 mV	159.4 mV	236.5 mV
Overshoot V_{ov2} at the virtual ground (V_{xp} - V_{xn})	72.7 mV	68.2 mV	53.4 mV	206.3 mV

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