A 90nm CMOS Bio-Potential Signal Readout Front-End with Improved Powerline Interference Rejection

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ABSTRACT

This paper describes a 90nm CMOS low-noise low-power biopotential signal readout front-end (RFE). The front-stage instrumentation amplifier (IA) features a chopper; an AC-coupler and a novel chopper notch filter for minimizing the dc-offset; transistors' flicker noise and 50Hz powerline interference concurrently. A noise-aware transistor selection (thin- and thick-oxide) in the IA enables a flexible tradeoff between noise and input impedance performances. The 2nd stage is a spike filter clocked by a parallel use of two non-overlapping clock generators, effectively tracking and suppressing the chopper spikes. The last stage is a gain-bandwidth-controllable amplifier for boosting the gain and alleviating different bio-potential signal measurements through simple digital controls. Simulation results showed that the RFE is capable of tolerating a differential electrode offset up to ±50mV, while achieving 140dB CMRR and 51.4nV/√Hz input-referred noise density. The notch at 50Hz achieves 41dB rejection. The entire RFE consumes 16.55 to 35.5µA at 3V.

1. INTRODUCTION

Measuring bio-potential signals, such as Electroencephalogram (EEG), Electrocardiogram (ECG), and Electromyogram (EMG) against various contaminating signals in portable biomedical monitoring systems is of great challenge in minimizing the power consumption while maintaining a high performance. The characteristics of EEG, ECG, EMG and the contaminating signals (i.e., flicker (1/*f*) noise, electrode offset and powerline interference) are given in Table I. The primary role of the readout front-end (RFE) is to extract those bio-potential signals out while rejecting others that contaminate the information. In the literature, a 0.5µm CMOS RFE compatible with EEG, ECG and EMG has been reported [1]. However, no powerline filter was implemented in that work. Experiments have shown that powerline interference couplings can strongly affect the quality of measurements. A low-pass notch filter for EEG system is presented in [2], but it is not capable for ECG and EMG measurement due to its low-pass characteristic. In this paper, a 90nm CMOS low-power, low-noise and high-common-mode rejection ratio (CMRR) RFE utilizing a novel chopper notch filter for powerline interference rejection is described. The block schematic of the entire system is shown in Fig. 1. The employed 90nm CMOS process not only offers high-quality area-efficient passives (e.g., MiM capacitor and high-resistive polysilicon), but also thin and thick-oxide transistors that help optimizing the circuit performance. The supply voltage (V_{DD}) is 3V for the RFE to facilitate the circuit design. For the back-end digital circuitry, 1V thin-oxide transistors have the direct advantages of smaller feature size and lower power consumption.

2. ARCHITECTURE OF THE RFE

As depicted in Fig. 1, the input stage of the RFE is a differential instrumentation amplifier (IA). Its gain is determined by the ratio of two resistors for robust gain accuracy over process and temperature variations. In this way, a high CMRR can also be achieved without precise resistor matching as in conventional three-stage OpAmp counterparts [3]. The 1/*f* noise and electrode offset are suppressed by concurrent adoption of AC-coupling and chopper stabilization. A new

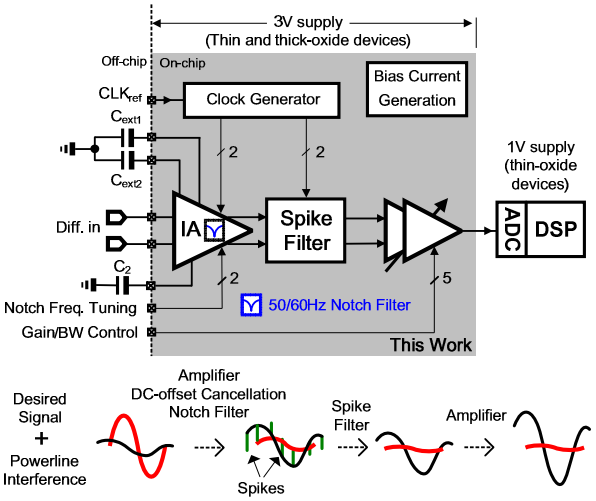

Fig. 1. Proposed bio-potential signals acquisition system.

Table. I. Bio-potential signals and the nearby contaminating signals [1]

	Bio-Potential Signals			Contaminating Signals		
	ECG	EMG	EEG	Flicker Noise	Electrode Offset	Powerline Interference
Freq. (Hz)	< 10^2	< 10^3	< 10^2	< 10^3	< 10^0	50 / 60
Amp. (µV)	< 10^4	< 10^3	< 10^2	10^{-1} – 10^1	10^{-1} – 10^4	10^3 – 10^4

chopper notch filter is merged inside the IA to eliminate the powerline interference. Spikes generated by the chopper are suppressed by applying a track-and-hold-like spike filter. Its spike-tracking clock is formed by a novel parallel operation of two non-overlapping clock generators. The last stage is a gain-BW-controllable amplifier, which also transfers the differential signals to single ended for the back-end analog-to-digital converter (ADC).

3. INSTRUMENTATION AMPLIFIER (IA)

Figure 2 shows the schematic of the IA that is designed to offer 10V/V voltage gain. Various circuit techniques are applied to improve the performances of the IA. Firstly, in order to remove the 1/*f* noise, the chopper modulates the input signal to a higher frequency where 1/*f* noise is negligible, and then demodulates it back to the baseband after amplification and filtering [4]. The second technique is AC-coupling (Fig. 2 left). The output voltage before passing through the demodulating chopper has a frequency spectrum as indicated in S_1, which contains the electrode offset at odd harmonic components, and the IA dc-offset at DC. OTA_2 with low-pass cut-off frequency f_p, extracts the DC components and converts them into the frequency spectrum S_4. On the other hand, the chopped output voltage with frequency spectrum S_2 will be filtered by OTA_1 and then modulated again to become the frequency spectrum S_3. As a result, two voltage signals contain only the electrode offset and IA offset will pass through the transconductance stages (gm_1 and gm_2). They will convert the voltage signals into current signals and negatively feedback to the

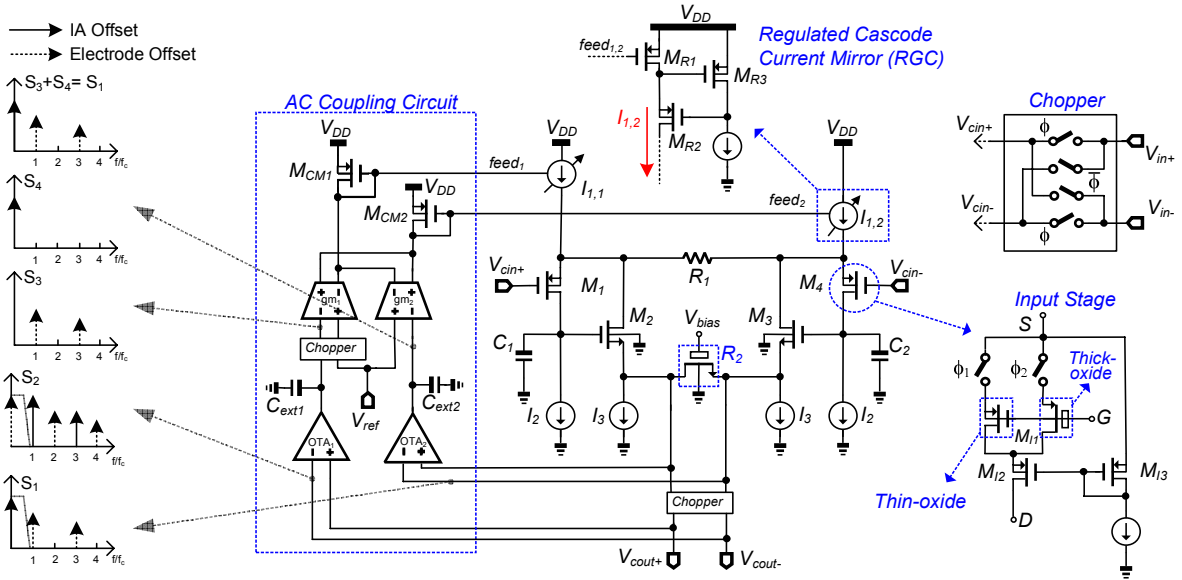

Fig. 2. Schematic of the IA including the AC-coupling circuit, regulated cascade current mirror (RGC), input stage and chopper.

regulated cascode current sources (RGC) [5]. The feedback current will combine at R_1 and reform a spectrum same as S_1. Therefore, the electrode offset and IA offset can be cancelled at the same time. Moreover, in order to reduce the residual offset causes by clock feedthrough and charge injection, the switches of the choppers are implemented by complementary devices with proper matching. The common-mode feedback circuit of the IA is not specified in the figure, which is implemented by using two differential pairs and will feedback to the gate of the current sources I_2.

The transfer function of the IA given in (1) shows its highpass filter characteristic and indicates that the gain is expressed as a ratio of R_2/R_1, where f_p is the low-pass cut-off frequency of the IA and gm is the transconductance of the AC coupling feedback circuit.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1}\frac{s+2\pi f_p}{s+A_{OTA}\,gmR_2(2\pi f_p)} \quad , \qquad (1)$$

The input-referred noise power spectrum density (PSD) of the IA is analyzed and given as follows,

$$\overline{v_{in,IA}^{\,2}} = \frac{16kT}{3}\left[\frac{1}{gm_{M1}}+\frac{1}{A_v^{\,2}gm_{M2}}+\frac{3}{4}\left(\frac{1}{g_1}+\frac{1}{A_v^{\,2}g_2}\right)+\frac{(2gm_{I1}+gm_{I3}+gm_1+gm_2)}{g_1^{\,2}}+\frac{gm_{I2}}{(g_1 /\!/\, gm_{M1})^2}\right] , \qquad (2)$$

where A_v is the gain of the IA, g_1 and g_2 are the reciprocal of R_1 and R_2 (where R_2 is tunable), gm_{I1}, gm_{I2}, gm_{I3} are the transconductance of the current sources, and the transconductance of M_{CM1} and M_{CM2} are set to gm_{I1} as they have the same current mirror ratio. The $1/f$ noise components are neglected in (2) since they are expected to be eliminated by the chopping technique. Equation (2) also states that the noise can be reduced by operating the input-transistor pairs in weak inversion by enlarging their sizes, and to bias the current source transistors in strong inversion through reducing their sizes.

In operation, the electrode offset and the differential signals presented at the gate of the input transistor pairs (M_1 and M_4) and drain of the current sources, $I_{1,1}$ and $I_{1,2}$, will modulate their output transconductance, resulting in degradation of CMRR. To overcome this issue, RGC is applied at $I_{1,1}$ and $I_{1,2}$, and current-balancing technique [1] is applied at M_1 and M_4, such that the drain-to-source voltage of M_{I1} can be made independent to the input DC level.

One leading advantage of 90nm CMOS process is the availability of both thin and thick-oxide transistors, opening up more possibilities to improve the IA's noise performance. In transistor selection, thin-oxide transistors are exploited to implement the transistors M_1 to M_4 and the current sources of the IA. To ensure there is no reliability issue, thick-oxide transistors are selected for implementing the rest components of the IA and the latter stages of the RFE. The transconductance of M_1 to M_4 (gm_{M1} for M_1 and M_4, gm_{M2} for M_2 and M_3) is generally given by $gm_{M1,M2} = \mu_n C_{ox}(W/L)(V_{gs}-V_{th})$, where thin-oxide transistor has a higher gate oxide capacitance per unit area (C_{ox}). For the same drain current, the amount of decrease at $(V_{gs}-V_{th})^2$ will be the same as the increase of C_{ox}. Therefore, $gm_{M1,M2}$ will have a factor of $(V_{gs}-V_{th})$ increment and the input-referred noise can be reduced according to (2). On the other hand, thin-oxide transistors also have a lower threshold voltage for enhancing the overdrive voltage, thus more voltage headroom can be provided for the sizes' reduction of the current sources transistors and $gm_{I1,I2,I3}$ can be degraded.

Figure 3 shows the input-referred noise level has a 10% reduction after applying the proposed transistors combination. Besides, smaller value of K/C_{ox} offered by thin-oxide transistors may also provide a lower $1/f$ noise according to the $1/f$ noise general equation $(v_{in,flicker}^{\,2})_{RMS} = K/[C_{ox}(WL)f]$, where K is the gain factor of the

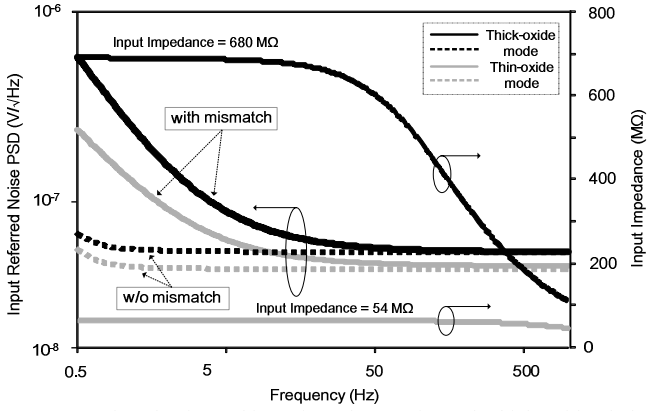

Fig. 3. Input-referred noise and input impedance using only thick-oxide (dark) or combination of thin and thick-oxide (light) transistors by mode switching at the input stage.

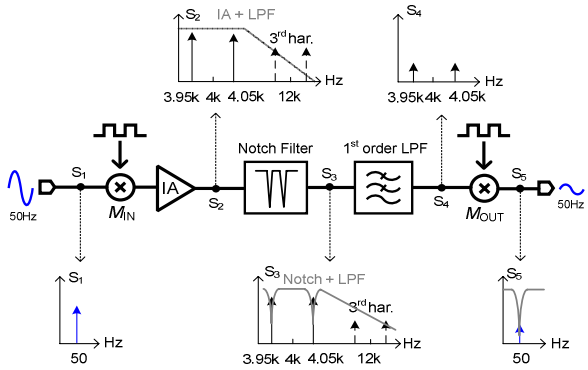

Fig. 4. Principle of the proposed notch filtering system.

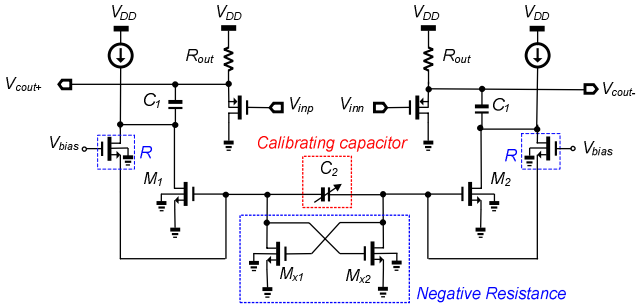

Fig. 5. Proposed notch filter (require two to reject at 3.95 and 4.05 kHz).

particular transistor. According to Fig. 3, the reduction of *1/f* noise is not significant after chopping technique is applied. However, if the precision of the chopper modulating clock is impaired due to transistors mismatch, the improvement of the proposed circuit will become obvious.

However, a common problem for using thin-oxide transistors is that the input impedance of the IA will be lowered, as shown in Fig. 3 (right axis). Typically, such an input impedance level will not significantly affect the quality of the signal acquisition, but a mode switching technique has been applied at the input pair of the IA to provide a flexible tradeoff between noise and input impedance (Fig. 2 right). As the input impedance mainly depends on M_{I1}, this technique provides the simplest way for switching the required input impedance and noise level to befit the use in different kinds of measurement.

4. CHOPPER NOTCH FILTER

Powerline interference is a strong noise source which can be easily picked up through the electrode cables, electrical system and the person being monitored [6]. In order to reduce this interference, a tunable chopper notch filter is adopted. Unlike the conventional low-frequency notch filters requiring huge passives for realizing a large time-constant on chip, the proposed chopper notch filter is extremely area efficient. Figure 4 shows the principle of the proposed chopper notch filter. Thanks to the chopper stabilization technique, the 50Hz powerline interference with a frequency spectrum S_1 can be filtered at a much higher frequency band, i.e., 3.95-kHz and 4.05-kHz at a 4-kHz chopping frequency. Then the output chopper will demodulate them back to the base-band after filtering as depicted (spectrum S_2 to S_5).

The chopper notch filter in schematic is shown in Figure 5. It is modified from a simple *LC* notch filter with the inductor *L* being implemented by active circuitry: transistor, resistor and capacitor for silicon-area reduction. The capacitance value required for the floating capacitor C_1 can be significantly reduced by more than 500× comparing to the traditional notch filters. In addition, a negative impedance circuit with a differential impedance level of $-2/gm_x$ is employed to boost the quality factor of the notching. The notch

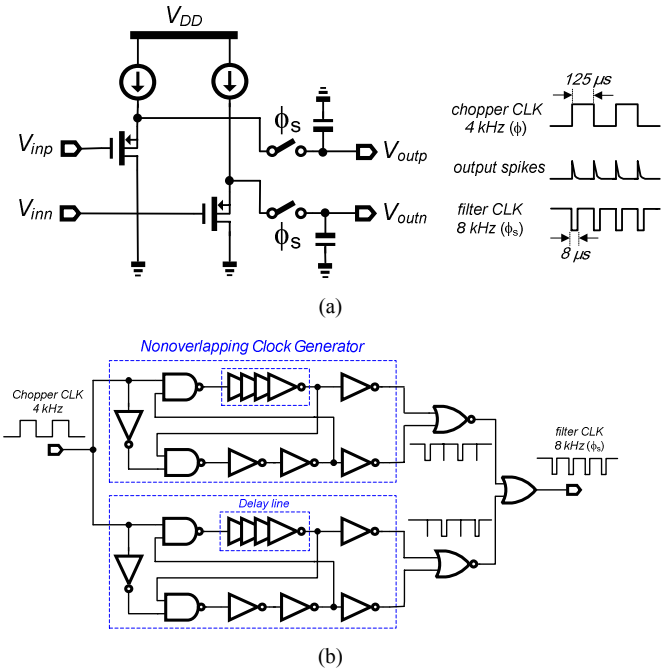

Fig. 6. (a) Spike filter and (b) the proposed spike-tracking clock generator.

frequency can be tuned and calibrated by the external capacitor C_2 and the resistor *R* that is implemented by a triode-region nMOS transistor. The transfer function of the notch filter is given by,

$$G(s) = \frac{s^2 C_1 C_2 R + s(C_1 + C_2 - C_1 gm_x R) + gm - gm_x}{s^2 C_1 C_2 (R + r_o) + s[C_1 + C_2 - C_1 (gm_x R + gm_x r_o - gm r_o)] + gm - gm_x} \quad (3)$$

where r_o is the output resistor of the source follower, *gm* is the transconductance of M_1 and M_2, and gm_x is the transconductance of M_{x1} and M_{x2}. According to (3), the term C_1+C_2-$C_1 gm_x R$ should be set to zero in order to maximize the deepness of the notch. Noting that r_o can be made sufficiently large to suppress the overshoot and deliver a high-Q notch.

5. SPIKE FILTER

A common problem of chopping technique is that spikes are generated due to the charge injection from the switches of the chopper. Fig. 6(a) shows the implemented spike filter and its operating principle. The spikes are generated at the edges of the chopper clock square wave with half of the chopper clock period. Thus the operating principle of the filter is based on the track-and-hold operation. The proposed digital circuitry that generates the desired low-duty-cycle clock waveform is shown in Fig. 6(b). It is based on the parallel operation of two non-overlapping clock generators and simple digital logics. The delay line consists of a chain of inverters and pseudo capacitors. The delay time that equals to the duration of the repetitive spikes. Noting that two delay lines cannot be built at the same non-overlapping channel, because they will otherwise induce a large time delay at the output clock and the spikes are not able to be tracked accurately in process variations. On the other hand, the proposed circuit permits individual delay-time optimization of each channel. Simulation results show that the spikes are completely filtered and result a relatively low THD (5 mVpp input and minimum gain) at the output of the RFE.

6. GAIN-BW-CONTROLLABLE AMPLIFIER

The final stage is a gain-BW-controllable amplifier [7]. Its 1st stage features a fixed gain of 20 V/V. Its 2nd stage can be selected to be 2.5, 5, 7.5 or 12.5 V/V. Thus, the total gain of the RFE can be adjusted continuously from 500 to 2500 V/V with the aid of bias voltage of R_2.

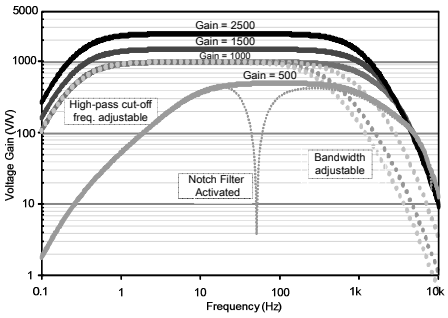

Fig. 7. Adjustable gain-BW and notch characteristics of the RFE.

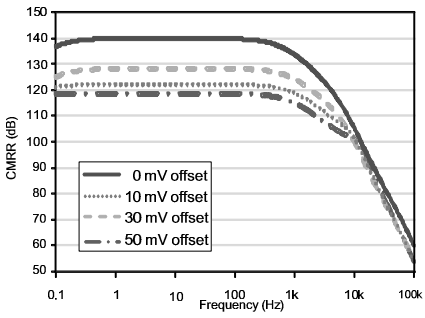

Fig. 8. CMRR under different electrode dc-offset levels up to 50 mV.

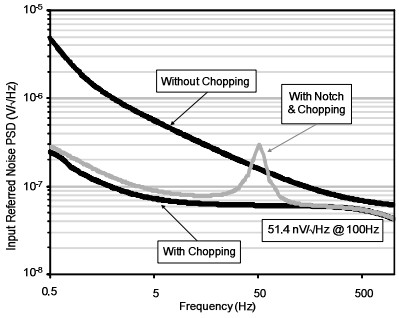

Fig. 9. Input-referred noise with and without chopping and notching.

7. SIMULATION RESULTS AND PERFORMANCE BENCHMARKS

The controllable gain feature of the RFE is demonstrated in Fig. 7, where the highpass cut-off frequency is equal to 0.4Hz and can be adjusted by the external capacitors. For the lowpass cut-off frequency, it is also adjustable by controlling the switches of the capacitive loads of the gain-BW-controllable amplifier. The simulated voltage gain is consistent to the expected value with tiny gain error. The rejection of powerline interference is more than 40dB at 50Hz and the 1st order notch has the intrinsic advantage of no passband ripple.

Figure 8 shows that the simulated CMRR varies with different input electrode offsets applied. The CMRR reaches 140dB up to 1kHz when there is no electrode offset. Since AC-coupling technique is applied to filter out the electrode and IA offsets, the CMRR is still as high as 118dB when the electrode offset is set to 50mV. Figure 9 shows the input-referred noise of the RFE before and after applying the chopping stabilization technique at the IA. It was found that the noise corner frequency is significantly reduced from roughly 500Hz to 5Hz. The residual 1/*f* noise is mainly due the stages after the IA. As shown in Fig. 9, a peak is observed at frequency 50Hz after the notch filter is activated, but the input-referred noise level at the latter band is not affected by the notch filtering operation. Table II compares the simulation results to [1] and the commercial widely-used IA AD620 [8] for biomedical applications, this work has the lowest NEF since it consumes a lower power and a lower input-referred noise after applying the thin and thick-oxide transistors combination at the IA. On the other hand, this work also provides a wide input common mode range of 1.25V, a CMRR as high as 140dB and a output swing of 2.5Vpp, not mentioning that it has the architecture advantage of being capable to be integrated together with the digital baseband, potentially resulting in a higher integration level. Comparing the RFE in this work to the existing work; it gives an additional notch filtering function, which can significantly rejecting the powerline interference.

8. CONCLUSIONS

A 3V, 106.5µW bio-potential readout front-end (RFE) with a continuous-time and tunable chopper notch filter has been presented. The IA of the RFE is implemented by the combination of thin and thick-oxide transistors available in the 90nm CMOS process, which can reduce the *1/f* and thermal noise of the IA concurrently. Mode switching at the input stage provides a simple way for selecting the required input impedance and noise level. For the spike filter, a novel spike-tracking clock generator is proposed. It is based on a parallel operation of two non-overlapping clock generators to form the desired spike-tracking waveform. The entire RFE can achieve 140 dB CMRR and is competent to sustain ±50 mV electrode offset. The *1/f* noise is significantly suppressed after chopping and the input-referred noise density is 51.4nV/√Hz. The chopper notch filter is available for ECG, EMG and EEG measurements, which can reject the powerline interference for more than 40 dB.

Table II Performance benchmarks of the designed RFE, [1] and [8]

		This work	[1]*	AD620 [8]*
Technology		90 nm CMOS	0.5 µm CMOS	N/A
Supply voltage		3 V	3 V	±2.3 V - ±18 V
Supply current	w/o notch filter	16.55 µA	20 µA	1.3 mA
	w notch filter	35.5 µA	N/A	N/A
Notch, @ 50 Hz		41 dB	N/A	N/A
Input CM range		1.05 V – 2.3 V	1.05 V – 1.7 V	vary via V_{DD}
Max. gain		2,500 V/V	2,500 V/V	10,000 V/V
Gain adjustable		via internal resistor	via internal resistor	via external resistor
Bandwidth		Adjustable	Adjustable	Not adjustable
High-freq. cut-off		0.4 Hz	0.34 Hz	N/A
Input-referred noise		51.4 nV/√Hz	60 nV/√Hz	9 - 13 nV/√Hz
THD	w/o notch filter	0.53 %	0.52 %	N/A
	w/ notch filter	0.77%	N/A	N/A
CMRR (0mV offset)		140 dB	120 dB	130 dB
CMRR (50mV offset)		118 dB	110 dB	N/A
NEF		8.5	9.2	16 - 23

* — Measurement Results

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