INFINITE IMPULSE RESPONSE SWITCHED-CAPACITOR INTERPOLATORS WITH OPTIMUM IMPLEMENTATION

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Abstract

This paper presents a new family of infinite impulse response (IIR) switched-capacitor (SC) interpolator building blocks for sampling rate increase from F_S to LF_S, and where the speed requirements of the amplifiers are determined by the lower input sampling frequency F_S. By using a complementary structure of their decimator counterparts, such new interpolators allow the realization of arbitrary baseband and anti-imaging amplitude responses employing a minimum number of switching waveforms, and since they possess similar attractive features with respect to capacitance spread, total capacitor area and speed requirements of the amplifiers they are also attractive for integration. The design of a simple 3rd. order IIR SC interpolator building block with sampling rate increase of L=2 is illustrated.

1. INTRODUCTION

An SC interpolator is a specialised network that implements a sampling rate increase from F_S to LF_S together with an appropriate filtering function to shape the baseband signals and reject the corresponding unwanted imaging components. Previously introduced finite impulse response (FIR) SC interpolators are more suitable for multinotch stopband approximations [1], whereas infinite impulse response (IIR) SC interpolators are more appropriate for high selectivity applications [2]. Such interpolators have been traditionally implemented based on *non-optimum* and *sub-optimum* classes of circuits, according to the resulting speed requirements of the operational amplifiers (OA's). The non-optimum class of IIR SC interpolator circuits, Fig.1-a, consists of an SC filter operating at LF_S and whose input signal is sampled at the lower rate F_S. These circuits are usually implemented using bi-phase SC filters designed by classical methods where the resulting speed of the OA's and capacitance spread are both determined by the higher output sampling rate LF_S. Fig.1-b represents the sub-optimum class of IIR SC interpolator circuits consisting of the cascading of a non-recursive polyphase structure with an interpolating factor of L and an SC filter operating at LF_S [2]. This type of structure yields greater design flexibility and allows for slower OA's in the polyphase structure with input sampling rate F_S, but faster OA's are still needed in the SC filter operating at LF_S.

This paper presents a new family of IIR SC interpolator building blocks with *optimum implementation* and which consist of a single network whose input and output sampling rates are F_S and LF_S, respectively, as schematically illustrated in Fig.2. The proposed building blocks use a complementary structure of their decimator counterparts [3-5], and since they retain similar attractive features with respect to capacitance spread, total capacitor area and speed requirements for the OA's, they are also particularly attractive for integration. We shall describe a systhematic approach to the design of the proposed building blocks, including the derivation of the capacitance ratios required to implement the original interpolating z-transfer function. The definition of the multiple switching waveforms that control the operation of the circuit in such a way that allow the maximum time for amplifier settling is also discussed. An illustrative example is given of the design of a 3rd. order IIR SC interpolator building block with sampling rate increase of L=2.
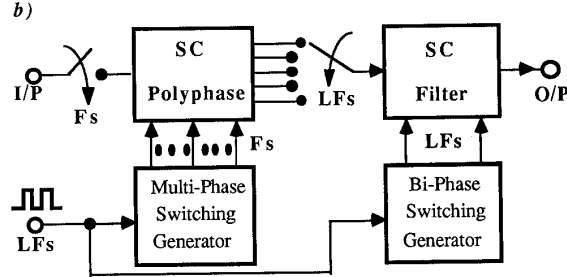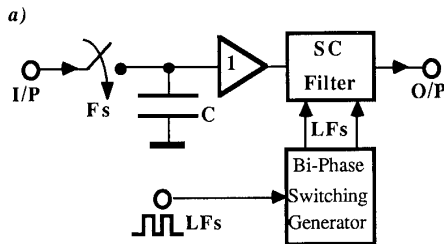
a)

b)

Fig.1 : a) Non-optimum and b) Sub-optimum classes of IIR SC interpolator circuits.
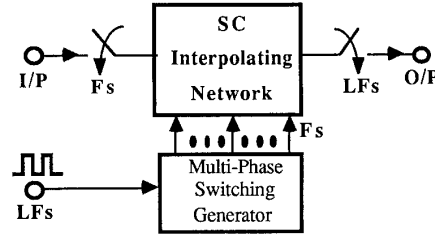
Fig.2 : Optimum class of IIR SC interpolator circuits.

2. N-TH ORDER IIR SC INTERPOLATOR BUILDING BLOCK

General z-Transfer Function: The original z-transfer function of the interpolator can be expressed as

$$H(z) = \frac{\sum_{j=0}^{N_P} a_j \cdot z^{-j}}{\prod_{i=1}^{S} [\, 1-2\, r_{P_i}\cos(\theta_{P_i}) \cdot z^{-1} + r_{P_i}^2 \cdot z^{-2}\,] \cdot \prod_{i=1}^{F} [\, b_{0_i} - z^{-1}\,]} \tag{1}$$

where the unit delay period corresponds to the sampling period $1/LF_S$ at the output of the interpolator. If the output sampling frequency is much higher than the maximum frequency of interest, i.e. $f_{cut-off}/LF_S \ll 1$, then the sample-and-hold effect on the overall response can be ignored. Otherwise, the coefficients in (1) must be prewarped by a computer-aided optimisation process to take into account such an effect over the passband of the interpolator. The numerator polynomial function can have an arbitrary order N_P and the order of the denominator polynomial function is $N=2S+F$, where S and F represent, respectively, the number of 2nd. and 1st. order sections. A well known modification of the original z-transfer function (1) leads to [6]

$$\overline{H}(z) = \frac{\sum_{m=0}^{N_P + 2S(L-1) + F(L-1)} \overline{a}_m \cdot z^{-m}}{\prod_{i=1}^{S} [\, 1 - 2\, r_{P_i}^L \cos(L\theta_{P_i}) \cdot z^{-L} + r_{P_i}^{2L} \cdot z^{-2L}\,] \cdot \prod_{i=1}^{F} [\, b_{0_i}^L - z^{-L}\,]} \tag{2}$$
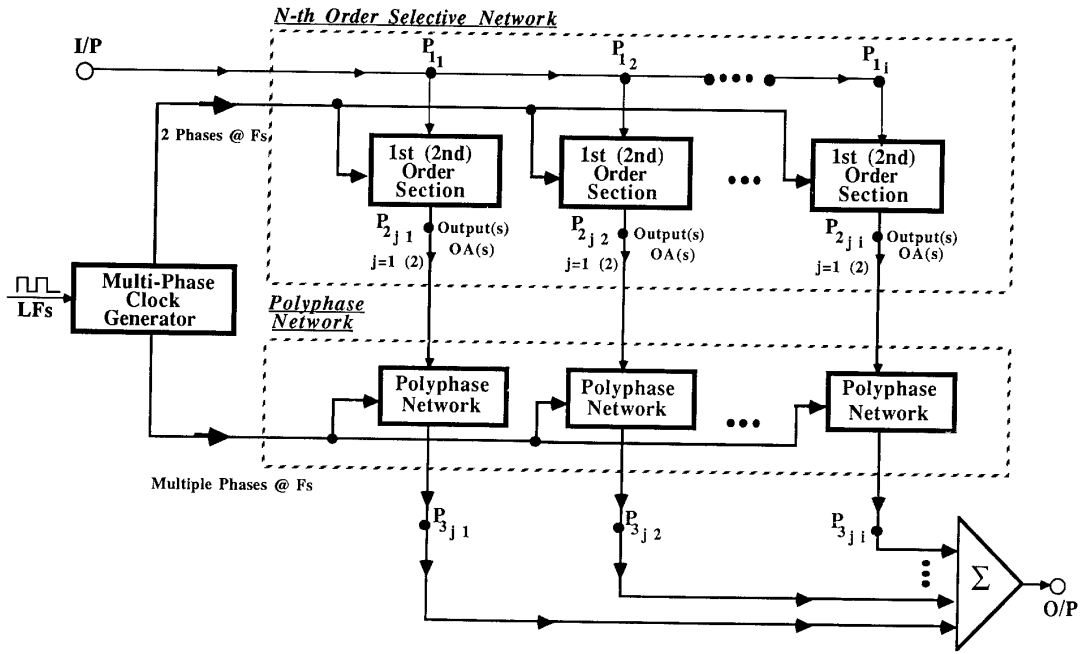
Fig.3 : General N-th order IIR SC interpolator building block with optimum implementation.

The above modified numerator polynomial function is expressed by

$$\sum_{m=0}^{N_P + 2S(L-1) + F(L-1)} \overline{a}_m \cdot z^{-m} =$$

$$= \sum_{j=0}^{N_P} (a_j z^{-j}) \cdot \prod_{i=1}^{S} (\sum_{k=0}^{2(L-1)} \alpha_{k_i} \cdot r_{P_i}^k \cdot z^{-k}) \cdot \prod_{i=1}^{F} (\sum_{l=0}^{L-1} b_{0_i} \cdot z^{-l}) \qquad (3)$$

where the coefficients α_k depend both on the poles of the original z-transfer function (1) (described by the polar coordinates r_{P_i} and θ_{P_i}) and on the interpolating factor L [4].

General Architecture: The general architecture which implements the above modified interpolating z-transfer function is presented in Fig.3. This can be divided into two major parts, namely one recursive network primarily responsible for the implementation of the denominator polynomial function and one polyphase network determining the numerator polynomial function. The recursive network can realize an arbitrary N-th order combination of real and complex conjugate poles determining the total number of OA's in the circuit, *all of which operate at the low output sampling rate F_S*. The polyphase network, on the other hand, is formed by a varying number of simple SC branches depending both on the sampling rate interpolation factor L and on the complexity of the numerator polynomial function. The analogue output signal is obtained at the output of an SC accumulator.

SC Implementation: In the block diagram of Fig.3, the N-th order recursive network is formed by the parallel connection of 1st. and 2nd. order sections. First order sections are classical damped integrators with an output polyphase network (Fig.4-a) [2-4]. Second order sections employ a biquad structure and two different sets of polyphase networks, each of which is connected to the output of an OA (Fig.4-b). For this type of section we can adopt alternative topologies, depending on the type of damping and on the accessible output. Damping can be either capacitive (E-Damping) or resistive (F-Damping), and even a combination of both, and the accessible output can be from either the 1st. or 2nd. amplifier. For the output polyphase networks we can select either a toggle switched inverter (TSI) branch or a parasitic-compensated toggle switched-capacitor (PCTSC) branch [7] and which, for simplicity, can be represented by the type of polygonal symbol shown in Fig.4-c. In such a symbol we indicate the time slot for input signal sampling, the time slot for charge transfer, and the equivalent capacitance value of the branch, which can be either negative, for PCTSC branches, or positive, for TSI branches. The operation of an interpolator circuit employing such a structure is based on

the timing diagram shown in Fig.4-d. Switching waveforms with time slots E and O control the operation of the recursive part of the circuit in a similar way as in conventional 1st. and 2nd. order sections. Such time slots are also utilised to define the input sampling of the polyphase networks and whose operation aditionally requires the time slots of time frames T and R. Time frame T comprises L time slots for charge transfer, each of which defines a new interpolating output sample, while the time slots in time frame R are utilised to reset the previous output sample of the accumulator. Based on such timing diagram, the operation of the proposed building block requires a total of (2L+1) switching waveforms but these can be reduced, on a case-by-case basis, by using some of the time slots E, O and in the time frame T to control also part of the resetting operations of the output accumulator.
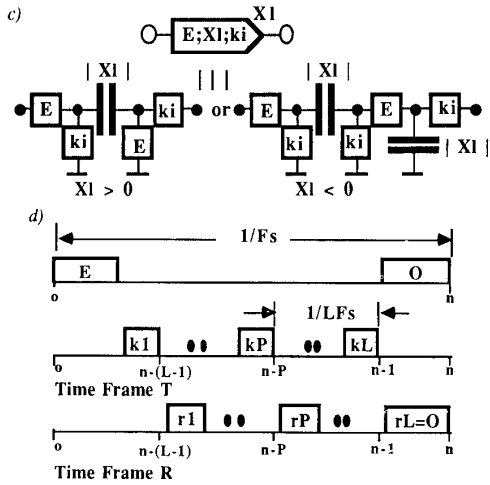
c)

d)
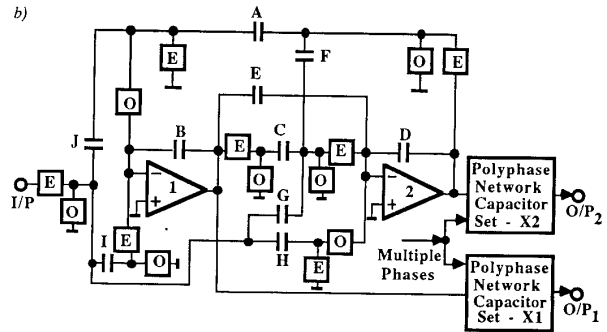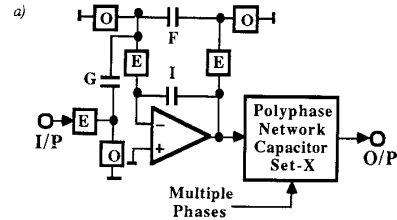
Fig.4 : General structures of a) 1st. order and b) 2nd. order SC interpolator sections; c) Symbolic representation of SC polyphase branches; c) Timing diagram.

The overall z-transfer function of the resulting circuit can be obtained from the partial z-transfer functions associated with each section. In general, for each 1st. order section (i=1,...F), we can write the transfer function between ports P_2 and P_1 as

$$T_{21_i}(z) = \frac{Vo_{P_{2_i}}}{Vi_{P_{1_i}}} \qquad (4\text{-}a)$$

and for each 2nd. order section (i=1,...S), this becomes

$$T_{21_i}(z) = \frac{Vo_{1P_{2_i}} + Vo_{2P_{2_i}}}{Vi_{P_{1_i}}} \qquad (4\text{-}b)$$

where the different outputs are obtained at the output of each amplifier. Thus, in the general expression

$$T_{21_{ji}}(z) = \frac{N_{ji}(z)}{D_i(z)} \qquad (5)$$

$N_{ji}(z)$ and $D_i(z)$ represent, respectively, the general numerators and denominator polynomials of either a damped integrator or a general biquad section [3,4,5,8], in which case j=1 and j=2 indicate the appropriate output terminal of the amplifiers. The transfer function between ports P_3 and P_2 can be represented by the equivalent transfer functions of the output SC branches

$$T_{32_{ji}}(z) = \sum_{l=0}^{L} (X_{l_{ji}} \cdot z^{-l}) \qquad (6)$$

where, in the terms $X_{l_{ji}}$, l is the order of the coefficient and j is the output terminal of the amplifiers in section i (for example, $X_{3\ 23}$ is the coefficient of z^{-3} in the output capacitor set of OA 2 in section 3). Considering that $Vi_{P11} = Vi_{P12} = ... = Vi_{P1i} = V_{in}$, then the overall z-transfer function of an N-th order interpolator results from

$$T(z) = \frac{V_o}{V_{in}} (z) = \sum_{i=1}^{S+F} \sum_{j=1}^{O} T_{21_{ji}}(z) \cdot T_{32_{ji}}(z) \qquad (7)$$

where O is the order of each section (O=1, for 1st order sections with only one output terminal, and O=2, for 2nd order sections with two output terminals). The design equations giving the capacitance values of the circuit are determined by equating (2) to the overall z-transfer function resulting from (7).

SC Accumulator: To realise the SC accumulator required to obtain the analogue output signal, whose general structure is illustrated in Fig.5-a,

three different solutions can be adopted. The solution presented in Fig.5-b employs L amplifiers, each of which is reset at the input sampling rate F_s. On the contrary, the solution presented in Fig.5-c employs only one amplifier but this is reset at the higher output sampling rate LF_s. In the solution of Fig.5-d we employ instead a unity gain buffer for reduced power and silicon consumption and higher frequency of operation [9,10]. This is similar to the solution presented in [10] for an SC analogue delay line, but because of the multiphase arrangement of the input polyphase branches the delay operator does not appear in the expression

$$V_o = \frac{1}{C_0} \cdot \sum_{k=1}^{N} (\pm) C_k \cdot V_k \qquad (8)$$

giving the total output voltage. In Fig.5-d, the branch with capacitor C_1 realizes a positive coefficient, whereas the branch with capacitor C_k realises a negative coefficient. This circuit is not totally insensitive to parasitic capacitances essentially because of the parasitic effect on the top plate of capacitor C_0 which, however, is only responsible for a small gain error. Parasitic capacitances associated with the bottom plate of each capacitor do not affect the performance of the circuit because they are always either voltage-driven or grounded, and the parasitic capacitance associated with the top plate of C_s can be compensated using a PCTSC branch [1,2]. The utilisation of this type of SC accumulator in the interpolator building block also leads to a much simpler and smaller circuit.
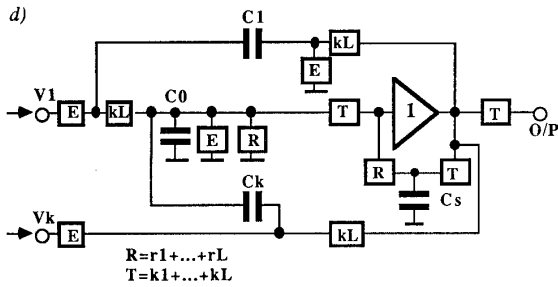
a)

b)

c)

T=k1+...+kL

R=r1+...+rL

d)

R=r1+...+rL
T=k1+...+kL
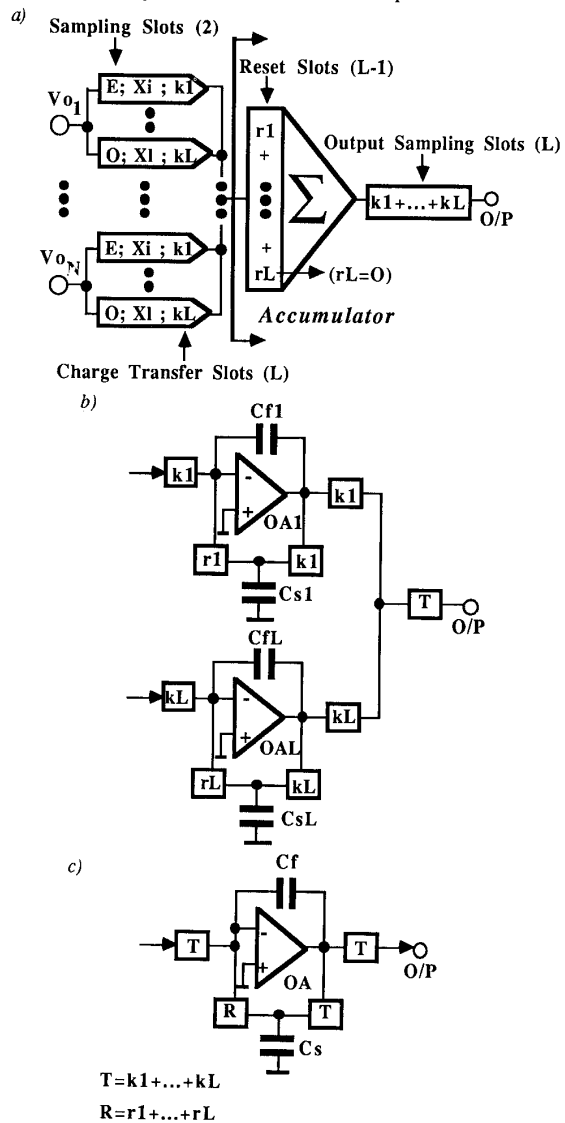
Fig.5 : *a) General SC Accumulator structure, and specific implementations with b) L amplifiers, c) only one amplifier and d) a unity gain buffer configuration.*

3. DESIGN EXAMPLE

For the purpose of demonstration we present next the design of a 3rd. order IIR SC interpolator building block with a factor L=2 of sampling rate increase. Based on a computer aided filter synthesis procedure we obtained the bilinear discrete-time coefficients given in Table1-a) for the z-transfer function of a 3rd. order prototype filter that realises a lowpass Tchebyshev approximation with cut-off frequency of 2 MHz, maximum passband ripple of 0.1dB, and an output sampling rate of $2F_s=15$ MHz. Then, according to the procedure presented before we obtained the coefficients given in Table 1-b) for the modified interpolating z-transfer function. The resulting SC interpolator circuit is shown in Fig.6, together with the corresponding timing diagram. After scaling for maximum dynamic range the resulting capacitance spread and total capacitor area, respectively, are approximately 20 and 106 capacitor units. Fig.7 shows the nominal computer simulated passband and overall amplitude responses of this interpolator, where the notches at LF_s and its integer multiples, are due to the output sample-and-hold effect.
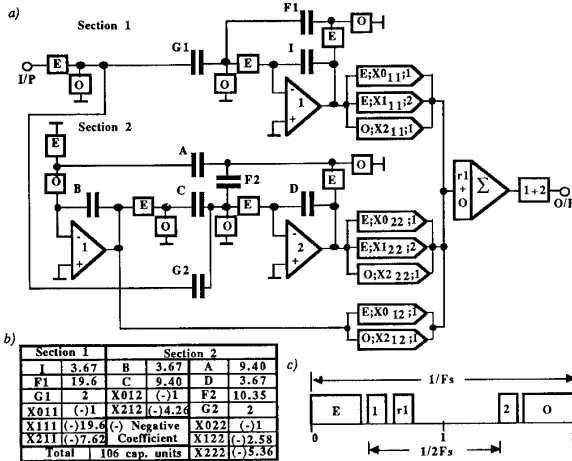
a)

b)

Section 1		Section 2		
I	3.67	B	3.67	A	9.40
F1	19.6	C	9.40	D	3.67
G1	2	X012	(-)1	F2	10.35
X011	(-)1	X212	(-)4.26	G2	2
X111	(-)19.6	(-) Negative		X022	(-)1
X211	(-)7.62	Coefficient		X122	(-)2.58
Total	106 cap. units			X222	(-)5.36

c)

Fig.6 : *a) 3rd. order IIR SC interpolator, and b) resulting capacitance values and c) switching waveforms.*

a)

Numerator	
k	0.057164
$2r_{02}\cos(\theta_{02})$	2
r_{02}^2	1
Denominator	
b_{01}	2.518693
$2r_{P2}\cos(\theta_{P2})$	0.752924
r_{P2}^2	0.511360

b)

Numerator	
a0	0.362639
a1	1.504935
a2	2.632816
a3	2.568851
a4	1.519425
a5	0.514719
a6	0.073625
Denominator	
b_{01}^2	6.343818
r_{P2}^3	0.261489
$2r_{P2}^2\cos(2\theta_{P2})$	-0.455825

Table 1 : *Coefficients of the a) prototype z-transfer function and b) modified interpolating z-transfer function.*

a)

Amplitude (dB)

3 rd. Order

Passband

Frequency (MHz)

b)

Amplitude (dB)
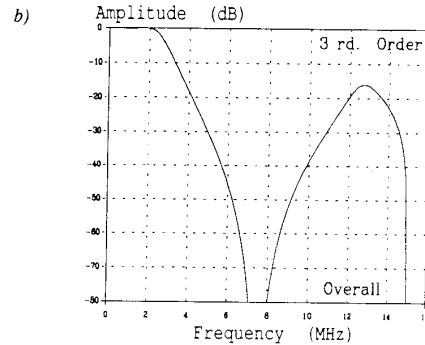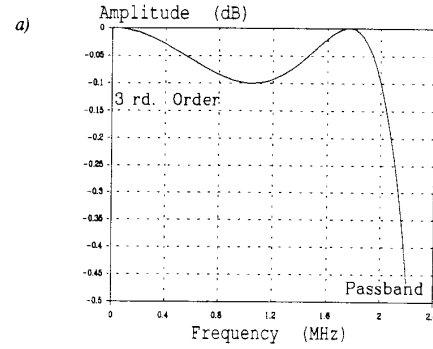
3 rd. Order

Overall

Frequency (MHz)

Fig.7 : *Computer simulated a) passband and b) overall amplitude responses.*

4. CONCLUSIONS

In this paper we have described a new family of IIR SC interpolator building blocks for sampling rate increase from F_s to LF_s, and where the speed requirements of the operational amplifiers are determined by the lower input sampling rate F_s. These new interpolators use a complementary structure of their decimator counterparts and allow the realization of arbitrary baseband and anti-imaging amplitude responses employing a minimum number of switching waveforms. Since they possess similar attractive features with respect to capacitance spread, total capacitor area and speed requirements of the amplifiers they are also attractive for integration. This was illustrated by considering the design of a simple 3rd. order IIR SC interpolator with sampling rate increase of L=2.

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