# An Open-Loop Octave-Phase Local-Oscillator Generator with High-Precision Correlated Phases for VHF/UHF Mobile-TV Tuners

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Abstract— An octave-phase local-oscillator (LO) generator for 170-to-860-MHz mobile-TV tuners is described. It is intended to incorporate with a polyphase mixer scheme for rejecting the 3<sup>rd</sup> and 5<sup>th</sup> harmonics of the LO that is critical for wideband reception. The circuit is structured by a cascade of 7 inverterbased phase correctors to generate a set of LO signals with octave phases in an open-loop formation, resulting in 4x relaxation of the synthesizer's operating frequency when comparing with the conventional closed-loop form that requires the use of a div-by-4 frequency divider. Optimized in a 90-nm CMOS process, the achieved phase precisions are  $\pm 0.8^{\circ}$  in VHF III (170 to 245 MHz) band and UHF (470 to 860 MHz) band while drawing 2.3 to 5.1 mA from a 1-V supply.

## I. INTRODUCTION

Hardware reuse for cost minimization has become one of the most essential design concerns of modern multistandard wireless communication systems. For mobile-TV applications, currently, the most dominant standards developing worldwide are DVB-H, T-DMB, ISDB-T and MediaFLO; most of them operate in VHF III (170 to 245 MHz) and UHF (470 to 860 MHz) bands. Although a zero-IF receiver topology concurrently covering 170 to 860 MHz features the highest integratability, such a wideband reception can suffer from the problem of harmonic mixing [1]. The in-band blockers located at the harmonic frequencies of the local oscillator (LO) (particularly the 3<sup>rd</sup> and 5<sup>th</sup> harmonics that experience no pre-filtering) become the co-channel interferers after frequency downconversion, as shown in Fig. 1(a). To deal with this fact, the concept of polyphase mixer scheme [2] was introduced for rejecting the 3rd and 5th harmonics of the LO. The scheme features low hardware complexity in implementation, i.e., 3 parallel paths having a gain ratio of  $1:\sqrt{2}:1$  are driven by a set of LO signal that are 45° apart of each other [Fig. 1(b)]. Unlike the generation of quadrature-phase LO signal in I/Q-mixer schemes, that the operating frequency of the synthesizer is only



Fig. 1. (a) Harmonic mixing problem in wideband receiver and (b) harmonic-rejection mixer for suppressing the LO 3<sup>rd</sup> and 5<sup>th</sup> harmonics.



Fig. 2. Multiphase LO generation. (a)  $2f_{out}$  for 4-phase outputs using a divby-2 frequency divider (b)  $4f_{out}$  for 8-phase outputs using a div-by-4 frequency divider (c)  $f_{out}$  for 8-phase outputs using a cascade of open loop phase corrector (proposed).

 $2 \times$  of the output frequency ( $f_{out}$ ) [Fig. 2(a)], an octave-phase LO signal requires the synthesizer [based on a phase locked-loop (PLL) and a *LC* voltage control oscillator (VCO)] to operate at  $4 \times$  of  $f_{out}$  [Fig. 2(b)], unavoidably complicating the design and increasing the power consumption.

In this paper, an open-loop [3] octave-phase LO generator based on a cascade of 7 phase-error correctors achieving high precision correlated phases is described. The prime advantage is that all involved circuitries are operated at  $f_{out}$  [Fig. 2(c)], avoiding using circuitries operating at  $4f_{out}$  [4].

### **II. CIRCUIT IMPLEMENTATION**

The linear model [5] of one phase corrector is shown in Fig. 3, where each inverter is modeled as a single-pole amplifier. Phasor analysis is applied to obtain phase correction transformation of the n-th phase corrector as given by,

 $Ap_{(n)} = p_{(n-1)} ,$ 

where,

A

$$= \begin{bmatrix} 1 & -bh & 0 & 0 & -ah & 0 & 0 & -ah \\ -ah & 1 & -bh & 0 & 0 & -ah & 0 & 0 \\ 0 & -ah & 1 & -bh & 0 & 0 & -ah & 0 \\ 0 & 0 & -ah & 1 & -bh & 0 & 0 & -ah \\ -ah & 0 & 0 & -ah & 1 & -bh & 0 & 0 \\ 0 & -ah & 0 & 0 & -ah & 1 & -bh \\ -bh & 0 & -ah & 0 & 0 & -ah & 1 \end{bmatrix},$$
(2)  
$$p_{(n)} = \begin{bmatrix} P_{0(n)} & P_{1(n)} & \cdots & P_{7(n)} \end{bmatrix}^T,$$
(3)

(1)

It turns out that the 8 independent eigenpairs of A are given by,

$$\begin{aligned} (\lambda_{1},\phi_{1}) &= \left(1 - (e^{-j\pi} - e^{-\frac{j7\pi}{4}})ah - e^{-\frac{j\pi}{4}}bh, \frac{1}{\sqrt{8}} \left[1 - e^{-\frac{j\pi}{4}} - e^{-\frac{j\pi}{2}} \cdots e^{-\frac{j7\pi}{4}}\right]^{T}\right) \\ (\lambda_{2},\phi_{2}) &= \left(1 - (e^{-j\pi} - e^{-\frac{j\pi}{4}})ah - e^{-\frac{j7\pi}{4}}bh, \frac{1}{\sqrt{8}} \left[1 - e^{-\frac{j7\pi}{4}} - e^{-\frac{j3\pi}{2}} \cdots e^{-\frac{j\pi}{4}}\right]^{T}\right) \\ (\lambda_{3},\phi_{3}) &= \left(1 - (e^{-j\pi} - e^{-\frac{j5\pi}{4}})ah - e^{-\frac{j3\pi}{4}}bh, \frac{1}{\sqrt{8}} \left[1 - e^{-\frac{j3\pi}{4}} - e^{-\frac{j3\pi}{2}} \cdots e^{-\frac{j5\pi}{4}}\right]^{T}\right) \\ (\lambda_{4},\phi_{4}) &= \left(1 - (e^{-j\pi} - e^{-\frac{j3\pi}{4}})ah - e^{-\frac{j5\pi}{4}}bh, \frac{1}{\sqrt{8}} \left[1 - e^{-\frac{j5\pi}{4}} - e^{-\frac{j\pi}{4}}\right]^{T}\right) \\ (\lambda_{5},\phi_{5}) &= \left(1 - (1 - j)ah + jbh, \frac{1}{\sqrt{8}} \left[1 - j - 1 \cdots j\right]^{T}\right) \\ (\lambda_{6},\phi_{6}) &= \left(1 - (1 - j)ah - jbh, \frac{1}{\sqrt{8}} \left[1 - 1 - 1 \cdots 1\right]^{T}\right) \\ (\lambda_{8},\phi_{8}) &= \left(1 - bh, \frac{1}{\sqrt{8}} \left[1 - 1 - 1 \cdots 1\right]^{T}\right) \end{aligned}$$

Assuming that N phase correctors are cascaded together, the phase transformation becomes,

$$p_{(N)} = A^{-N} p_{(0)} , \qquad (5)$$

where  $p_{(0)}$  is the input signal to the phase generator and is chosen to be,

$$p_{(0)} = \begin{bmatrix} 1 & 1 & -1 & 1 & -1 & -1 & 1 & -1 \end{bmatrix}^T bh , \qquad (6)$$

which satisfies,

$$p_{(0)} = (a_1\phi_1 + a_2\phi_2 + a_3\phi_3 + a_4\phi_4)bh \ , \tag{7}$$

where,

$$a_{1} = \frac{1}{\sqrt{2}} + j(1 - \frac{1}{\sqrt{2}}) \quad a_{3} = \frac{1}{\sqrt{2}} + j(1 + \frac{1}{\sqrt{2}}) \\ a_{2} = \frac{1}{\sqrt{2}} - j(1 - \frac{1}{\sqrt{2}}) \quad a_{4} = \frac{1}{\sqrt{2}} - j(1 + \frac{1}{\sqrt{2}}) \quad (8)$$



Fig. 3. The linear model of the n-th phase corrector.



Fig. 4. The performance of the cascading phase corrector from linear mode.

Given that the input is composed by just the first four modes of the phase generator, the last four modes will not appear after the transformation. Moreover, if the eigenvalue of  $A^{-1}$  has an absolute value of less than 1, the corresponding mode will decay eventually. When  $\omega < \sqrt{a/b} \omega_C$ , all the absolute values of the eigenvalues of  $A^{-1}$  are less than 1 which leads to weak phase correction. When  $\omega \approx \sqrt{a/b} \omega_C$ , only the absolute value of  $\lambda_1^{-1}$  is larger than 1. Thus, only the mode  $\phi_2$  is 'survived'. However, if there are more than one eigenvalues of  $A^{-1}$  which have a magnitude of greater than 1, the phase correction ability is determined by the ratio between the two largest absolute values of their eigenvalues.

For instance, considering that there are five phase correctors in cascade, the steady-state phase-error functions  $|p_{m(1)} / p_{m(0)} - \exp(-j7\pi/4)|$  are plotted in Fig. 4. The phase correction ability is weak when the input frequency is lower than the cutoff one.

Figure 5 depicts the schematic of a single-stage open-loop phase corrector. Only inverters with two different sizes, classified as *L* and *S* types, are required. The circuit optimization is conducted in transistor level since the mode  $\phi_4$  is dominant in the simulation instead of  $\phi_2$ , and the multiphase outputs in practice have an upper frequency locking limit that cannot be



Fig. 5. The schematic of the open loop phase corrector.



Cascade of Repeated Cell Fig. 6. Block schematic of the open-loop 8-phase clock generator.



Fig. 7. The schematic of the dual-mode switching inverter.

counted by the linear model. The phase corrector fades out when the input frequency exceeds the frequency locking range. In order to fulfill the frequency locking range and phase precision requirements of the targeted mobile-TV standards, 7 open-loop phase correctors in cascade are necessary (Fig. 6). The required input signal is a single-phase sine wave.

As mentioned, the proposed multiphase LO generator has a limit frequency locking range. In order to extend the locking range with low power consumption, the inverters are designed to provide dual modes as shown in Fig. 7. If  $S_1$  and  $S_2$  are switched OFF, the phase generator works for the VHF III band while if they are switched ON, the phase generator works for the UHF band. The sizes of M1 to M4 within L-type inverter are  $3\times$  of the ones within S-type inverter.

### **III. SIMULATION RESULTS**

The feasibility of the proposed open-loop octave-phase LO generator was verified in a Cadence environment using a ST 90nm CMOS process with Spectre as the simulator. The standard supply is 1 V. The transient simulation results of the 8 output phases are shown in Fig. 8. The natural frequencies of the phase corrector are 317.5 MHz or 713.1 MHz when it works in VHF III or UHF mode, respectively. In order to demonstrate the performance of the proposed phase generator, the phase-error function:  $\phi_k(f) = (t_k(f)f - k/8)360^\circ$  for k = 1, 2, up to 7 is considered. From Fig. 8,  $t_1 = 145.74$  ps,  $t_2 = 291.81$  ps,  $t_3 =$ 436.67 ps,  $t_4 = 581.14$  ps,  $t_5 = 726.63$  ps,  $t_6 = 872.72$  ps and  $t_7 =$ 1017.89 ps. The histograms depicted in Fig. 9 show the MCS of the phase error. The standard deviation of the phase errors are  $1.76^{\circ}$  and  $0.85^{\circ}$  when  $f_{out} = 245$  MHz and  $f_{out} = 860$  MHz, respectively. The simulated phase errors for the VHF III and UHF bands over the 5 process corner: TT, FF, SS, FS and SF are shown in Fig. 10(a)-(e), respectively. The phase precision is optimized to be within ±0.8° for all process corners. Figure 11 plots the power dissipation versus the  $f_{out}$  in the VHF III and



UHF bands. Typically, the dynamic power consumption ranges from 2.3 to 5.1 mW excluding that consumed by the output



Fig. 9. Histrogram of a 100-run MCS to process variation and mismatch (a)  $f_{out} = 245$  MHz (b)  $f_{out} = 860$  MHz.

driving buffers.



Fig. 10. Phase errors of the generated waveforms at (a) TT (b) FF (c) SS (d) FS and (e) SF corner versus four-

#### **IV. CONCLUSIONS**

This paper has proposed an open-loop octave LO generator suitable for multiband mobile-TV tuners. It is to incorporate with a polyphase mixer scheme for suppressing the  $3^{rd}$  and  $5^{th}$ harmonics of the LO, thereby minimizing the problem of harmonic mixing. Simulation results showed that the achieved phase precisions are  $\pm 0.8^{\circ}$ . The power consumption ranges from 2.3 to 5.1 mW at a 1-V supply. The key advantage of this openloop structure is that the PLL and *LC* VCO of the frequency synthesizer can operate at the same frequency as the LO generator, resulting in significant relaxation of speed and power when comparing with the conventional closed-loop method that relies on frequency division to generate the multiphase LO signals.

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#### REFERENCES

- M. Gupta, S. Lerstaveesin, D. Kang and B. S. Song"A 48-to-860MHz CMOS Direct-Conversion TV Tuner," *IEEE Int. Solid-State Conf. (ISSCC), Digest.*, pp. 206-207, Feb. 2007.
- [2] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K. C. Tsai, C. W. Lee and R. R. Gray, "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," *IEEE JSSC*, vol. 36, no. 12, Dec. 2001.



Fig. 11. Dynamic power dissipation of the octave-phase LO generator versus  $f_{out}$ .

- [3] K. H. Kim, P. W. Coteus, D. Dreps, S. Kim, S. V. Rylov and D. J. Friedman, "A 2.6mW 370MHz-to-2.5GHz Open-Loop Quadrature Clock Generator," *IEEE Int. Solid-State Conf. (ISSCC), Digest.*, pp. 458-627, Feb. 2008.
- [4] G. C. T. Leung and H. C. Luong, "A 1-V 5.2-GHz CMOS Synthesizer for WLAN Applications," *IEEE JSSC*, pp. 1873 -1882, vol. 39, no. 11, Nov. 2004.
- [5] A. Rezayee and K. Martin, "A Three-Stage Coupled Ring Oscillator with Quadrature Outputs," in *Proc. IEEE ISCAS*, pp.484-487, May 2001.