A Process- and Temperature- insensitive Current-Controlled Delay Generator for Sampled-Data Systems

He-Gong Wei, U-Fat Chio, Yan Zhu, Sai-Weng Sin, Seng-Pan U [1] and R.P. Martins [2]
Analog and Mixed-Signal VLSI Laboratory (http://www.fst.umac.mo/lab/ans_vlsi)
Faculty of Science and Technology, University of Macau, Macao, China
E-mail: weihegong@ieee.org
1 – Also with Chipidea Microelectronics (Macao) Ltd.
2 – On leave from Instituto Superior Técnico/UTL, Lisbon, Portugal

***Abstract*—This paper proposes a process- and temperature-insensitive current-controlled delay generator which can be widely used in sampled-data systems. The delay generator provides a large tunable range by adjusting the control current and load capacitance. Full transistor-level simulations, including process corner and Monte-Carlo analysis, are presented. The delay generator is designed in 90nm CMOS technology and consumes 330 µW power from a 1.2V power supply, at a typical case of using 10µA control current and 30fF load capacitance. The process corner simulation results exhibit a typical delay of 2.09 ns with a corner variation of -7.1% / +7.6%. The 500-times process Monte-Carlo simulation obtains a mean of 2.09 ps with a standard-deviation (σ) of 28.9 ps (1.38%).**

I. INTRODUCTION

Sampled-data building-blocks provide the indispensable link between the analog world and the digital processing in current state-of-art VLSI design. For example, data converters are crucial in medical imaging, instrumentation, consumer electronics and telecommunications [1]-[3]. In these applications, time-accuracy becomes quite significant since pulse variations may imply a considerable reduction of settling time, decreasing the linearity. In addition, the design margin for transistor implementation will also be reduced. For instance, to implement an amplifier for switched-capacitor circuits [4], [5] its speed is required to be designed under the narrowest pulse width imposed by process variation. If a process-insensitive pulse could be produced the speed requirements of the amplifier could be relaxed, thus reducing the power consumption in the whole design. Therefore, delay generators which can provide accurate clock pulses become important components in the design of sampled data systems.

The variation of the pulse obtained from the delay generator derives mainly from variations in process and temperature. To overcome these changes several solutions have been proposed which employ either off-chip [6] or on-chip [7] methods. This paper proposes a current-controlled delay generator that includes a switch-controlled current mirror, a load capacitor and some logic gates. The delay generator provides a tunable time-delay without the complexity of a delay-locked loop (DLL) but reduces the effects of process and temperature variations.

The organization of the paper will be the following: section II describes the overall architecture of the delay generator and it will include a comparison with common delay cells; section III will exhibit the demonstration of the overall performance of the delay generator through full transistor-level simulations involving process-corner and process-Monte-Carlo analysis; the conclusions will be drawn in Section IV.

II. DELAY GENERATOR IMPLEMENTATION

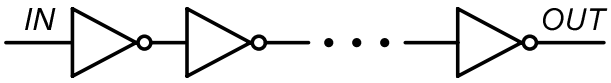

Figure 1: Traditional delay cell: *the inverter chain.*

The traditional delay generation uses the inverter-chain as shown in Figure 1, which is also called gm/C circuit [4], [8]. The delay is generated through the accumulation of the inverters' propagation delays. Since its circuit architecture only includes inverters the implementation is quite simple. However, the variation of the generated delay, mainly from process variation, can be significantly large after fabrication. When the process varies, the threshold voltage V_{TH} of the MOSFET usually changes a lot. Since the trans-conductance g_m of the MOSFET will also varies it implies a change in the propagation delay of the inverter, thus leading the total delay of the inverter chain to a significant variation.

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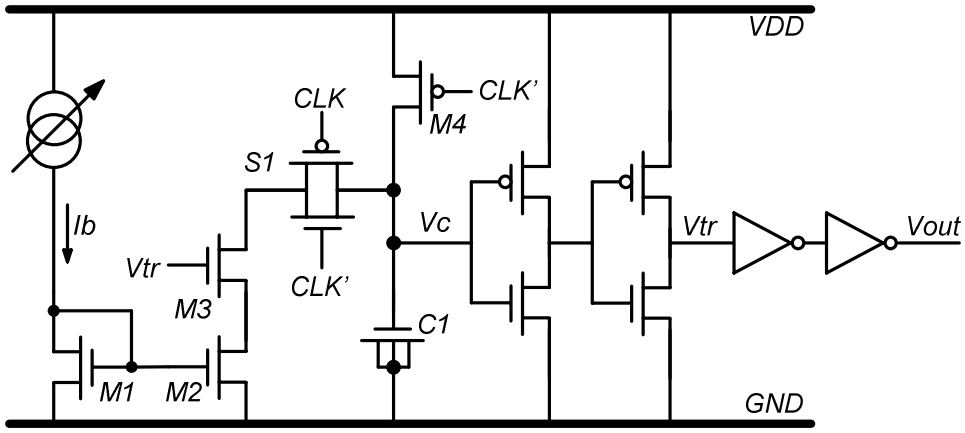


Figure 2: Circuit architecture of the proposed current-controlled delay generator

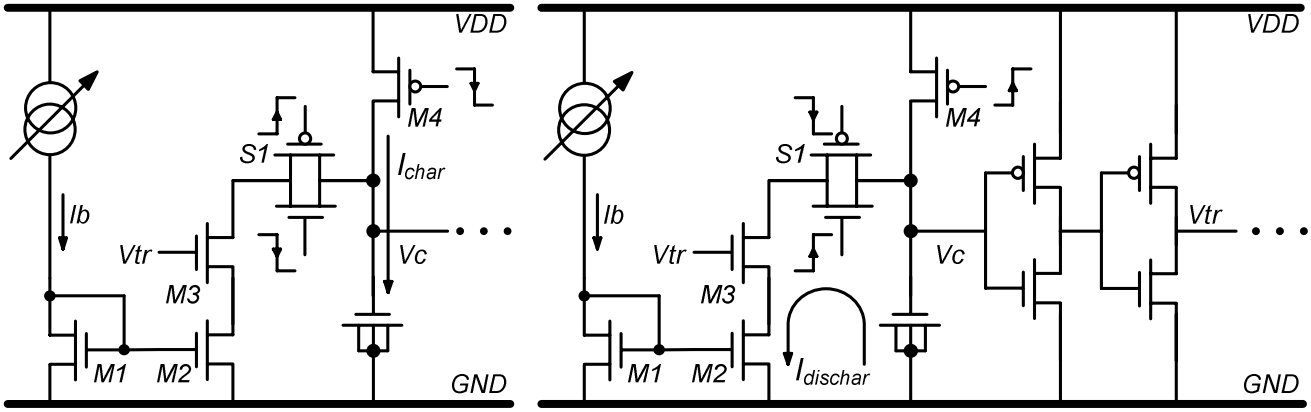


Figure 3: (a) Phase 1 and (b) phase 2 of the proposed delay generator.

Table I: Capacitance comparison of MOSCAP and MIMCAP in capacitance-process-corner analysis.

Cap.	Typical	Min	Max
MOSCAP	2 pF	1.92 pF (-4%)	2.10 pF (+5%)
MIMCAP	2 pF	1.69 pF (-15.5%)	2.30 pF (+15%)

The proposed current-controlled delay generator is presented in Figure 2 and it is controlled by an adjustable current source. The generated delay is related to the current and also to the capacitance C1, being no longer dependent on the propagation delay of logic gates. The current is provided by a current mirror, which is more insensitive to process variations, and the load capacitor C1 is implemented by a MOS capacitor (MOSCAP), which is less sensitive to process variations when compared with other capacitors' type such as the metal-insulator-metal capacitor (MIMCAP). It is well-known that MIMCAP has better linearity [9] than MOSCAP, but it exhibits higher sensitivity to process variations [10]. Table I shows the capacitance-process-corner analysis of the MOSCAP and MIMCAP, where the changes in MOSCAP due to process

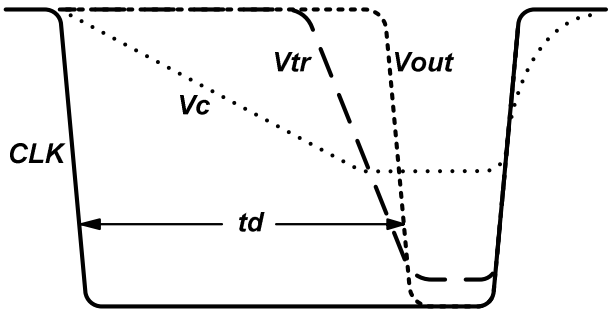


Figure 4: Key Waveform in the proposed delay generator

variations is much smaller. By adjusting the input current I_b in the current mirror, the proposed current-controlled delay generator will have the ability to establish a value of delay within a very large range while reducing the sensitivity to process variation.

The current-controlled delay generator has two operating phases. As shown in Figure 2, CLK is the input clock and CLK' is its inverse (with C1 as the loading capacitor). Two inverters connected in series have been added between V_{tr} and V_{out} as buffers to modify the rising/falling time of V_{tr} and to drive the load of next stage.

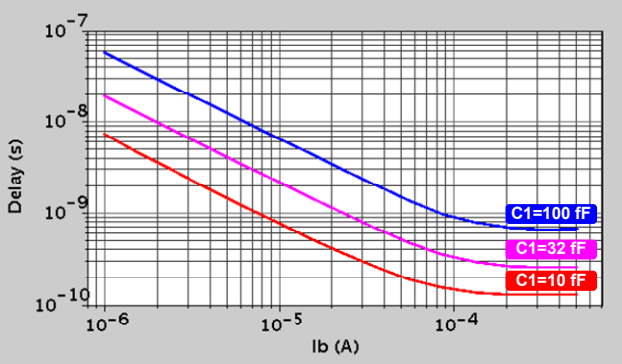


Figure 5: Delay versus the control current Ib

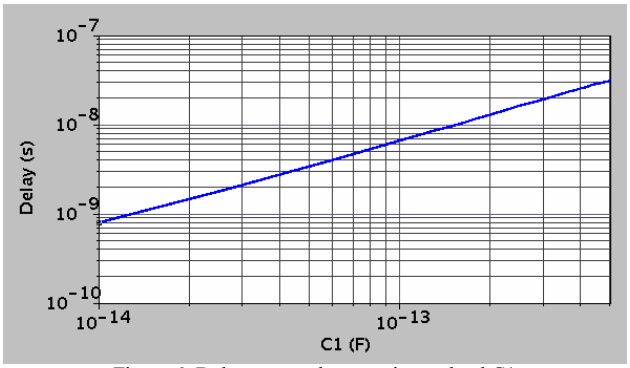
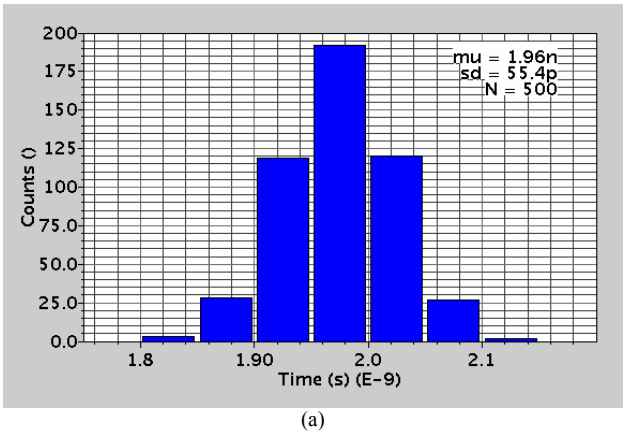


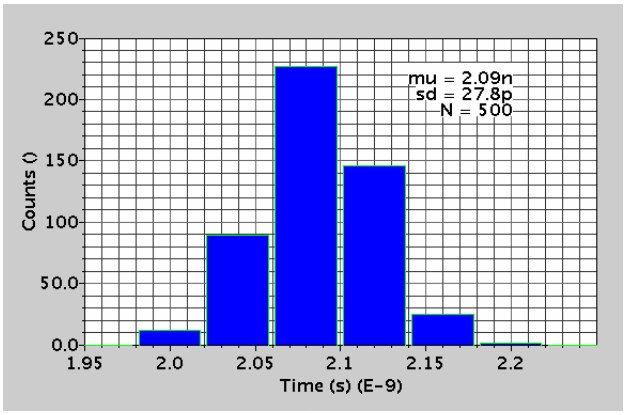
Figure 6: Delay versus the capacitance load C1

In phase 1 as shown in the equivalent circuit of Figure 3(a), when CLK goes high, the switch S1 will shut-off and the switch M4 will turn on. Then, a transient current I_{char} will charge C1 until C1's top-plate voltage V_C reaches the supply voltage. When CLK goes low, as shown in Figure 3(b), the switch M4 shuts but S1 closes. Because V_C has been charged to the supply voltage, the voltage V_{tr} obtained from V_C after two inverters, will equal the supply voltage also. Thus, M3 connects and a constant current $I_{dischar}$ begins to flow. The current mirror M2 is designed to have the same size as M1 so the $I_{dischar}$ is equal to I_b. The charge stored on the top-plate C1 flows to the ground through S1, M3 and M2 and the voltage V_C drops. When V_C reaches the triggering point of the inverter, V_{tr} becomes digital '0' and makes M3 to shut-off. Then, the charge in C1 stops flowing and V_C remains the same. In the following phase, V_C will be charged to V_{dd} again and V_{tr} also goes to V_{dd} rapidly pulled-up by the inverter.

Figure 4 shows the waveform of the interested voltage in the delay generator, in which it can be observed that V_C decreases in a constant slope. This slope, which only depends on the biasing current I_b and the capacitance C1, determines the amount of the time delay t_d, since the propagation delay in the two inverter-buffers is tiny when compared with the total delay of the circuit. Both I_b and C1 have small variations with process or temperature, therefore, the timing delay t_d will also experience small variation, as well.



(a)



(b)

Figure 7: 500-times process Monte-Carlo simulation for (a) inverter chain and (b) proposed delay generator.

III. Simulation Results

The proposed current-controlled delay generator has been simulated at full transistor-level using a 90nm CMOS process. As discussed above, the amount of the delay is determined by the biasing current I_b in the current mirror and the load capacitance C1. By altering the current or the capacitance the delay generator has the ability to be adjusted within a very large range. Figure 5 shows the controllable range of delay versus the bias current I_b with constant C1, where the delay is inversely proportional to I_b. Moreover, when I_b is large, the delay will be dominated by the intrinsic delay in the two-inverters, M3 and S1. The intrinsic delay which is mainly derived from C1 and the parasitic capacitance at V_C exhibits a saturation region for large values of I_b, as shown also in Figure 5. This unexpected region will not be considered and only the linear region will be utilized in the application. On the other hand, Figure 6 shows the controllable range of delay versus the load capacitance C1, with constant I_b, where the delay is proportional to C1. From Figures 5 and 6 it can be observed that the controllable range of the delay is very large, from hundreds of picoseconds to hundreds of nanoseconds.

Table II: Temperature variation simulation results

Temperature (^{o} C)	Inverter Chain	Proposed delay generator
-40	1.76 ns	2.07 ns
0	1.89 ns	2.08 ns
27	1.98 ns	2.09 ns
100	2.16 ns	2.09 ns
150	2.27 ns	2.09 ns

Table III: Process corner simulation results

Corner	Inverter Chain	Proposed delay generator
tt	1.98 ns	2.09 ns
ff	1.74 ns (-12.1%)	2.17 ns
ss	2.32 ns (+17.2%)	2.05 ns
fnsp	1.97 ns	2.25 ns (+7.6%)
snfp	1.94 ns	1.94 ns (-7.1%)

Table IV: Performance Summary

Technology	90nm CMOS
Power supply	1.2 V
Temperature	27 deg
Delay	2.09 ns
I_b	10 μA
C1	30 fF
Process corner	-7.1% / +7.6%
Process Monte-Carlo	σ = 27.8 ps
Power	330μW

Table II shows the delay variation of the proposed delay generator versus the temperature from -40 ^{o} C to 150 ^{o} C, and compares it with the delay generated by the inverter chain. The delay is chosen at about 2 ns as a typical value with the suitable I_b and C1, obviously where the proposed delay generator is insensitive to the temperature variation. The comparison due to process variation is shown in Table III, where five process corners, including tt (the typical), ff, ss, fnsp and snfp, are simulated with the typical delay of about 2 ns. The proposed delay generator with corner-process variations of -7.1% to +7.6% is much more insensitive than the inverter-chain whose corner-process variation is -12.1% / +17.2%. The 500-times process Monte-Carlo simulation is also shown in Figure 7 to demonstrate the process sensitivity of the delay generator, when compared to the inverter-chain. The means of the two Monte-Carlo simulations are arbitrarily located at about 2 ns. In Figure 7(a), the standard deviation of the inverter-chain is 55.5 ps (2.8%) but it is 27.8 ps (1.4%) for the proposed delay generator as shown in Figure 7(b). Table IV summarizes the overall performance of the proposed delay generator at tt process corner and room temperature.

IV. CONCLUSIONS

In this paper, a current-controlled delay generator which can be widely used in sampled-data systems has been introduced and simulated at full transistor-level in 90nm CMOS process. The proposed delay generator is demonstrated to exhibit lower sensitivity to process and temperature variations by process-corner and process-Monte-Carlo analysis when compared with the inverter-chain delay cell. Besides that, it has also the advantage of adjusting the delay in a very large range through selection of the bias current and load capacitance. At a typical delay of 2.09 ns, the delay generator consumes 330 μW power from a 1.2 V power supply, at typical corner and room temperature, with I_b=10 μA and C1=30 fF.

ACKNOWLEDGMENT

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