A 1-V 90dB DR Audio Stereo DAC with embedding Headphone Driver

Kim-Fai Wong, Ka-Ian Lei, Seng-Pan U[1] and R.P. Martins[2]
Analog and Mixed-Signal VLSI Laboratory, FST, University of Macau, Macao, China
1-Also with Chipidea Microelectronics (Macao) Ltd., 2-On leave from Instituto Superior Técnico (IST)/UTL, Lisbon, Portugal

***Abstract*—This paper presents a 1V 3rd order ΣΔ audio DAC with headphone driver. The circuit includes a 1st order FIR, 2nd order low-pass filter and as well as the headphone driver all are integrated into the internal DAC by sharing one compact low-voltage class-AB operational amplifier per channel. Implemented in 0.18-µm CMOS process it achieves 90dB dynamic range (DR) and consumes 2.6 mW per channel from 1-V supply.**

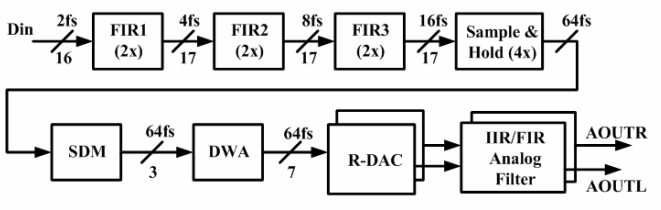

Fig. 1: Overall architecture of the audio DAC.

I. INTRODUCTION

Presently, along with the multimedia handheld devices for communication and entertainment growth rapidly, the demand for low power consumption and light portable devices has significantly increased. In addition, the enhancement of high quality and performance in audio applications is also a developing trend. Sigma-Delta modulation has become the predominant method of conversion between analog and digital domains for audio applications [1], because ΣΔ digital-to-analog converters (DACs) provide a quality equivalent to Nyquist-rate DACs with much less sensitivity to the imperfections of their building blocks, hence relaxing the circuit requirements and reducing the cost. This paper proposes the design of a low-voltage, high performance and low-power stereo audio DAC for handheld multimedia devices.

After this introduction, the digital sigma delta modulator (SDM) of the audio DAC will be presented in section II. The circuit components of the analog part of the DAC will be described in section III. In section IV the simulation results will be presented. Finally, the conclusions will be summarized in section V.

II. SDM ARCHITECTURE

The proposed digital ΣΔ modulator architecture of the audio DAC is depicted in Fig. 2 [1]-[3]. It is a third-order single-loop with a 3-bit quantizer operating with a data rate of 2.8224 MHz (an OSR of 64 is adopted). The multi-bit quantizer presents the advantages of guaranteeing the stability of the single-loop structure simultaneously with the relaxation of the design requirements of both the op-amp (slew-rate and bandwidth) in the DAC and the reconstruction low-pass filter [1]. Besides, dither signal is added in front of the quantizer which guarantees multi-bit operation also at a low-level of the signal and introduces a negligible Dynamic Range (DR) loss. Its signal transfer function (STF) and noise transfer function are:

$$STF(z) = \frac{a_1 \cdot a_2 \cdot b_1 \cdot z^{-2}}{1 + (g_1 \cdot a_2 - 2 + a_2) \cdot z^{-1} + (1 - g_1 \cdot a_2 + a_1 \cdot a_2 - a_2) \cdot z^{-2}} \quad (1)$$

$$NTF(z) = \frac{1 - (3 - g_1 \cdot a_2) \cdot z^{-1} + (3 - g_1 \cdot a_2) \cdot z^{-2} - z^{-3}}{1 + (g_1 \cdot a_2 - 2 + a_2) \cdot z^{-1} + (1 - g_1 \cdot a_2 + a_1 \cdot a_2 - a_2) \cdot z^{-2}} \quad (2)$$

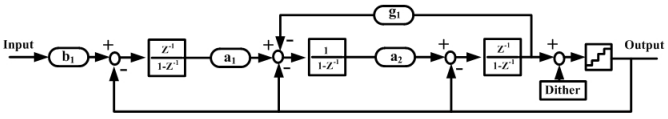

Fig. 2: Digital Σ△ modulator architecture.

In order to minimize the in-band quantization noise, the zeros of the NTF are designed to optimally spread in the band by introducing Cascaded Resonators with distributed feedback (CRFB) structure in the modulator [2]. Hence, one zero is located at dc and a complex zero is located near the edge of the signal band. The characteristic of signal-to-quantization noise versus the loop coefficients of the SDM is shown in Fig.3. As a result the optimized loop coefficients are $a_1 = 0.75$ $a_2 = 0.5$ $b_1 = 1$, $g_1 = 2^{-10}$.

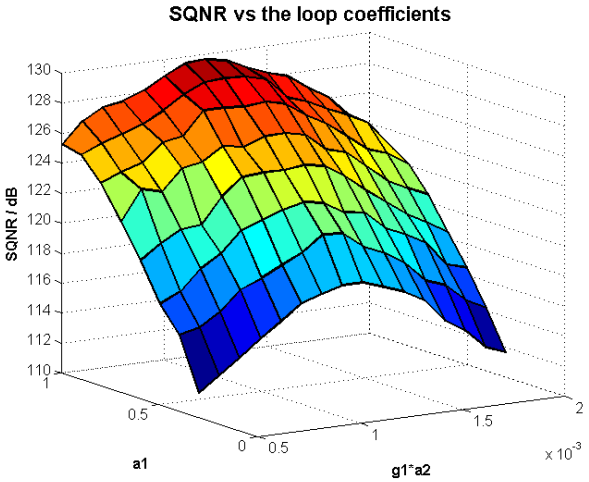

Fig. 3: SQNR versus the loop coefficients.

III. Resistor-Array DAC (R-DAC), Analog Low-Pass Filter (LPF) and Driver

The analog section of the audio DAC which includes R-DAC, a 2nd order LPF and headphone driver is shown in Fig. 4 [2]. As mentioned in section II, the SDM utilizes a 7-level quantizer, therefore 7 unitary elements $(b_1 \sim b_7)$ are used at the DAC interface. However, the natural mismatch (e.g. process variation) between the unitary elements degrades the linearity of the DAC and introduces significant distortion in the output. Hence, a DWA randomizer is applied between the digital SDM and the DAC interface to deal with this non-linearity, as depicted in Fig. 1 [4], [6].

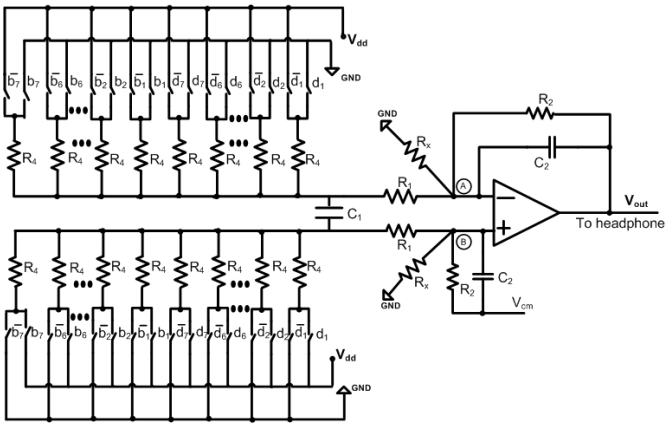

Fig. 4: DAC combined with 1st order FIR, 2nd order LPF and headphone driver.

Since the audio DAC operates under 1V supply, it is difficult to have a virtual ground common-mode (CM) voltage at half of supply voltage $(V_{dd}/2)$. Therefore, two extra resistors R_x are inserted at the virtual ground to shift these two node voltages (A and B) to a value lower than $V_{dd}/2$, in order that the input pair of transistors (PMOS) can be properly biased. Seven extra unitary elements $(d_1 \sim d_7)$ which are delayed by one clock cycle with respect to b_i, are used to integrate a first order FIR into the DAC [2], [5]. It introduces a zero at half of the sampling frequency to attenuate the out-of-band noise.

A 2nd order analog low-pass filter is also embedded into the DAC, but not the Sallen-key filter from [2] because that will contribute with higher thermal noise. Then, its transfer function can be expressed by:

$$H(s) = -\frac{R_2/(R_i + R_1)}{(1 + sC_2R_2)(1 + s2C_1 \cdot R_i // R_1)} \qquad (3)$$

where $R_i = \frac{R_4}{14}$

Its -3dB cutoff frequency is designed at 1 MHz and the in-band thermal noise (considering the contribution from all resistors at the DAC output) is designed to be less than $11.33 pV_{rms}^2$. The used resistor and capacitor vales result in: $R_1 = 3$ kΩ, $R_2 = 3.085$ kΩ, $R_4 = 70$ kΩ, $R_x = 742$ Ω, $C_1 = 52.2$ pF, $C_2 = 42.22$ pF.

Since the headphone driver ($16\Omega // 300pF$) is also integrated into the audio DAC, slew-rate is one of the key parameters for the design of the op-amp in the DAC. Class A op-amp is not appropriate because its slew-rate is always limited by the tail current. A two stage op-amp with class-AB output stage is adopted, with its architecture depicted in Fig. 5, because it increases the slew-rate and hence reduces the slew-rate-induced distortion. The output stage of the op-amp incorporates a minimum selector in the feedback loop, which contains the output transistors of the first stage of the op-amp. The bias current of the output stage transistors is regulated by this feedback loop [7]. The performance of the two stage op-amp is summarized in Table I.

Table I: The performance of the op-amp

Op-amp Performance	
Parameter	Value
DC-Gain	93 dB
Unity gain frequency	5 MHz
Phase Margin	54^0
Output-referred in-band noise	$96.58pV_{rms}^2$
Current Consumption	2.6mA
Supply Voltage	1V

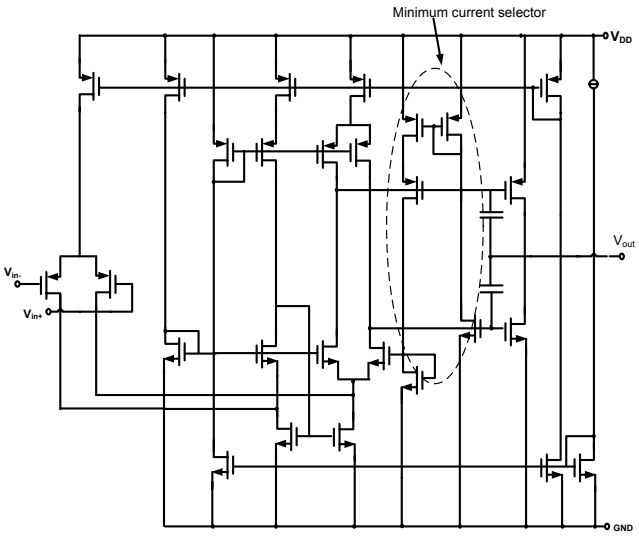

Fig. 5: Op-amp with class-AB output stage.

IV. SIMULATION RESULTS

The simulated output spectrum of the audio DAC for an input signal of 1 kHz and 0-dBFS is depicted in Fig. 6. The SNDR versus the input signal level from -90dB to 0dB is shown in Fig. 7. Without A-weighting, it achieves 82dB peak SNDR and 90dB DR. The overall performance of the audio DAC is summarized in Table II.

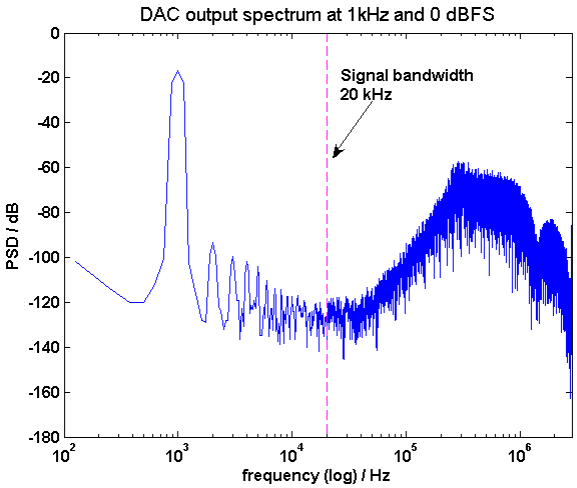

Fig. 6: Output spectrum at 1kHz and 0-dBFS

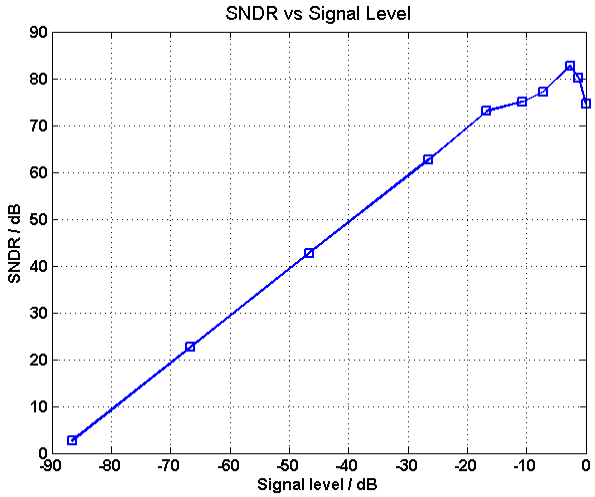

Fig. 7: SNDR versus input signal level.

V. CONCLUSIONS

With multi-bit operation in the SDM its stability and performance are improved, besides that the design requirements of the analog components of the DAC are also relaxed. With the loose filtering requirement and the strength of class-AB output stage, both the analog low-pass filter and headphone driver are integrated into the DAC through the sharing of a single operational amplifier. Finally, the audio DAC exhibits a good Hi-Fi performance for portable multimedia devices.

Table II: Overall performance of the audio DAC

	This Work
Supply Voltage	1V
Signal Bandwidth	20kHz
Clock Frequency	2.8224MHz
OSR	64
Output Swing	$0.6V_{pp}$
Load	Headphone (16Ω//300pF)
Power Consumption	2.6mW per channel
Peak SNDR	82dB
Dynamic Range	90dB
Active Die Area	Analog chip: $1.8 \times 0.9 mm^2$
Technology	$0.18\,\mu m$ CMOS

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