A Novel CMOS Switched-Current Mode Sequential Shift Forward Inference Circuit for Fuzzy Logic Controller

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***Abstract*—A novel switched-current (SI) mode sequential shift forward inference circuit for a fuzzy logic controller (FLC) is presented. The cumulative error in each inference cycle is effectively cancelled in comparison with the previous architecture [1]. SI basic cells are employed for high-frequency and low-voltage operation. The sequential structure ensures a low-power and compact realization whereas the digital portion is fully programmable. The analog input signal is processed directly without the need of an A/D or D/A interface. SPECTRE simulation results validate the feasibility of the proposed controller that is implemented in 0.35-µm CMOS with a battery 1.5-V supply.**

I. INTRODUCTION

Fuzzy logic is designed to mimic the human thinking process by incorporating the uncertainty inherent to all physical systems [2]. Relying on the human nature of the fuzzy logic, an increasing number of successful applications have been developed, such as automatic process control, pattern-recognition systems, fuzzy neurons, chaos, etc. Fuzzy systems can be implemented by software or hardware. The software solution can be highly effective and compatible if volume production, speed or portability is not demanded. On the other hand, different kinds of hardware solution, such as digital microprocessors, field-programmable FLC, application-specific FLC, analog and mixed signal FLC, have been proposed during the last decade.

Analog FLC usually presents better performance than digital implementations in the real-time control systems because of their parallel architecture. However, chip area consumption contributes a great concern as the fuzzy rules increase. In some practical applications, a small area of circuitry on the chip is required at the sacrifice of processing speed. Sampled-analog implementation is a better solution when considering speed and chip area consumption. A switched-capacitor (SC) FLC was proposed based on an efficient architecture that optimizes the processor in terms of both area and power dissipation [3] [4]. Stamatis et al [1] proposed a FLC with continuous-amplitude in fuzzy inferences and defuzzification, discrete-amplitude in fuzzy fuzzification. In sampled-analog FLC, cumulative error cannot be ignored in full sequential inference architecture.

A growing interest in low voltage and low power circuits in standard CMOS technology can be observed because of portable electronic devices and smart sensors. Current mode circuit shows great future since using current as a signal carrier enables it to be unrestricted by supply voltage. The major advantages of the SI technique are the high-speed and low-voltage operation, while the major disadvantages are the relatively larger noise and less accuracy when compared with the SC technique. However, a grade of membership handled in the fuzzy system is 0 through 1 and a resolution of 10% is enough [5]. These characteristics will imply that the current copier in SI technique will be suitable for most applications.

A switched-current mode mixed analog and digital FLC can meet the demands mentioned before. This paper presents a novel switched-current mode sequential shift forward inference circuit without cumulative error in each inference cycle under 1.5-V battery supply.

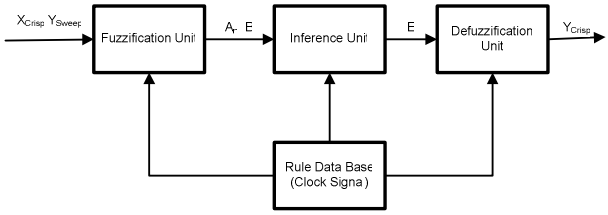

Fig. 1 FLC architecture block diagram.

II. FLC ARCHITECTURE

The architecture proposed for a FLC is presented in Fig. 1 consisting of 4 fundamental units for, fuzzification, inference, defuzzification and rule data base control.

A. Inference Algorithm

Two operations have to be performed in the inference mechanism: the calculation of each rule's output and the aggregation of all of them to obtain the overall output. To infer each rule's conclusion, the first value to be calculated is the firing strength or activation degree of the rule which measures

the degree of matching between the controller input values and the antecedent part of the rule. This value results from the connection of antecedents via triangular norms (conjunctions "and") or conorms (disjunctions "or")[6]. Among the associated operations (minimum and maximum, algebraic product and sum, bounded product and sum, etc.), minimum (min) and maximum (max) can be easily implemented by current mode circuits.

Most of the FLC use fuzzy sets to define the consequent linguistic variables. The inference methods that they usually implement are based in the "min-max" Mamdani's method, which uses a min operator to perform the fuzzy implication and a max operator to aggregate rules [7], and the "product-sum" method, which uses algebraic product and sum instead of min and max [8]. In our proposed system, the fuzzy inference algorithm is a "min-max" Mamdani's type and the i^{th} rule can be written as follows:

If x_1 is A_{1i} and x_2 is A_{2i} then y_i is B_i

where x_1, x_2 are the input variables, y_i is the i^{th} output variable from the antecedent, and A_{1i}, $A_{2i,}$ and B_i are fuzzy sets for the i^{th} rule. When the input assumes particular values a_1, a_2, the fuzzy inference process based on the "min-max" algorithm can be formally written as follows:

$$\mu_{Ci}(y_i) = \min(\mu_{Bi}(y_i), \min[\mu_{A1i}(a_1), \mu_{A2i}(a_2),]) \quad \forall y_i \exists [y_{low}, y_{high}] \quad (1)$$

$$\mu_E(y) = \max(\mu_{C1}(y_i), \cdots, \mu_{Ci}(y_i)) \quad \forall y_i \exists [y_{low}, y_{high}] \quad (2)$$

where $\mu_{E(y)}$ represents a membership function of fuzzy set E. As a function of y, y_{low} and y_{high} define the output universe of discourse.

B. *Example of the Min-Max Inference*

Considering the control example of an air conditioner [5], Fig.2 shows that there are 3 rules and each rule has 2 input variables. X_1 in column 1 is the difference between the room temperature and the set temperature at which the room is desired to be kept. X_2 in column 2 is the changing speed of the temperature. Y in column 3 is the output power of the air conditioner. The shadow part in column 3 is the μ_{Ci} from Eq.1 as the outcome of the implication process (MIN). The shadow part of the last column is μ_E in Eq.2 as the outcome of aggregation (MAX).

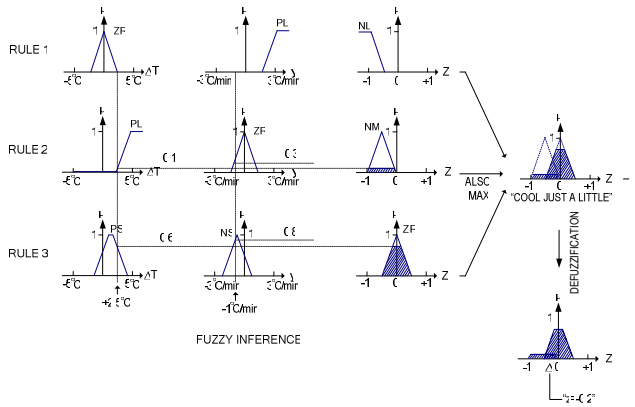

Fig.2 An aspect of an individual fuzzy inference, aggregation (ALSO) and defuzzification.

III. PROPOSED INFERENCE UNIT

Fig.3 shows the signal feedback sequential Fuzzy Inference Unit (FIU) block diagram proposed in [1]. In the first cycle, input $A_{[1]}$ is stored in P2 and ready for comparison. In the second cycle, input $A_{[2]}$ is compared with $A_{[1]}$ and the minimum current is stored in P1. Once the MIN operation is done, the resultant current is copied into P2. The same procedure is repeated for the third input, if any. At the end of this process, P2 has a stored current, which represents the result of the antecedent of the i^{th} rule. Here, the inputs are assumed to change slowly compared to the pipelined inference process. It is simple to add more inputs to the controller by going through the above procedure for other additional inputs. However, the feedback process in each cycle will cumulate the error in current copier and MIN circuit. The cumulative error becomes larger and larger as the cycles in each inference process increasing. This error is not severe in [1] because only the antecedent implication process is pipelined and the aggregation process is parallel. The cancellation of this kind of error, however, would be important in full pipelined or sequential processes.

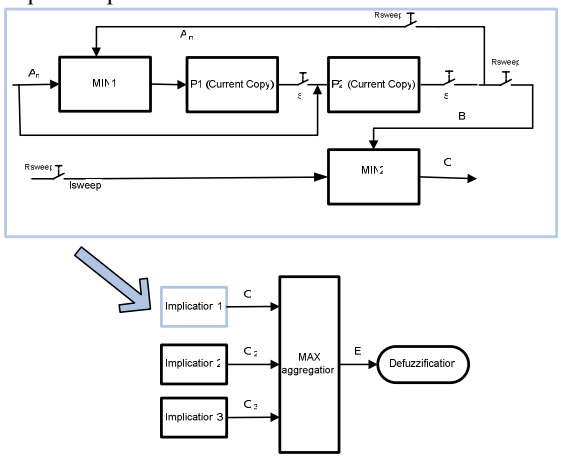

Fig. 3 Signal feedback sequential FIU block diagram.

The feedback loop is cancelled in the proposed SI inference circuit, thus canceling the cumulative error in each inference cycle. Moreover, sequential structure in antecedent implication and aggregation processes becomes realistic without the cumulative error. Fig.4 (a) shows the proposed SI sequential shift forward FIU block diagram. Clock signal is simpler than the signal feedback sequential FIU because only two non-overlapping clocks CLK and CLK- are needed as illustrated in Fig.4 (b). In the first clock phase, $A_{[1]}$ is stored in P1 and P2 stored a maximum value in the reset cycle. Following the second clock phase, the value in P1 and P2 is compared to each other and the EN clock signal is generated if the value in P1 is less than P2 and the value in P1 is transferred to P2. The same procedure is repeated for the next cycle. $A_{[2]}$ is stored in P1 and compared with $A_{[1]}$. If $A_{[2]}$ is smaller than $A_{[1]}$, $A_{[2]}$ is stored in P2. Otherwise, $A_{[1]}$ will be kept. At the end of this process, P2 has a stored minimum value. Because of the structural architecture, the MIN2 in feedback FIU as illustrated in Fig.3 can be eliminated if one cycle (two clock phases) is added. At the end of this process P2 has a stored current, which represents the value of B in i^{th} rule. It becomes realistic to add more inputs to the sequential shift forward FIU without the cumulative error.

Fig.4 (c) shows the truncation block diagram with simple current memory cell and current minimum comparator only. With the same architecture, the aggregation process can also be finished in a sequential fashion by sacrificing speed as illustrated in Fig.4 (d). Moreover, the defuzzification and the aggregation cycle can be processed at the same time in a sampled analog structure. A sacrifice in speed requirements contributes to area (circuitry) and power saving.

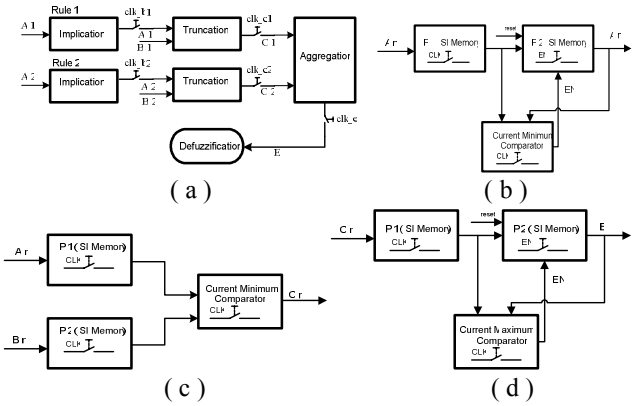

Fig. 4 (a) The proposed SI sequential shift forward FIU block. (b)Implication block. (c)Truncation block . (d)Aggregation block.

IV. Circuit Implementation And Simulation Results

The overall circuit implementation was achieved by using a 0.35-μm CMOS technology with a 1.5-V supply.

A. SI Memory Cell

The basic cell in the proposed circuit would be the SI memory cell. In SI circuits, using current as the signal carrier imposes that the impedance at every node is low. The settling time of a SI memory cell, with the structure shown in Fig.5, is determined by the time constant given by

$$\tau = \frac{C}{g_{m0}} \qquad (3)$$

,where C is the total capacitance at the gate of the memory transistor M0 and g_{m0} is the transconductance of the same transistor. The simplest way to raise g_m is to increase the W/L ratio of the MOSFET. However, since the total capacitance will also be increased simultaneously, it would be necessary to use a cascode transistor in the output MOSFET avoiding a heavy increase in the capacitance, at the sacrifice of voltage headroom. So, a self-bias wide swing current mirror will be used as illustrated in Fig.6 (a). Fig.6 (b) shows the step response of the proposed SI memory cell from 30μA to 130μA and vice-versa with a settling time less than 20 ns and an accuracy of 98%.

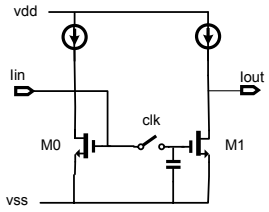

Fig.5 First generation SI memory cell.

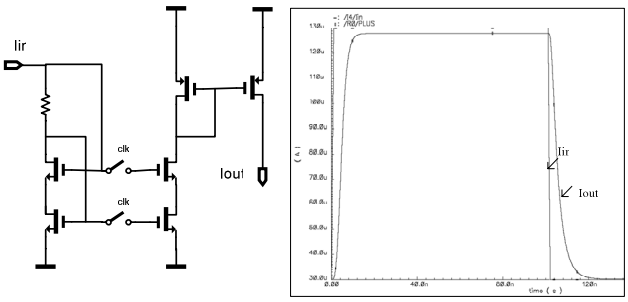

Fig.6 (a) Self-bias wide swing SI memory cell
(b) Step response of the SI memory cell.

B. Current Comparator

The current mirror comparator uses high output resistance current mirrors connected as a class AB stage, to amplify small differences in input currents when large variations in output voltage occur. However, the high output resistance will also reduce the frequency performance. One possibility for increasing the speed is to lower the slewing node impedance.

Fig.7 (a) shows a low impedance current comparator [9], where, as a consequence of the low input resistance, simpler current mirrors can be used to provide current subtraction in the input node. As illustrated in Fig.7 (b), the response time of comparison of two input currents Iin+ and Iin- is less than 10ns.

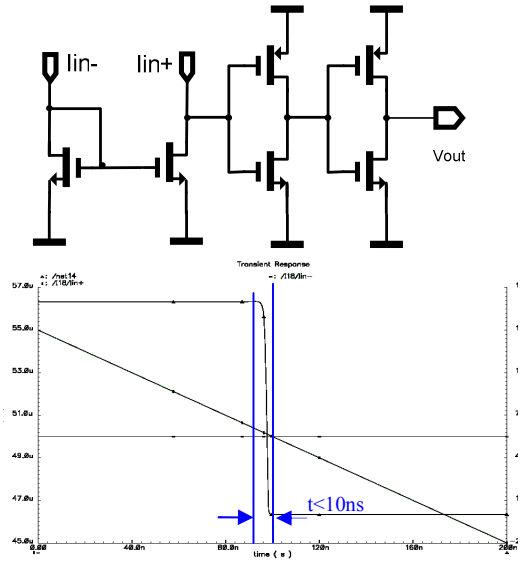

Fig.7 (a) Low impedance current comparator and its (b) Response Time.

C. Current Minimum and Maxmum Circuit

Fig.8 (a) exhibits the proposed current minimum circuit which consists of two SI memory cells and one current comparator. If Iin+ is less than Iin-, the current comparator output EN is positive, keeping the minimum value in P2 as mentioned in the last section. The current maximum circuit is used as an aggregation unit, which is similar to the current minimum with a slight modification of the comparator output EN where the reset current is now the minimum value in P2.This implies that the largest value stays in P2. By combining the SI

memory cell and the current comparator the clock phase can be set to 40ns fulfilling the circuit requirements and maintaining the accuracy at 96% as illustrated in Fig.8 (b). The error is caused by the sampled-and-hold circuit in the SI memory cell which is acceptable in fuzzy logic systems as referred before.

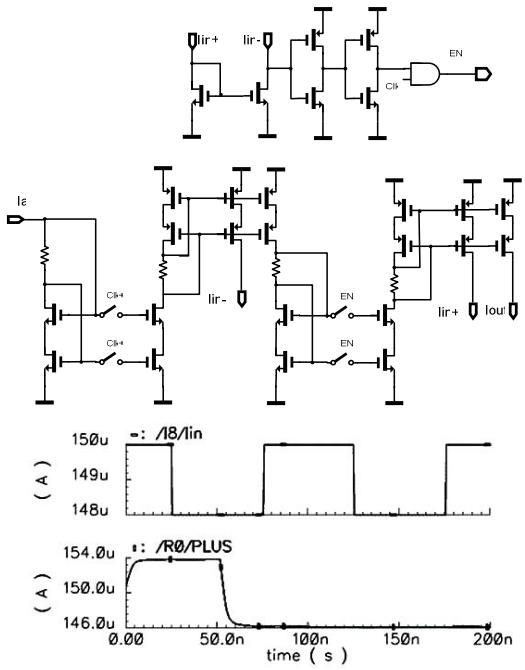

Fig.8 (a) Proposed current minimum circuit and its (b) transient response

D. SI sequential shift forward FIU circuit

For the overall circuit simulation, 2 inputs and 2 rules Mamdani fuzzy system is simulated. Inputs and rules can be added by re-arranging the clock signal as mentioned before. Fig. 9 is the transient response of truncation process of two rules and the aggregation process of these rules, which shows great accuracy .

V. CONCLUSIONS

A novel SI sequential shift forward FIU has been proposed. The cumulative error in feedback loop is cancelled and the structure is in full sequential fashion, i.e., exhibiting simpler circuit complexity and lower power consumption. Implemented in 0.35-µm CMOS technology with a 1.5-V supply, the circuit performance was verified with SPECTRE achieving a high speed operation of 20 MHz clock frequency. The achieved accuracy is better than 95% satisfactorily fulfilling the requirement of most fuzzy logic systems.

ACKNOWLEDGMENT

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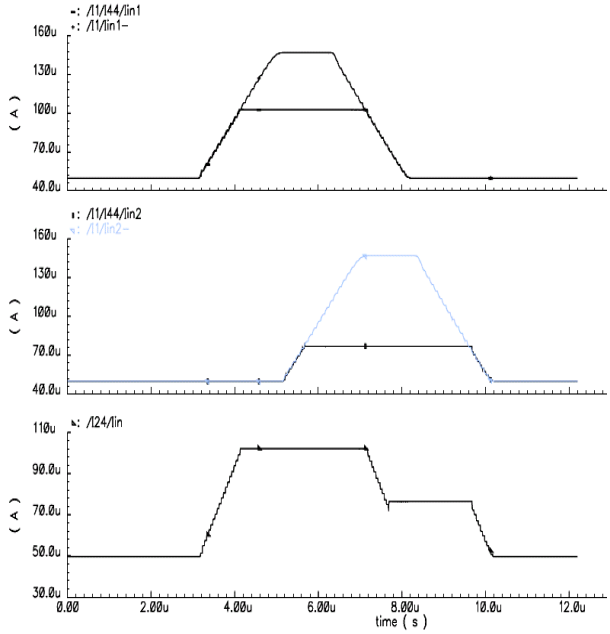

Fig.9 Transient response of truncation process of (a)the first rule, (b)the second rule and (c)the aggregation process of these rules

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