Linearity Analysis On A Series-Split Capacitor Array for High-Speed SAR ADCs

Yan Zhu, U-Fat Chio, He-Gong Wei, Sai-Weng Sin, Seng-Pan U [1], R.P.Martins [2]
Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/lab/ans_vlsi)
Faculty of Science and Technology, University of Macau, Macao, China
1 – Also with Chipidea (Mips), Macau, **2** - On leave from IST, Technical University of Lisbon, Portugal
E-mail: terryssw@ieee.org

Abstract— **A novel Capacitor array structure for Successive Approximation Register (SAR) ADC is proposed. This circuit efficiently utilizes charge recycling to achieve high-speed of operation and it can be applied to high-speed and low-to-medium-resolution SAR ADC. The static linearity performance, namely the INL and DNL, of the proposed structure is theoretically analyzed and behavioral simulations are performed to demonstrate its effectiveness. Simulation results show that to achieve the same conversion performance the proposed capacitor array structure can reduce the average power consumed from the reference ladder by 90%, as compared to the binary-weighted splitting capacitor array structure.**

I. Introduction

The SAR ADC is widely used in many communication systems, such as ultra-wideband (UWB) and wireless sensor networks which require low power consumption and low-to-medium-resolution converters. Traditional SAR ADCs are difficult to be applied in high-speed, however the improvement of technologies and design methods have allowed the implementation of high-speed, low-power SAR ADCs that become consequently more attractive for a wide variety of applications [1], [2].

The power dissipation in a SAR converter is dominated by the reference ladder of the DAC capacitor array. Recently, a capacitor splitting technique has been presented, which was proven to use 31% less power from the reference voltage and achieve better DNL than the binary-weighted capacitor (BWC) array [3]. The total power consumption of a 5b binary-weighted split capacitor (BWSC) array is 6mW, which does not take into account the power from reference ladder [1]. However, as the resolution increases, the total number of input capacitance in the binary-scaled capacitive DAC will cause an exponential increase in power dissipation, as well as a limitation with reduction of speed due to a large charging time-constant. Therefore, small capacitance spreads for DAC capacitor array is highly desirable in high speed SAR ADCs [4].

This paper presents a novel structure of a split capacitor array to optimize the power efficiency and the speed of SAR ADCs. Due to the series combination of the split capacitor array, both small capacitor ratios and power-efficient charge recycling in the DAC capacitor array can be achieved, leading to fast DAC settling time and low power dissipation in the SAR ADC. The linearity performance (INL and DNL) and parasitic capacitance effect of the proposed structure will be theoretically discussed and behavioral simulations will be executed. Deferent from the BWSC array which only achieves better DNL (but not INL) than the BWC array, the proposed capacitor array structure can have both better INL and DNL than the series capacitor (SC) array. The design and simulations of an 8b 180-MS/s SAR ADC in 1.2-V supply voltage are presented in 90nm CMOS exhibiting a Signal-to-Noise-and-Distortion Ratio (SNDR) of 48 dB, with a total power consumption of 14mW which demonstrates the feasibility of the proposed structure.

II. The Overall SAR ADC Operation

The architecture of a SAR ADC is shown in Fig.1, consisting of a series structure of a capacitive DAC, a comparator and successive approximation (SA) control logic. The SA control logic includes shift registers and switch drivers which control the DAC operation by performing the binary-scaled feedback during the successive approximation. The DAC capacitor array is the basic structure of the SAR ADC and it serves both to sample the input signal and as a DAC for creating and subtracting the reference voltage.

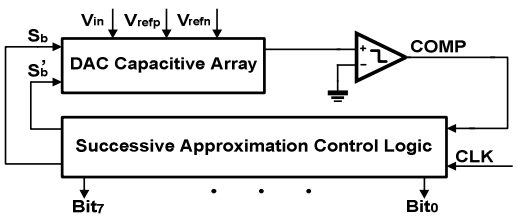

Fig. 1: Simplified block diagram of a SAR ADC architecture.

III. Capacitor Array Structure

A. Capacitor Structure Design

The major limitation on the speed of the SA converter is often related with the RC time constants of the capacitor array, reference ladder and switches. For a binary-weighted capacitor (BWC) array the size of capacitors rise exponentially with the resolution in number of bits, which cause large power and RC settling time, thus limiting the speed of the overall SAR ADC. To solve this problem, Fig. 2(a) shows a series capacitor (SC) array [5], which utilizes attenuation capacitors C_{atten} to separate the capacitive DAC into b_M bits MSB and b_L bits LSB arrays. Thus, smaller capacitor ratios can be achieved as compared to the BWC array. However, charge-redistribution switching method for SC array has been proven to be inefficient when discharging the MSB capacitor and charging the

978-1-4244-2167-1/08/$25.00 ©2008 IEEE

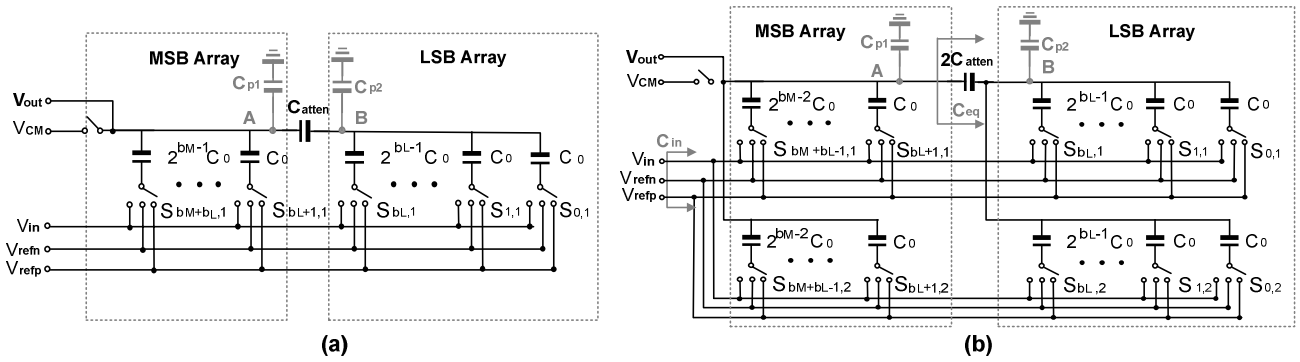

Fig. 2: a) ($b_M + b_L$)-bit SC array, b) ($b_M + b_L$)-bit SSC array.

MSB/2 capacitor, which takes 5 times more power than the charge-recycling switching method. Thus, a series split capacitor (SSC) array is proposed, as shown in Fig. 2(b), which can both alleviate the speed limitation and implement a charge-recycling switching approach.

The solution to perform charge-recycling for SC array is different from the BWC array, which just splits the MSB capacitor C_{MSB} into n-1 sub-capacitors. As illustrated in Fig. 2(b), the C_{MSB} of the SC array is split into b_M -1 sub-capacitors in MSB array, where the total capacitance of the b_M-1 sub-capacitors is $C_{MSB} - C_0$ and as a result the capacitors in LSB array and C_{atten} should be doubled, thus the C_{eq} can be calculated as

$$C_{eq} = 2C_{atten} \,//\, C_{totalLSB} = 2C_0. \tag{1}$$

$$C_{totalLSB} = 2^{b_L+1}C_0 \tag{2}$$

$$C_{totalMSB} = \sum_{n=1}^{b_{M-1}} 2^n C_0 \tag{3}$$

where $C_{totalLSB}$ and $C_{totalMSB}$ are the sum of LSB and MSB array capacitors, respectively. The C_{eq} can then be seen as two split unit capacitors C_0 attached to the right side of MSB array to maintain the capacitive ratio as 2^{bM-2}:…:2:1:1. Therefore, the charge-recycling methodology in each section can perform binary-scaled feedback during the successive approximation.

The power dissipation of DAC capacitor array is obtained from the dynamic and static power consumption of the reference ladder and usually it is dominated by the static power which is used to supply the reference voltage for the DAC capacitor array. During the same high conversion speed, the static power is determined with the RC settling time from the maximum capacitance C_{max} in the capacitor array. In an 8 bit case, the C_{max} of a SSC and BWSC structure are $8C_0$ and $64C_0$, respectively. Therefore, the BWSC will consume 8 times more static power than the SSC structure. The dynamic power is proportional to the sum of array capacitance C_{total} of which the bottom-plate is connected to the reference voltage supply [1]. In an 8 bit case, the C_{total} of the SSC array is $46C_0$. But for the BWSC array, C_{total} is $256C_0$, which can consume 5 times more dynamic power than the proposed structure. Therefore, the smaller C_{max} and C_{total} imply an increase in efficiency of the overall conversion performance.

B. Linearity Performance

To analyze the linearity of the SSC and SC arrays, each of the capacitors is modeled as the sum of the nominal capacitance value and the error term:

$$C_{n,1} = 2^{n-1}C_0 + \delta_{n,1} \tag{4}$$

$$C_{n,2} = 2^{n-1}C_0 + \delta_{n,2} \tag{5}$$

where (4) and (5) represent the capacitance in the upper and lower split array, respectively. Considering the case where all the capacitance errors are independent-identically-distributed Gaussian random variables with variances of

$$E[\delta_{n,1}^2] = E[\delta_{n,2}^2] = 2^{n-1}\sigma_0^{\,2} \tag{6}$$

and where σ_0 is the standard deviation of the unit capacitor. The accuracy of a SAR ADC is dependent on the DAC outputs which are calculated here in the case of no initial charge on the array (V_{in} =0). For a given DAC digital input X, with $D_{n,m}$ equals 1 or 0 representing the ADC decision for bit n, the analog output V_{out} (X) of the SSC array can be calculated as:

$$V_{out}(X) = \frac{2C_{atten}(\sum_{n=1}^{b_L}\sum_{m=1}^{2} D_{n,m}C_{n,m} + \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}C_{n,m}) + (C_{totalLSB} + \sum_{n=1}^{b_L}\sum_{m=1}^{2}\delta_{n,m})\sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}C_{n,m}}{2C_{atten}\,(\,C_{totalLSB} + C_{totalMSB}) + C_{totalLSB}\,C_{totalMSB} + \Delta C} V_{ref} \tag{7}$$

where

$$C_{n,m} = 2^{n-1}C_0 + \delta_{n,m} \tag{8}$$

$$\Delta C = \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2}\delta_{n,m}(2C_{atten} + C_{totalLSB}) + \sum_{n=1}^{b_L}\sum_{m=1}^{2}\delta_{n,m}(2C_{atten} + C_{totalMSB} + \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2}\delta_{n,m}). \tag{9}$$

Subtracting the nominal value (i.e. $\delta_{n,m}$=0 in (7)) from (7) yields the INL as

$$INL_{SSC} = \frac{2C_{atten}(\delta_X + \delta_Y) + \delta_Y\delta_X + C_{totalLSB}\delta_Y + \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}C_{n,m}\delta_X}{2C_{atten}\,(\,C_{totalLSB} + C_{totalMSB}\,) + C_{totalLSB}\,C_{totalMSB} + \Delta C} V_{ref} \tag{10}$$

where $\delta_X = \sum_{n=1}^{b_L}\sum_{m=1}^{2} D_{n,m}\delta_{n,m},\ \delta_Y = \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}\delta_{n,m}.$

The first and second terms in the numerator of (10) are quite small, as compared with the third and forth terms in the numerator and the third term ΔC in the denominator does not depend on the bit decision $D_{n,m}$, which only cause a gain error but not affecting the linearity performance, then they can be neglected. Thus the (10) can be simplified as

$$INL_{SSC} \approx \frac{C_{totalLSB}\delta_Y + \sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}C_{n,m}\delta_X}{2C_{atten}\,(\,C_{totalLSB} + C_{totalMSB}\,) + C_{totalLSB}\,C_{totalMSB}} V_{ref} \tag{11}$$

and the variance can be expressed as

$$E[INL_{SSC}^2] = \frac{C_{totalLSB}^2(E_{b_{M-1},1} + E_{b_{M-1},2}) + (\sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2} D_{n,m}C_{n,m})^2(E_{b_L,1} + E_{b_L,2})}{[2C_{atten}\,(\,C_{totalLSB} + C_{totalMSB}\,) + C_{totalLSB}\,C_{totalMSB}]^2} V_{ref}^{\,2} \tag{12}$$

where

$$E_{b_{M-1},1}=E\left[\left(\sum_{n=1}^{b_{M-1}}D_{n,1}\delta_{n,1}\right)^2\right],\ E_{b_{M-1},2}=E\left[\left(\sum_{n=1}^{b_{M-1}}D_{n,2}\delta_{n,2}\right)^2\right],\ E_{b_L,1}=E\left[\left(\sum_{n=0}^{b_L}D_{n,1}\delta_{n,1}\right)^2\right],\ E_{b_L,2}=E\left[\left(\sum_{n=0}^{b_L}D_{n,2}\delta_{n,2}\right)^2\right].$$

To simplified the analysis, only the worse-case INL is considered which includes all the capacitor errors together (i.e. $D_{n,m}$=1). From (6), it can be concluded that $E_{bM-1,1}=E_{bM-1,2}$ and $E_{bL,1}=E_{bL,2}$. Thus (12) can be obtained as

$$E\left[INL_{SSC}^2\right]=\frac{(2^{b_L}C_0)^2\sum_{n=1}^{b_{M-1}}2^n\sigma_0^2+(\sum_{n=1}^{b_{M-1}}2^{n-1}C_0)^2\sum_{n=1}^{b_L}2^n\sigma_0^2}{[C_{atten}(2^{b_L+1}C_0+\sum_{n=1}^{b_{M-1}}2^nC_0)+2^{b_L}C_0\sum_{n=1}^{b_{M-1}}2^nC_0]^2}V_{ref}^2. \quad (13)$$

While for the SC array, the variance $E[INL^2_{SC}]$ can be calculated similarly as

$$E\left[INL_{SC}^2\right]=\frac{(2^{b_L}C_0)^2\sum_{n=1}^{b_M}2^{n-1}\sigma_0^2+(\sum_{n=1}^{b_M}2^{n-1}C_0)^2\sum_{n=1}^{b_L}2^{n-1}\sigma_0^2}{[C_{atten}(2^{b_L}C_0+\sum_{n=1}^{b_M}2^{n-1}C_0)+2^{b_L}C_0\sum_{n=1}^{b_M}2^{n-1}C_0]^2}V_{ref}^2 \quad (14)$$

subtracting (13) from (14), and by notice that the denominators of (13) and (14) are approximately equal, then its value can be obtained as

$$E\left[INL_{SC}^2\right]-E\left[INL_{SSC}^2\right]\approx\frac{(2^{b_L}C_0)^2\sigma_0^2+(\sum_{n=1}^{b_{M-1}}2^nC_0)^2\sum_{n=1}^{b_L}2^{n-2}\sigma_0^2}{[C_{atten}(2^{b_L}C_0+\sum_{n=1}^{b_M}2^{n-1}C_0)+2^{b_L}C_0\sum_{n=1}^{b_M}2^{n-1}C_0]^2}>0. \quad (15)$$

As a result of (15), the INL of SSC array is proven to be lower than the SC array which is different from the BWC and BWSC arrays that were proven to have no difference between the INLs [1].

The maximum DNL for the SSC array is expected to occur at the step below the MSB transition [1], and the two corresponding output voltages can be calculated as

$$V_{err}(X)\approx\frac{C_{totalLSB}\sum_{n=1}^{b_{M-1}}\delta_n+\sum_{n=1}^{b_{M-1}}2^{n-1}C_0\sum_{n=1}^{b_L}\sum_{m=1}^{2}\delta_{n,m}}{2C_{atten}\ (\ C_{totalLSB}\ +\ C_{totalMSB}\ )+C_{totalLSB}\ C_{totalMSB}}V_{ref} \quad (16)$$

$$V_{err}(X-1)\approx\frac{C_{totalLSB}\sum_{n=1}^{b_{M-2}}\sum_{m=1}^{2}\delta_{n,m}+\sum_{n=1}^{b_{M-2}}2^nC_0\sum_{n=1}^{b_L}\sum_{m=1}^{2}\delta_{n,m}}{2C_{atten}\ (\ C_{totalLSB}\ +\ C_{totalMSB}\ )+C_{totalLSB}\ C_{totalMSB}}V_{ref}. \quad (17)$$

By subtracting (17) from (16), they will yield

$$DNL_{SSC}=\frac{2^{b_L+1}C_0(\delta_{b_{M-1}}-\sum_{n=1}^{b_{M-2}}\delta_{n,2})+C_0\sum_{n=1}^{b_L}\sum_{m=1}^{2}\delta_{n,m}}{2C_{atten}\ (\ C_{totalLSB}\ +\ C_{totalMSB}\ )+C_{totalLSB}\ C_{totalMSB}}V_{ref}^2 \quad (18)$$

with variance

$$E\left[DNL_{SSC}^2\right]=\frac{(2^{b_L}C_0)^2(2^{b_{M-2}}\sigma_0^2-\sum_{n=1}^{b_{M-2}}2^{n-1}\sigma_0^2)+C_0^2\sum_{n=1}^{b_L}2^{n-1}\sigma_0^2}{[C_{atten}(2^{b_L+1}C_0+\sum_{n=1}^{b_{M-1}}2^nC_0)+2^{b_L}C_0\sum_{n=1}^{b_{M-1}}2^nC_0]^2}V_{ref}^2 \quad (19)$$

$$=\frac{[(2^{b_L}C_0)^2+2C_0^2\sum_{n=1}^{b_L}2^{n-1}]\sigma_0^2}{2[C_{atten}(2^{b_L+1}C_0+\sum_{n=1}^{b_{M-1}}2^nC_0)+2^{b_L}C_0\sum_{n=1}^{b_{M-1}}2^nC_0]^2}V_{ref}^2.$$

For SC array the $E[DNL^2_{SC}]$ can be calculated similarly as

$$E\left[DNL_{SC}^2\right]=\frac{[(2^{b_L}C_0)^2+C_0^2\sum_{n=1}^{b_L}2^{n-1}]\sigma_0^2}{[C_{atten}(2^{b_L}C_0+\sum_{n=1}^{b_M}2^{n-1}C_0)+2^{b_L}C_0\sum_{n=1}^{b_M}2^{n-1}C_0]^2}V_{ref}^2 \quad (20)$$

subtracting (19) from (20), then its value can be calculated as

$$E\left[DNL_{SC}^2\right]-E\left[DNL_{SSC}^2\right]\approx\frac{(2^{b_L}C_0)^2}{2[C_{atten}(2^{b_L}C_0+\sum_{n=1}^{b_M}2^{n-1}C_0)+2^{b_L}C_0\sum_{n=1}^{b_M}2^{n-1}C_0]^2}>0. \quad (21)$$

Thus, from (21) it can be concluded that the maximum DNL of the SSC is lower than that of the SC array.

C. Parasitic Effects

One potential issue with these two series capacitor array structures (SSC and SC) are the parasitic capacitance C_{p1} and C_{p2} on the nodes *A* and *B*, which will deteriorate the desired voltage division ratio and result in poor linearity. Note that the parasitic effect is caused by the bottom- and top-plate parasitic capacitance of C_{atten} as well as the top-plate parasitic capacitance of MSB and LSB array capacitors which can be calculated as:

$$C_{p1}=\alpha\cdot C_{atten}+\beta\cdot C_{totalMSB} \quad (22)$$

$$C_{p2}=\beta\cdot C_{atten}+\beta\cdot C_{totalLSB} \quad (23)$$

where α and β represent the percentage of bottom- and top-plate parasitic capacitance of each capacitor, respectively. For the SSC array, the analog output $V_{out}(X)$ with C_{p1} and C_{p2} taken in to account can be calculated as

$$V_{out}(X)=\frac{2C_{atten}(\sum_{n=1}^{b_L}\sum_{m=1}^{2}D_{n,m}C_{n,m}+\sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2}D_{n,m}C_{n,m})+(C_{totalLSB}+C_{p2})\sum_{n=1}^{b_{M-1}}\sum_{m=1}^{2}D_{n,m}C_{n,m}}{2C_{atten}(C_{totalLSB}+C_{totalMSB}+C_{p1}+C_{p2})+(C_{totalLSB}+C_{p2})(C_{totalMSB}+C_{p1})}V_{ref}. \quad (24)$$

As this equation shows the parasitic capacitance C_{p1} and C_{p2} in the denominator are completely uncorrelated in the bit decisions, which can cause only a gain error and have no effect to the linearity performance. However, the parasitic capacitance C_{p2} in the numerator contributes with a code-dependent error, which degrades the linearity of the SAR ADC.

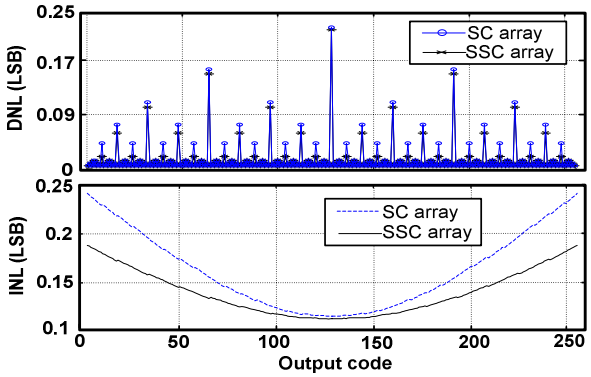

Fig. 3: Behavioral simulation comparing the linearity of the SSC and the SC array.

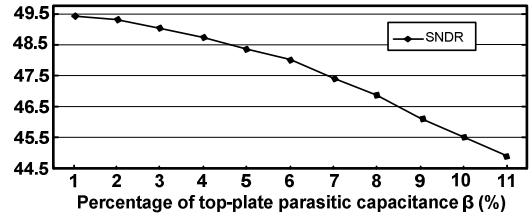

Fig. 4: Behavioral simulation of 1000 Monte Carlo SNDR versus the percentage of the top-plate parasitic capacitance β for the SSC array.

D. *Behavioral Simulations*

Two behavioral simulations of the SSC and the SC array DAC were performed to verify the analysis here. The values of the unit and attenuation capacitors are taken to be Gaussian random variables with standard deviation of 1% (σ_0/C_0=0.01), and the ADC is otherwise ideal. Fig.3 shows the result of 10000-time Monte Carlo runs, where the standard deviation of DNL and INL are plotted versus output code at the 8-bit level. As expected, the SSC array has better INL and DNL than its SC array counterpart. Fig.4 illustrates the result of 1000-time Monte Carlo runs, where the SNDR are plotted versus the percentage of the top-plate parasitic capacitance β for the SSC array structure. With C_{p2} increasing, the parasitic capacitance will decrease the SNDR of the conversion performance. But with the variance from 1% to 11% parasitic capacitance of β, a good linearity performance of a SAR ADC can still be achieved.

IV. Simulation Of a 8-bit 180MS/s SAR ADC

To verify the proposed capacitor structure of the capacitive DAC, a 1.2 V, 8b, 180-MS/s SAR ADC was designed using a 90 nm CMOS process with metal-isolator-metal (MIM) capacitor option. The SAR ADC is implemented in a fully-differential architecture with a full scale differential input range of $1.2V_{PP}$. The dynamic comparator [6] used in this ADC and it is composed of a preamplifier and a regenerative latch. Considering the parasitic capacitance of the attenuation capacitors that will reduce the linearity of the ADC, 5% top-plate and 10% bottom-plate, parasitic capacitances are included in the simulations according to the data from the foundry datasheet.

Fig. 5 shows a spectrum plot of the SAR ADC through a Monte-Carlo simulation with an input signal of 76MHz leading to an SNDR of 48dB, which clearly demonstrates the tolerance of the parasitic effect caused by the C_{p2}. Fig. 6 also shows the corresponding 30-time Monte-Carlo mismatch simulations where the ADC achieves a mean SNDR of 49dB with an input signal of 76MHz. Fig. 7 compares the power consumption from the reference ladder versus SNDR of the proposed and BWSC array structure, which demonstrates that the BWSC results in poor SNDR, due to the large RC settling time. To reach the same conversion performance the BWSC array consumes 10 times more power than the proposed structure. Table I summarizes the overall performance of the SAR ADC with the total power consumption of 14mW only and FOM of 0.35pJ/conversion-step, clearly demonstrating the low power dissipation feature of the proposed technique.

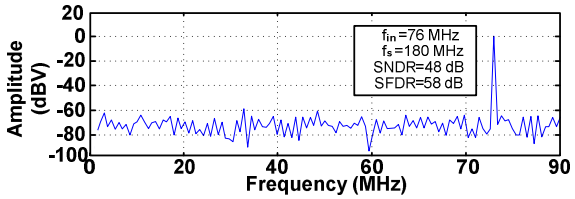

Fig. 5:Simulated FFT spectrum of the ADC.

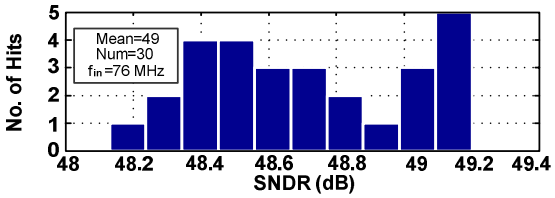

Fig. 6: 30-time Monte-Carlo simulation of SNDR of 8b SAR.

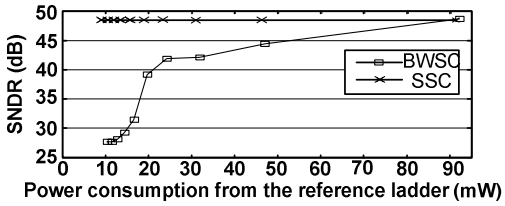

Fig. 7: Simulated SNDR versus power consumption from the reference ladder for SSC and BWSC array.

TABLE I. PERFORMANCE SUMMEY OF THE SAR ADC

Technology	90-nm CMOS with MIM
Resolution	8 bit
Sampling Rate	180 MS/s
Supply Voltage	1.2 V
Full Scale Analog Input	1.2 Vpp differential
SNDR (@fin=76MHz)	48 dB
SFDR (@fin=76MHz)	58 dB
ENOB (@fin=76MHz)	7.7 bit
FOM	0.35pJ/conversion step
Power Consumption	
Anolog	2.4 mW
Digital	2.3 mW
Reference ladder	9.3 mW
Total	14 mW

Conclusions

A novel series split capacitive DAC technique has been proposed which can both implement a charge recycling approach and achieve a small input capacitance. The reduction of the maximum ratio and sum of the total capacitance can lead to area savings and power efficiency, which allow the SAR converter to work at high-speed while meeting a low power consumption requirement. Theoretically analysis and behavioral simulations of the linearity performance demonstrate that the proposed SSC structure can have a better INL and DNL than the SC array structure. Simulation results of a 1.2V, 8b, 180-MS/s SAR ADC were presented exhibiting an SNDR of 48dB at a 76MHz input with the total power consumption of 14mW that certifies the power efficiency of the novel circuit structure.

Acknowledgment

This work was financially supported by University of Macau under the Research Grant with Ref no: RG058/06-07S/MR/FST.

References

[1] B. P. Ginsburg and A. P. Chandrakasan,"500-MS/s 5-bit ADC in 65-nm CMOS with Split Capacitor Array DAC" *IEEE J. Solid-State Circuits*, vol.42, no.4, pp.739-746, Apr. 2007.

[2] D. Draxelmayr, "A 6b 600MHz 10mW ADC Array in Digital 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp.264-265, Feb. 2004.

[3] B.P.Ginsburg and A.P.Chandrakasan, "An Energy-Efficient Charge Recycling Approach for a SAR Converter with Cpacitive DAC," *in Proc. IEEE ISSCAS*, pp.184-187, 2005.

[4] M. S. W. Chen and R. W. Brodersen, "A 6b 600 MS/s 5.3mW asynchronous ADC in 0.13µm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 574-575, Feb. 2006.

[5] R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, John Wiley & Sons, Inc., 2nd Edition 2004.

[6] G. Yin, F. Eynde, and W. Sansen, "A High-Speed CMOS Comparator with 8-b Resolution," *IEEE J. Solid-State Circuits*, vol.27, no.2, pp.208-211, Feb. 1992.