A 2.4μm CMOS SWITCHED-CAPACITOR VIDEO DECIMATOR WITH SAMPLING RATE REDUCTION FROM 40.5 MHZ TO 13.5 MHZ

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Abstract

This paper describes the design and integrated circuit implementation of a 5-th order elliptic lowpass Switched-Capacitor (SC) video decimator with a cut-off frequency of 3.6MHz and sampling rate reduction from 40.5MHz to 13.5MHz. A recently proposed novel decimator architecture is employed to make the settling time requirements of the operational amplifiers similar to those of a conventional SC filter with switching frequency of only 13.5MHz. The circuit is implemented using a 2.4μm CMOS double-poly process yielding a total area of less than 1mm^2. The power consumption is less than 50mW with 10V power supply.

1. INTRODUCTION

In recent years, significant research efforts have been devoted worldwide to the design of Switched-Capacitor (SC) circuits and systems for applications in video signal processing and high speed data transmission, e.g. [1,2]. Multirate SC networks have a great potential for such applications, specially for those that require a filtering function together with the alteration of the sampling rate [3,4]. SC decimators with Infinite Impulse Response (IIR) transfer functions constitute an important class of such circuits, mainly because of their ability to produce highly selective amplitude responses at minimum hardware cost. Until recently, however, IIR SC decimators have been designed in a non-optimum fashion whereby the operational amplifiers (OA's) have to operate at the higher sampling rate at the input of the decimator, as it happens in conventional SC filters, thus restricting the range of applications at high-frequency.

Recent advances in multirate SC networks led to the development of optimum IIR SC decimators which efficiently reduce the speed requirements of the OA's, as well as the capacitance spread and total capacitor area. In this class of circuits, we have presently available 1st. and 2nd. order building blocks [5,6] which can be cascaded to realize higher order transfer functions [7]. However, for such applications it is more efficient to consider the design of an N-th order building block which is capable of producing arbitrary passband and anti-aliasing amplitude responses using more economical circuits [8]. Based on this type of architecture, we present in this paper the design and integrated circuit implementation of an SC decimator suitable for video applications according to the CCITT recommendations [9,10]. An efficient circuit topology is adopted yielding rather low values of the capacitance spread (8) and total capacitor area (less than 100), as well as reduced response degradation under non-ideal characteristics of the OA's. The circuit employs high frequency OA's with 70dB DC-Gain and 100MHz Gain-Bandwidth (GBW) product (the phase margin is 55°, with 1pF capacitive load), and which can settle in much less than the maximum time of 34ns allowed by the switching waveforms. The circuit, which is implemented in a 2.4μm CMOS double-poly process [11], occupies a total area of less than 1mm^2 and consumes less than 50mW with 10V power supply.

2. 5-th ORDER SC LOWPASS VIDEO DECIMATOR

The SC lowpass video decimator considered in this paper is designed to reduce the sampling rate from $3F_S$=40.5MHz to F_S=13.5MHz (M=3), and possesses a 5th. order elliptic lowpass frequency response with passband ripple of 0.2dB, cut-off frequency F_C=3.6MHz, and minimum 35dB rejection above 4.44MHz [9,10].

Modified Z-Transfer Function: Based on a computer aided filter synthesis tool [12], we obtained the bilinear discrete-time coefficients given in Table 1 for the original Z-transfer function of the decimator prototype filter that can be expressed as

$$H(z)=k\frac{\left[\prod_{i=1}^{2}(1-2r_{0_i}\cos(\theta_{0_i}).z^{-1}+r_{0_i}^2.z^{-2})\right].[1+z^{-1}]}{\left[\prod_{i=1}^{2}(1-2r_{P_i}\cos(\theta_{P_i}).z^{-1}+r_{P_i}^2.z^{-2})\right].[b_0-z^{-1}]} \quad (1)$$

where the unit delay period corresponds to the sampling period of $1/3F_S$ at the input of the decimator. The zeroes and poles of the 2nd. order sections are represented by polar coordinates $r_{0(P)i}$ and $\theta_{0(P)i}$, whereas the pole of the 1st. order section is represented by b_0. The modified Z-tansfer function for optimum implementation of this SC decimator can be written as [6]

$$\bar{H}(z)=\frac{\sum_{m=0}^{15}\bar{a}_m.z^{-m}}{\left[\prod_{i=1}^{2}(1-2r_{P_i}^3\cos(3\theta_{P_i}).z^{-3}+r_{P_i}^6.z^{-6})\right].[b_0^3-z^{-3}]} \quad (2)$$

where the unit delay period still corresponds to $1/3F_S$. For unity DC-gain, the resulting modified discrete-time coefficients are given in Table 2.

SC Circuit: To implement the above modified Z-transfer function, we arrived at the SC decimator circuit shown in Fig.1-a, which operates with the switching waveforms of Fig.1-b. This circuit topology has been selected in order to obtain low capacitance spread and total capacitor area, and also reduced response degradation under non-ideal characteristics of the OA's [8]. Following the procedure presented in [8] the circuit can be described by the following Z-transfer function

$$T(z)=\frac{V_{out}=V_{3_3}}{V_{in}}(z)=\frac{k_3}{D_3(z)}.[N_{31_3}(z)+W_3(z).N_{32_3}(z).\frac{V_{3_2}}{V_{in}}(z)] \quad (3\text{-a})$$

with

$$\frac{V_{3_2}}{V_{in}}(z)\frac{k_2}{D_2(z)}.[N_{31_2}(z)+W_2(z).N_{32_2}(z).(k_1.\frac{N_{31_1}(z)}{D_1(z)})] \quad (3\text{-b})$$

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The terms k_i, $D_i(z)$, $N_{31i}(z)$ and $N_{32i}(z)$ are associated with the Z-transfer function of each section and $W_i(z)$ is the equivalent Z-transfer function of the coupling section. For the 2nd. order sections [6,8] the constant coefficient is given by

$$k_{1(3)} = \frac{1}{(1+F_{1(3)})} \qquad (4\text{-a})$$

whereas the numerator polynomial functions are expressed as

$$N_{31_{1(3)}}(z) = B_{1(3)} X_{2(5)}(z).[1-z^{-3}] - C_{1(3)} X_{1(4)}(z) \qquad (4\text{-b})$$

and

$$N_{32_{1(3)}}(z) = -C_{1(3)} \qquad (4\text{-c})$$

and, for the denominator polynomial functions, we have

$$D_{1(3)}(z) = [1+\beta_{1(3)} z^{-3} + \gamma_{1(3)} z^{-6}] \qquad (4\text{-d})$$

whose terms $\beta_{1(3)}$ and $\gamma_{1(3)}$ are given by

$$\beta_{1(3)} = \frac{A_{1(3)} C_{1(3)} - B_{1(3)} D_{1(3)} (1+B_{1(3)} D_{1(3)} + B_{1(3)} F_{1(3)})}{B_{1(3)} (D_{1(3)} + F_{1(3)})} \qquad (4\text{-e})$$

$$\gamma_{1(3)} = \frac{B_{1(3)} D_{1(3)}}{B_{1(3)} (D_{1(3)} + F_{1(3)})} \qquad (4\text{-f})$$

For the 1st. order section [6,8] we have the constant coefficient

$$k_2 = 1 \qquad (5\text{-a})$$

the numerator polynomial functions

$$N_{31_2}(z) = X_{31}(z) = X_{30} + X_{31} z^{-1} + X_{32} z^{-2} + X_{33} z^{-3} \qquad (5\text{-b})$$

and

$$N_{32_2}(z) = 1 \qquad (5\text{-c})$$

and, the denominator polynomial function

$$D_2(z) = [(D_2 + F_2) - D_2 z^{-3}] \qquad (5\text{-d})$$

Finally, for the coupling sections [6,8] we have

$$W_{2(3)}(z) = W_{2(3)} . z^{-3} \qquad (6)$$

In the above expressions, the terms X_{jl} (z) of the numerator polynomial functions represent the equivalent transfer functions of the input SC branches, where j is the order of the OA in the circuit and *l* the order of the coefficient (example: X_{32} is the coefficient of z^{-2} in the input capacitor set of OA **3**).

The final normalized capacitance values, which are also given in Fig.1-a, are obtained after equating (2) to (3), and scaling for maximum signal handling. An optimising procedure has also been employed to minimise the capacitance spread and total capacitor area in the circuit yielding, respectively, 8 and less than 100 units.

Numerator		Denominator	
k	.022698	$2r_{P_1}\cos(\theta_{P_1})$	1.488760
$2r_{O_1}\cos(\theta_{O_1})$	1.519196	$r^2_{P_1}$	.688412
$r^2_{O_1}$	1	$2r_{P_2}\cos(\theta_{P_2})$	1.609266
$2r_{O_2}\cos(\theta_{O_2})$	1.133340	$r^2_{P_2}$	.922218
$r^2_{O_2}$	1	b_0	1.434209

Table 1: Bilinear discrete-time coefficients of the 5th. order SC decimator prototype filter.

Numerator				Denominator	
a_0	.0669623	a_8	.4744776	$2r^3_{P_1}\cos(3\theta_{P_1})$	.2250505
a_1	.1434827	a_9	.4249211	$r^8_{P_1}$	.3262457
a_2	.2032289	a_{10}	.3593368	$2r^3_{P_2}\cos(3\theta_{P_2})$	-.284706
a_3	.2925909	a_{11}	.284333	$r^6_{P_2}$	.7843341
a_4	.3759253	a_{12}	.1981566	b^3_0	2.950105
a_5	.4316805	a_{13}	.1162735		
a_6	.4950802	a_{14}	.0484072		
a_7	.5151721	a_{15}	.0131211		

Table 2: Coefficients of the 5th. order SC decimator.

3. IC IMPLEMENTATION

Operational Amplifiers: For the SC decimator circuit shown in Fig.1, we have designed an high-speed single-ended folded cascode OA whose structure is shown in Fig.2. To obtain a fast settling time we use a well known technique [10,13] which employs two compensating capacitors C_C together with the output capacitor C_L. The pole and zero frequencies of the amplitude response are given by

$$f_{P_D} = \frac{g_{0_6}}{2.\pi.C_L} \qquad (7)$$

for the dominant pole, by

$$f_{P_{N-D}} = \frac{g_{m_6}}{2.\pi.(C_C + C_P)} \qquad (8)$$

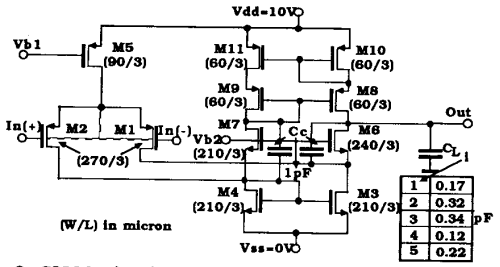

Fig. 2: CMOS circuit structure of the Operational Amplifier.

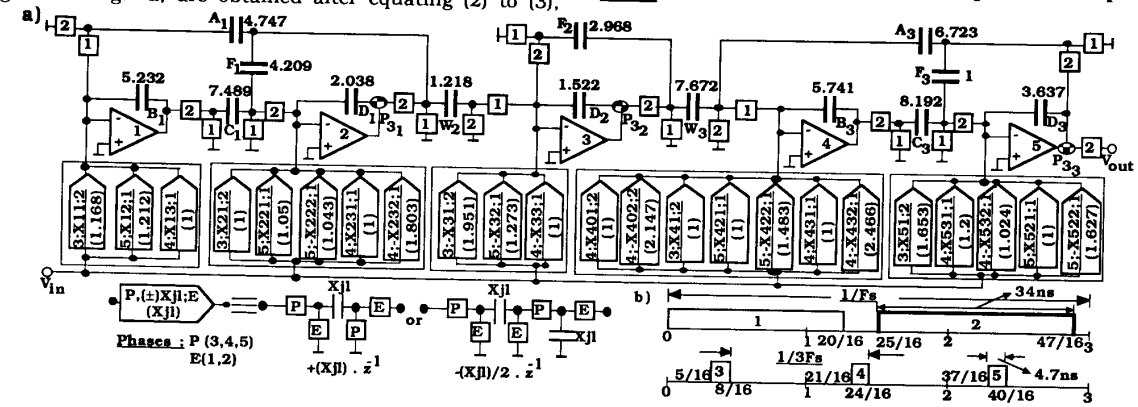

Fig.1 : 5th. order SC Video Decimator (M=3, Fsin=40.5MHz, Fsout=13.5MHz, Fcutoff=3.6MHz, Ripple=0.2dB). a) Circuit. b) Switching Waveforms.

for the first non-dominant pole, and by

$$f_z = \frac{g_{m_6}}{C_C} \qquad (9)$$

for the zero. The parameters g_{06}, g_{m6} and C_P are, respectively, the output conductance, the transconductance and the parasitic capacitance at the source node of cascode transistor M_6. If $C_P << C_C$, then the zero compensates for the first non- -dominant pole and the settling time will be imposed by another non-dominant pole at a much higher frequency. In Fig.3 we present results of the electrical simulation of the OA using the ELDO program [14]. The amplitude and phase responses (Fig.3-a) show a DC-Gain=70dB and a value of GB≈100MHz (phase margin, $\phi_m \approx 57^o$) with C_C=1PF and C_L=1.3pF (maximum OA capacitive load in the circuit). For a unity gain configuration, and input voltage step of 1V, the settling-time is 17ns (Fig.3-b). The DC transfer characteristic of the amplifier is presented in Fig.3-c showing an output voltage swing of 6V.

To maximise the settling times of the amplifiers in the circuit we have appropriatelly tailored the values of the output compensating capacitors C_L in the circuit, according to the capacitive loads of each OA in each switching phase. Thus, OA's which have larger output capacitive loads (OA's **1** and **4**) will have smaller values of C_L, whereas OA's with smaller output capacitive loads (OA's **2**,**3** and **5**) will have larger values of C_L.

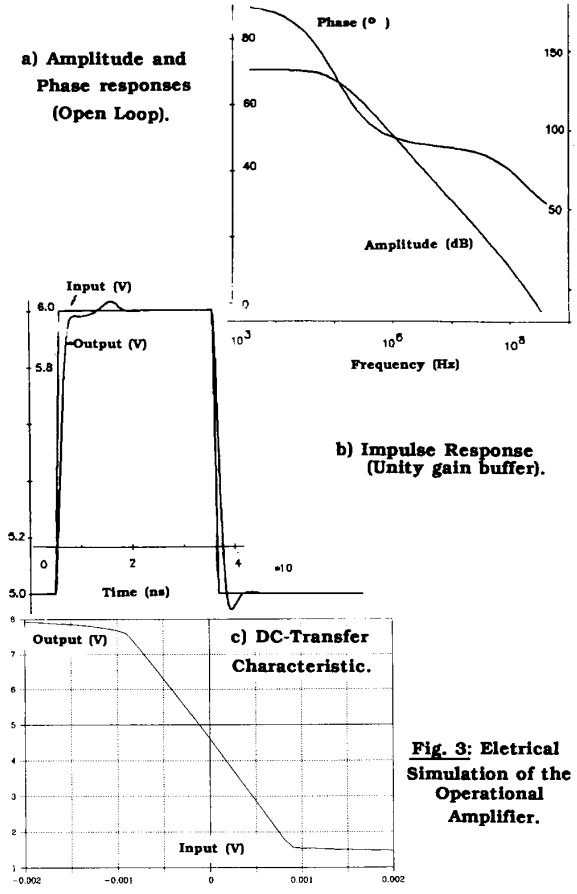

Fig. 3: Eletrical Simulation of the Operational Amplifier.

Analogue Switches: For very high speed of operation together with reduced charge injection and clock feedthrough, we have adopted the structure of Fig.4-a to realise the analogue switches in the SC decimator of Fig.1. The transistors in the input polyphase networks have larger (W/L) ratios than in the recursive network, since they must supply more current in larger capacitors and switch in time intervals of only 4.7ns. The on-resistance, evaluated with ELDO [14], Fig.4-b, is $R_{on} \approx 700\Omega$ (W/L=15/3) and $R_{on} \approx 900\Omega$ (W/L=12/3) for the circuit operating voltage (around 5V). These values imply time constants of $\tau_1 \approx 0.5$ns (C≈0.1pF), in the input polyphase networks, and of $\tau_2 \approx 5$ns (C≈1pF) in the recursive network.

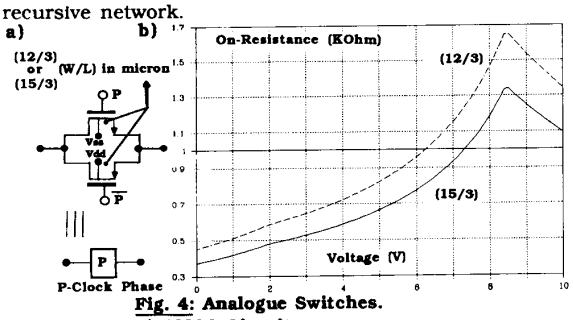

Fig. 4: Analogue Switches.
a) CMOS Circuit.
b) Simulated On-Resistance.

Capacitors: High precision capacitors have been designed with guard rings around the top plate in order to minimise etching and fringing effects. To maximise the accuracy of larger capacitance ratios, we employ an association of unit capacitors (unity capacitance is approximately $0.1pF = 18x18\mu m^2$), and to prevent high-frequency parasitic signal injection into the analog path through the substrate the overall set of capacitors is shielded using an N-well substrate connected to ground.

Chip Architecture The SC video decimator has been implemented as an integrated circuit using a 2.4μm CMOS, N-well, double-poly, single-metal technology [11]. The layout architecture of the chip is presented in Fig.5. Special cares have been taken into account in order to reduce parasitic high-frequency signal injection in the analog path, clockfeedthrough and capacitance overlap bettween the outputs and inverting inputs of the OA's. Different analog and digital power supplies are provided to decouple the analog part of the circuit (OA's and Capacitors) from the digital part (Switches). The clock busses are separated from the rest of the circuit and independent power supply voltages are also supplied to bias all the OA's.

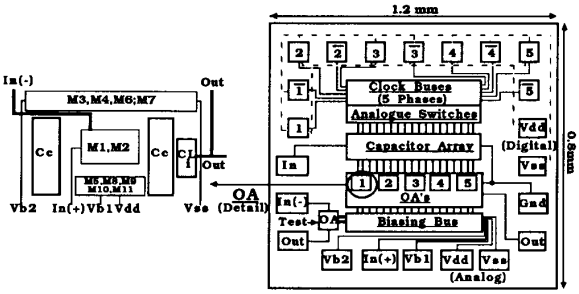

Fig. 5: Integrated Circuit Architecture.

4. COMPUTER SIMULATED RESULTS

Functional Simulation: For ideal OA's and nominal capacitance values, the SC decimator of Fig.1 produces the computer simulated [15] passband and overall amplitude responses illustrated in Fig.6. In Fig.7 we can observe the resulting deviations of the amplitude responses when we consider practical 100MHz OA's with varying DC-Gain, together with realistic capacitance ratio accuracies of 0.1%. These results show an acceptable circuit performance for 100MHz OA's with DC-Gain values over 60dB, whereas for smaller DC-Gain values there is a visible degradation specially in the anti-aliasing-band.

Electrical Simulation: The electrical simulation of the circuit, which is carried-out using ELDO, is performed into two steps using appropriate macromodels for the amplifiers (DC-Gain=70dB, GB=100MHz, Slew rate=10V/ns) and switches(R_{on}=0.75KΩ). In the first step, we obtain the impulse response of the circuit by means of a transient analysis obtained for a 1V-step input voltage (Fig.8-a). Then, with an FFT post-processor, we obtain the amplitude frequency response illustrated in Fig.8-b.

5. CONCLUSIONS

In this paper we describe the design and integrated circuit implementation of a 5-th order elliptic lowpass SC video decimator, with cut-off frequency of 3.6MHz and sampling rate reduction from 40.5MHz to 13.5MHz. This is based on a novel decimator architecture which considerably relaxes the speed requirements of the amplifiers, and also minimises the capacitance spread and total capacitor area. The circuit employs high performance OA's with 70dB DC-Gain and 100MHz GB product, and which can settle in less than the maximum time of 34ns allowed by the switching waveforms. For a 2.4μm CMOS double-poly process, the overall circuit occupies less than 1mm^2 of silicon area, and consumes less than 50mW with 10V power supply.

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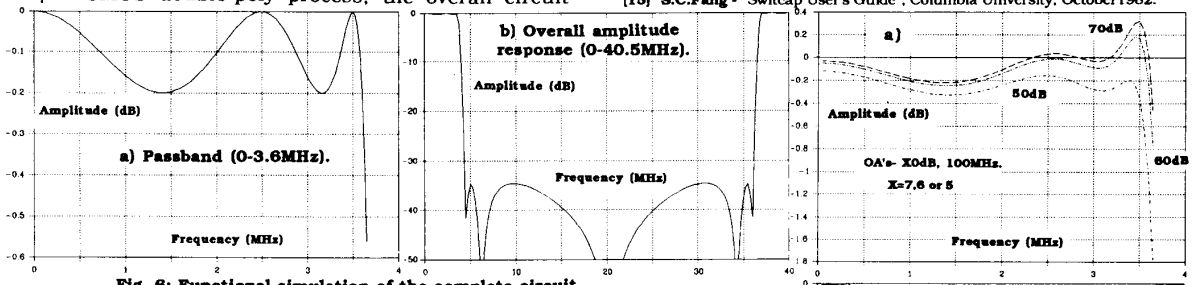

Fig. 6: Functional simulation of the complete circuit. (Amplitude response with ideal OA's and nominal Capacitor values).

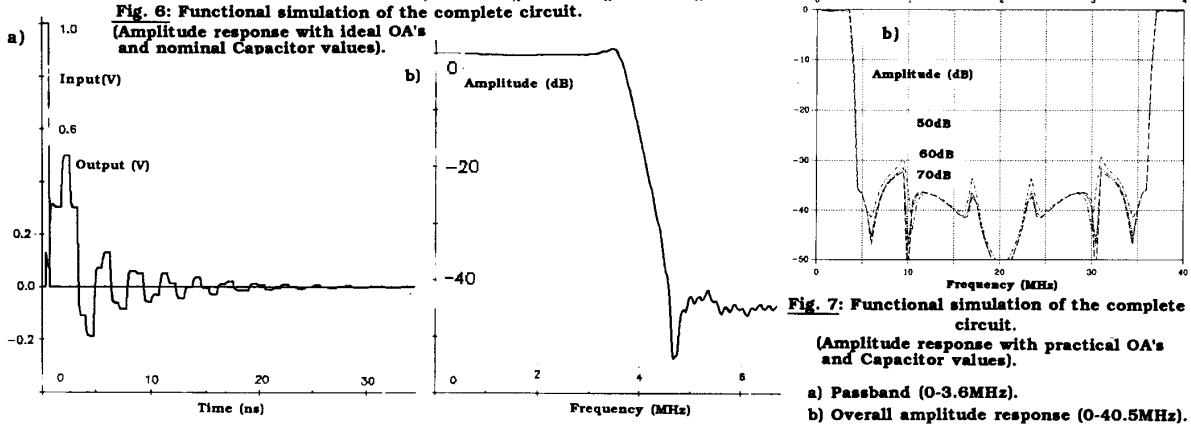

Fig. 8: Eletrical Simulation of the complete circuit. a) Impulse Response. b) Amplitude Response.

Fig. 7: Functional simulation of the complete circuit. (Amplitude response with practical OA's and Capacitor values).

a) Passband (0-3.6MHz).
b) Overall amplitude response (0-40.5MHz).