A Power Scalable 6-bit 1.2GS/s Flash ADC with Power on/off Track-and-Hold and Preamplifier

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***Abstract*—A power scalable 6-bit 1.2GS/s flash Analog-to-Digital Converter (ADC) is designed in 90nm CMOS. Rapid power on/off Track-and-Hold (T/H) and preamplifiers are proposed to provide scalable power consumption with sampling rate variation. Full transistor-level simulations of the ADC are presented from 1 MS/s (3 mW) to 1.2 GS/s (41 mW). At the maximum sampling rate the DNL is -0.9/+0.7 LSB and the INL is -0.8/+0.6 LSB. The ADC achieves 33 dB SNDR, 44 dB SFDR, and 0.9 pJ/conversion-step at Nyquist from 1.2V power supply.**

I. INTRODUCTION

Flash ADCs are the key components in many applications such as data storage read channels or wireless communication systems where very high sampling rate and low resolution are required [1], [2]. On the other hand, for a variety of applications with a wider range of requirements related with power and speed it becomes desirable to integrate in a flash ADC the capability of scaling power as a function of the sampling rate in order to optimize the analog front-end operation with the replacement of individual power-optimized ADCs [3], [4]. With a significant reduction in power dissipation at lower sampling rates flash ADCs can be applied both at very high-speed or low-speed in wireless sensor systems, biomedical engineering, or mobile communications, as for example in multi-band OFDM and UWB for wireless personal area networks [5].

In this paper a power-scalable 6-bit 1.2 GS/s flash ADC will be proposed. The novel architecture includes a T/H and a preamplifier designed to allow fast power on/off and therefore consuming negligible power during power-down except in the resistive ladder. The proposed power on/off techniques achieves not only very high-speed power-up but also enhances the T/H's speed and linearity at high frequency. Moreover, a new rapid preamplifier power on/off method will also be introduced having the possibility of application in multi-stage preamplifier-chains.

The organization of the presented paper is as follows. Section II describes the overall architecture of the power-scalable flash ADC and introduces the corresponding timing diagram as well. The novel rapid power on/off circuits for both the T/H and the preamplifiers are presented in Section III. In Section IV the overall performance of the power-scalable flash ADC will be demonstrated by full transistor-level simulations, with the conclusions drawn in Section V.

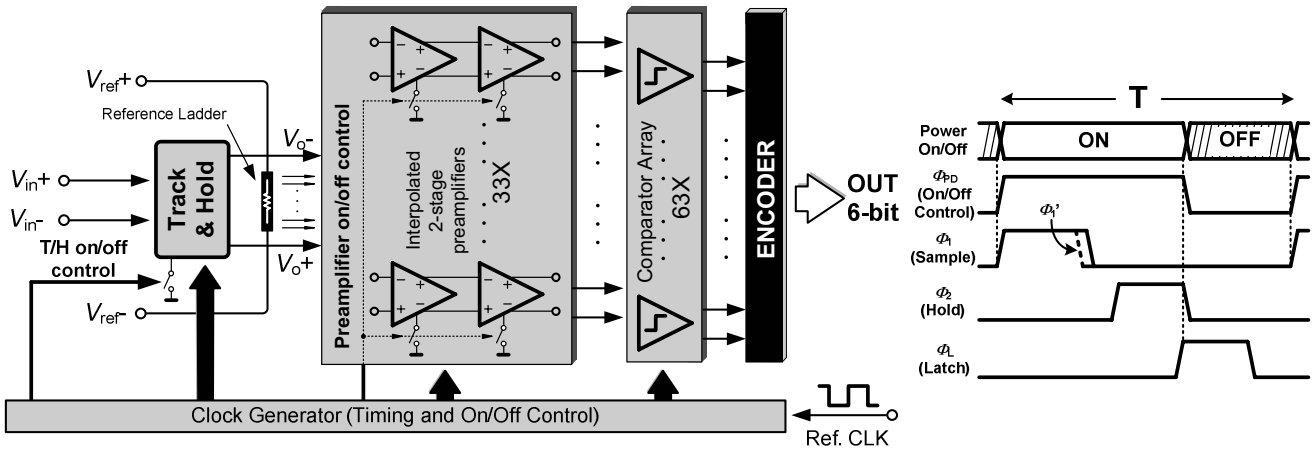
II. POWER SCALABLE FLASH ADC ARCHITECTURE

Although traditional flash converters could provide a viable solution for high-speed implementations their architectures exhibit a major drawback related with the large static power consumption of the track-and-hold circuit, the comparators' preamplifier chain and the reference resistive ladder.

Here, a novel flash ADC architecture is proposed, as shown in Figure 1(a), where the T/H and the pre-amplifiers are designed to allow power-down through the power on/off control signal. When the T/H is on (tracking) it samples the input, and, during the Hold phase the subsequent preamplifier will subtract the sampled signal from the reference voltage with the cooperation of a 32-taps resistive ladder. The 33 preamplifiers are interpolated to minimize the power consumption and designed with two-stages to achieve high amplification gain and to alleviate the comparator's offsets. Both the T/H and preamplifiers are optimized for 1.2 GS/s while at a lower sampling rate their powers are switched off after signal processing is completed. Each of the 63 dynamic latches is followed by a SR latch to generate a thermometer code. The final encoder will firstly transform the thermometer code into a Gray code, which is robust enough to tolerate the bubble error, and later into a binary code in every clock cycle.

Figure 1(b) shows the corresponding timing diagram of the proposed ADC where the T/H and the preamplifiers share the same power on/off control clocks to activate/halt the operations. The T/H samples the input in Φ_1 and maintains the output in Φ_2, while the preamplifiers sample the reference voltage from the resistive ladder in Φ_1 and subtract the signal from the T/H in Φ_2, on the other hand Φ_L is the strobe phase for the dynamic latches. It is important to emphasize that the power on/off control clock of the T/H (or the preamplifiers) starts immediately with Φ_1, which imposes that extra power-on time is not necessary, since the proposed T/H (and preamplifiers) is (are) powered on very rapidly. In addition, the average power of the ADC can be calculated as:

$$P_{avg} = P_{ON}\frac{t_{ON}}{T_S} + P_{fixed} \quad (1)$$



(a) (b)

Figure 1: Proposed Power-Scalable Flash ADC: (a) General architecture (with novel power on/ off control), (b) Corresponding timing-diagram.

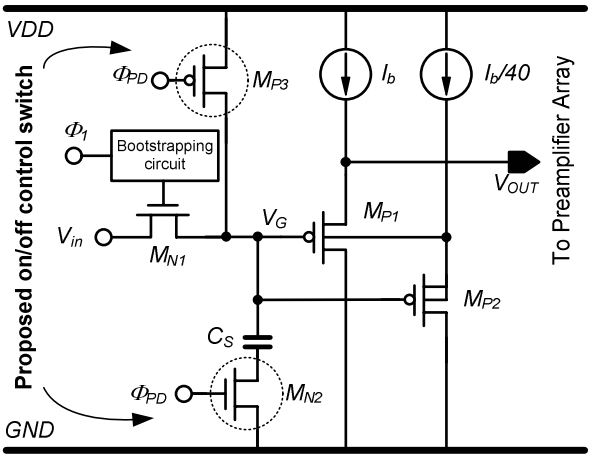


Figure 2: Proposed novel power on/off Track-and-Hold circuit.

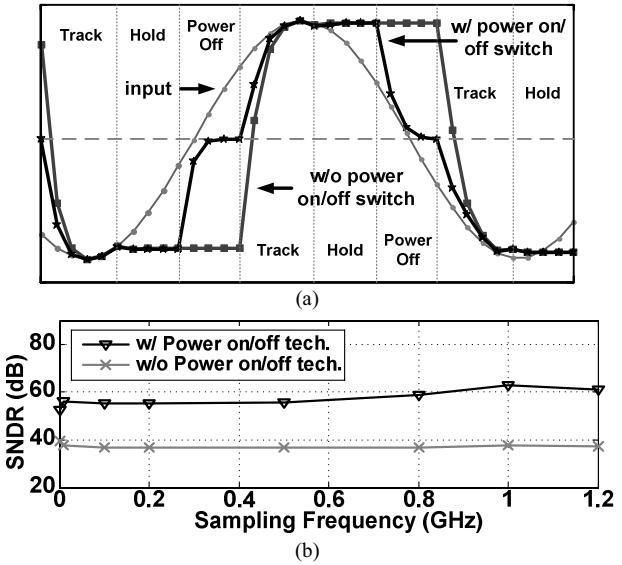


Figure 3: T/H operation w/ or w/o power on/off circuit : (a) transient and (b) simulated SNDR.

where, t_{ON} is the on time of the ADC, which is approximately the inverse of the maximum sampling rate of 1.2GS/s; P_{fixed} is the power consumption from the unscalable components (mainly from the resistive ladder); T_S is the scalable sampling period and P_{ON} is the power consumption during t_{ON} (excluding the P_{fixed}). Therefore, low power consumption is achieved at low sampling frequency, simultaneously with the ADC's power-scalability.

III. Proposed Rapid Power On/Off Circuits

The power-scalability of the proposed ADC is implemented with novel rapid power on/off circuit architectures, namely in the T/H and the preamplifiers:

A. Power on/off Track-and-Hold

A source-follower buffer based T/H circuit is widely used as the front-end of the flash ADC to achieve good dynamic performance by mitigating the problems of signal-dependent delay, sampling comparators aperture uncertainty, delays in the analog signal and the clock signal, and the resulting bubble errors [6]-[8]. In particular, for high speed applications the T/H circuit becomes essential.

Figure 2 shows the proposed T/H circuit with the respective rapid power on/off control. To achieve high linearity, bootstrapped switches [9] and replica-based well-biasing [8] techniques have also been included in the circuit implementation. The bootstrapped circuit can eliminate the signal-dependent charge injection from input sampling switch M_{N1}, thus ensuring accurate sampling in a very short time-frame. The replica branch draws only 1/40 current of the main source-follower achieving the reduction of the output capacitive load, and therefore increasing the tracking bandwidth, while simultaneously reducing the non-linearity induced by the body-effect [8].

A power on/off T/H is expected to avoid drawing static power when the T/H is at rest which can imply large power savings for applications where the T/H's working time-frame is much smaller than the whole period. The traditional method of powering down the T/H includes the addition of a series switch in the main source follower branch [7]. However, in the present high speed application the dc biasing current becomes quite large (4.4mA) which implies that an extra switch resistance would generate a large voltage drop, thus limiting the output swing and the linearity. Although a low-

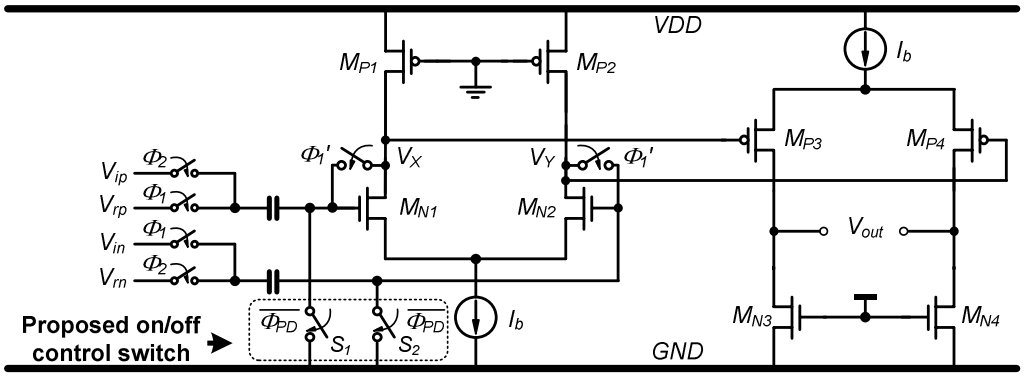


Figure 4: Circuit architecture of the proposed novel power on/off preamplifier.

resistance switch could be designed its consequently large size will slow down the speed.

The power on/off technique used here and shown in Figure 2 consists in adding a PMOS switch M_{P3} between the supply voltage and the gate of M_{P1}. When Φ_{PD} is reset, the gate of M_{P1} and M_{P2} will be pulled-up to V_{DD}, so M_{P1} and M_{P2} will go into cutoff region and therefore the bias current of the main source-follower and the replica branch will be cut-off. When Φ_{PD} is set, the M_{P3} is disconnected and the gate of M_{P1} is connected directly to the input.

During power down, M_{P3} will also pull-up the top plate of the sampling capacitor C_S, thus degrading the speed during power-down. To alleviate this problem, a NMOS switch M_{N2} is consequently added between C_S and the ground. When Φ_{PD} is reset, C_S will then float and the speed of the power-down transient can be improved since the source-follower doesn't need to discharge C_S.

Notice that this power-down operation will also contribute to the improvement in speed and linearity of the T/H circuit. As shown in Figure 3(a), without the power down method, tracking the input implies a significant time if the two sampled values of V_{IN} have a large voltage difference, which can be, in the worst case, equal to a full-scale input swing. However, when the proposed power-down method is applied, the differential voltage of V_G and V_{OUT} are reset to zero in each clock cycle. Thus, the output voltage varies from zero to V_{IN} after every period, implying that the maximum change of the output voltage will be half of the input swing and therefore the tracking time can be further reduced. On the other hand, with the same short tracking time, the T/H with power down operation can achieve higher SNDR (55-63 dB) than the normal T/H circuit (37-39 dB) as illustrated by the simulated results of Figure 3(b).

B. *Power on/off Preamplifier*

Preamplifiers provide sufficient gain to reduce offsets and kickback noise from comparators [6], [10], [11]. In the proposed ADC a two-stage preamplifier with interpolation and auto-zeroing is utilized to minimize the power consumption and comparator offset.

Figure 4 shows the circuit architecture of the two-stage preamplifier that basically operates in two phases, Φ_1 that is the sampling phase of the reference voltage also performing the auto-zeroing and Φ_2 which is the amplification phase when the difference between the input signal and the reference voltage is amplified. Besides these there is an additional phase Φ_1', similar to Φ_1 but having a falling edge that appears a little bit earlier than Φ_1 to alleviate charge-injection problems. Also represented in Figure 4 are the proposed power-down switches S_1 and S_2. To simplify the design as well as to improve the power-up speed, the two-stage preamplifier

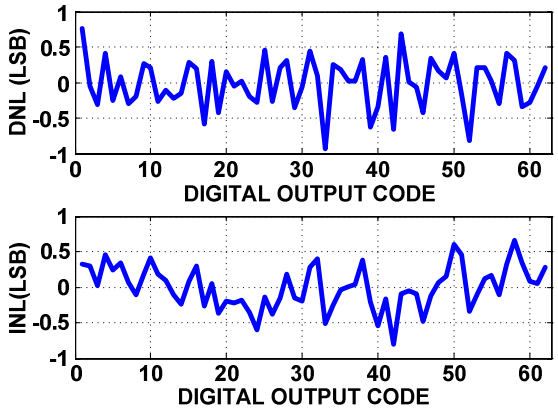


Figure 5: Simulated INL & DNL of the proposed ADC @ f_S = 1.2GS/s.

is specially implemented with a NMOS input pair in the first stage and a PMOS input pair in the second stage. When S_1 and S_2 close, M_{N1} and M_{N2} will be pulled down to ground and the current of the 1st stage differential pair is cut-off. The outputs of the first stage preamplifier (V_X and V_Y) are then pulled-up to V_{DD}. Since now the 2nd stage is a PMOS pair, M_{P3} and M_{P4} will then be cut-off and the current in the second stage preamplifier is also cut-off. Through a special arrangement of the N-type and P-type differential pairs both stages of the preamplifiers are powered-down by simple switches S_1 and S_2. The proposed preamplifier power-down method uses only two switches and powers on/off very fast also because no series switches are added with the current sources. Furthermore, the proposed technique can be extended to multi-stage preamplifier power-down operation where the N-type and P-type preamplifiers are used alternatively.

IV. Simulation Results

The proposed power-scalable flash ADC with power on/off T/H and preamplifier has been simulated at full transistor-level using a 90nm CMOS process. Figure 5 presents the simulated INL (-0.9/+0.7 LSB) & DNL (-0.8/+0.6 LSB) and Figure 6 shows a frequency spectrum from one case of the Monte-Carlo simulation @ f_{in} = 563 MHz and f_S = 1.2 GS/s, with 33dB SNDR and 44dB SFDR. Figure 7 shows the histogram of 100 times Monte-Carlo simulations where the SNDR achieves a mean of 32.5 dB. Figure 8 presents the SNDR obtained also from a Monte-Carlo simulation versus input frequency at 1.2 GS/s to demonstrate that the proposed ADC can achieve an Effective-Resolution Bandwidth (ERBW) of 8.3 GHz. Finally, Figure 9 illustrates the power and SNDR of the ADC versus the sampling rate variation from 1 MS/s to 1.2 GS/s, comparing with the power

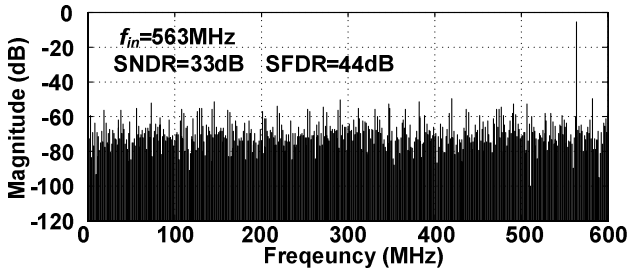


Figure 6: FFT of the digital output @ f_{in} = 563MHz and f_S = 1.2GS/s.

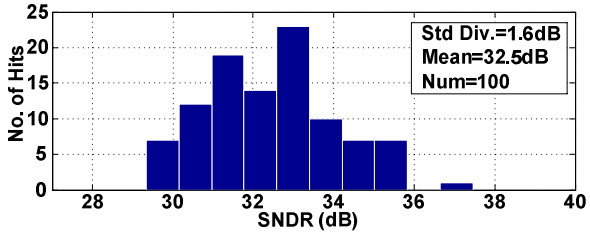


Figure 7: Histogram of SNDR of proposed novel ADC @ f_{in} = 563MHz and f_S = 1.2GS/s.

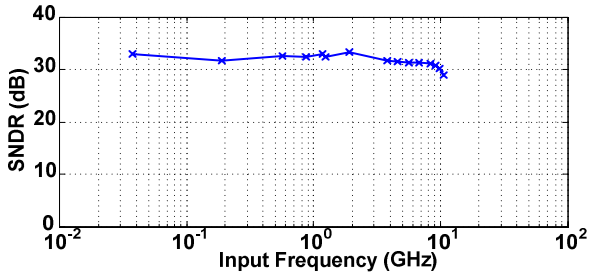


Figure 8: Simulated SNDR versus input frequency @ f_S = 1.2GS/s.

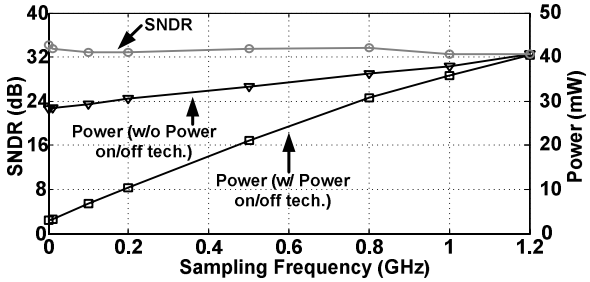


Figure 9: A plot of ADC power and SNDR versus sampling rate.

consumption in the two alternative cases, with and without the proposed power on/off controls. In the latter, the power consumption is scaled from 3 mW to 41 mW while maintaining the SNDR of 32-34 dB. Because of the dynamic architecture, the ADC's power consumption scales almost linearly and power scalability is achieved demonstrating the effectiveness of the proposed architecture. At the maximum sampling rate of 1.2 GS/s with a Nyquist input and applying the typical FOM definition for ADCs,

$$FOM = \frac{Power}{2^{ENOB} \cdot f_S} \tag{2}$$

the FOM of the proposed ADC is calculated to be 0.9 pJ/conversion-step. Table I summarizes the overall performance of the ADC.

V. CONCLUSIONS

This paper presents a power scalable 6-bit 1.2GS/s flash ADC with power on/off controls applied both in the T/H and preamplifiers.

Technology	90nm CMOS	
Resolution	6-bits	
Input Range	1.2 Vpp (0.3 Vcm)	
DNL @ fs=1.2GS/s	-0.9 / +0.7 LSB	
INL @ fs=1.2GS/s	-0.8 / +0.6 LSB	
ERBW @ fs=1.2GS/s	8.3GHz	
Sampling Frequency	1.2GS/s	500MS/s
Input Frequency	563MHz	234MHz
ENOB	5.2bit	5.4bit
SNDR	33dB	34dB
SFDR	44dB	45dB
Power	40.5mW	21.1mW
Supply voltage	1.2V	

TABLE I: PERFORMANCE SUMMARY OF THE PROPOSED NOVEL ADC

By powering down the T/H and preamplifiers the ADC exhibits lower power consumption (excluding the resistive ladder) after the signal processing is completed and thus achieving power-scalability. The performance of the proposed ADC is demonstrated through simulation in a 90nm CMOS process, from 1 MS/s (3 mW) to 1.2 GS/s (41 mW) while maintaining the SNDR of 32-34 dB and achieving 0.9 pJ/conversion-step FOM at maximum sampling rate.

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