A 100MS/s recycling 2-step ADC embedding Programmable Gain Amplification for DVB Satellite

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***Abstract* — A 100MS/s, 6-bit recycling two-step analog-to-digital converter (ADC) with an embedded programmable gain amplification function is designed in 0.18-μm CMOS, being suitable for use in digital video broadcasting – satellites (DVB-S). In the proposed ADC, a programmable gain amplifier (PGA), a sample-and-hold amplifier (SHA) as well as a multiplying digital-to-analog converter (MDAC) are combined and merged into a single switched-capacitor (SC) block, thus providing good savings in terms of power and silicon area implementation. The proposed embedded PGA function optimizes efficiency in A/D conversion according to the dynamic input signal requirement of the DVB-S application. Full transistor-level simulation is provided for the ADC with 35-dB SNDR and 41-dB SFDR at 100 MS/s, and the DNL and INL are within ±0.6 and ±0.5 LSB, respectively. The proposed ADC consumes only 12 mW from a 1.8-V power supply.**

I. INTRODUCTION

The increase in demand for higher visual-audio quality is implying now a gradual replacement of traditional TV broadcasting by Digital Video Broadcasting (DVB). Here, an analog-to-digital converter (ADC) design for DVB-satellite (DVB-S) transmission [1] will be addressed. For the application concerned the ADC is required to have a sampling frequency of 100MS/s and a resolution of 6 bit. In a full flash ADC architecture the number of comparators grows exponentially to 2^N for an increasing resolution N, which would be translated directly into exponential growth of the die area, power consumption and input capacitance. Alternatively, a two-step ADC architecture will be chosen as an optimized solution [2-5] with $2*2^{N/2}$ comparators with the consequent savings in power, area and input capacitance.

Since the amplitude of the signal received from the tuner may not correspond to the full scale of A/D conversion, due to attenuation in the transmission path, a Programmable Gain Amplifier (PGA) needs to be added before the ADC, as shown in Fig.1, which will be one of the most power-thirsted components in the whole system. To overcome this problem a new circuit architecture is presented where the PGA function is embedded into the ADC. Then, the two-step ADC is designed with a recycling two-step architecture that includes the switched-capacitor Sample-and-Hold (S/H) and the Multiplying Digital-to-Analog-Converter (MDAC) [2], as well as embedding the PGA function.

In this paper, a detailed description of the overall ADC architecture and the key techniques for minimizing the power consumption are provided in Section II. A circuit-level design of the combined PGA/SH/MDAC function in the two-step ADC will be presented in Section III. In Section IV transistor-level simulation results will demonstrate the performance of the ADC and finally the Conclusions are drawn in Section V.

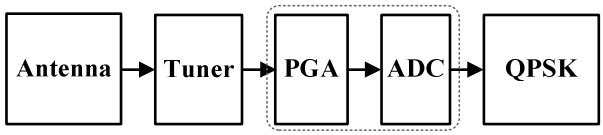

Fig.1 Receiver block diagram of a DVB-S system

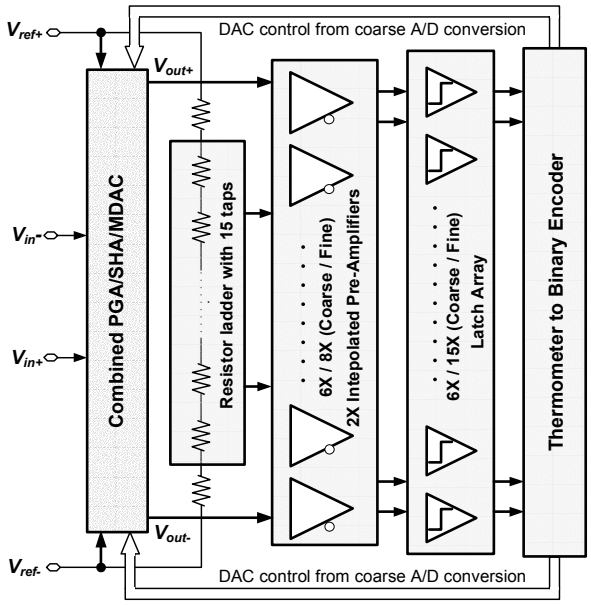

Fig. 2 Proposed ADC architecture

II. PROPOSED ADC ARCHITECTURE

Fig. 2 shows the proposed recycling two-step ADC using a capacitor-array MDAC. The MDAC not only replaces the usual functions of the S/H amplifier, the DAC and the residue amplifier [2], but also contains an embedded PGA. The resistive ladder subdivides the reference voltage scale into 2^4 voltage levels, which are compared with the analog output of the MDAC in the

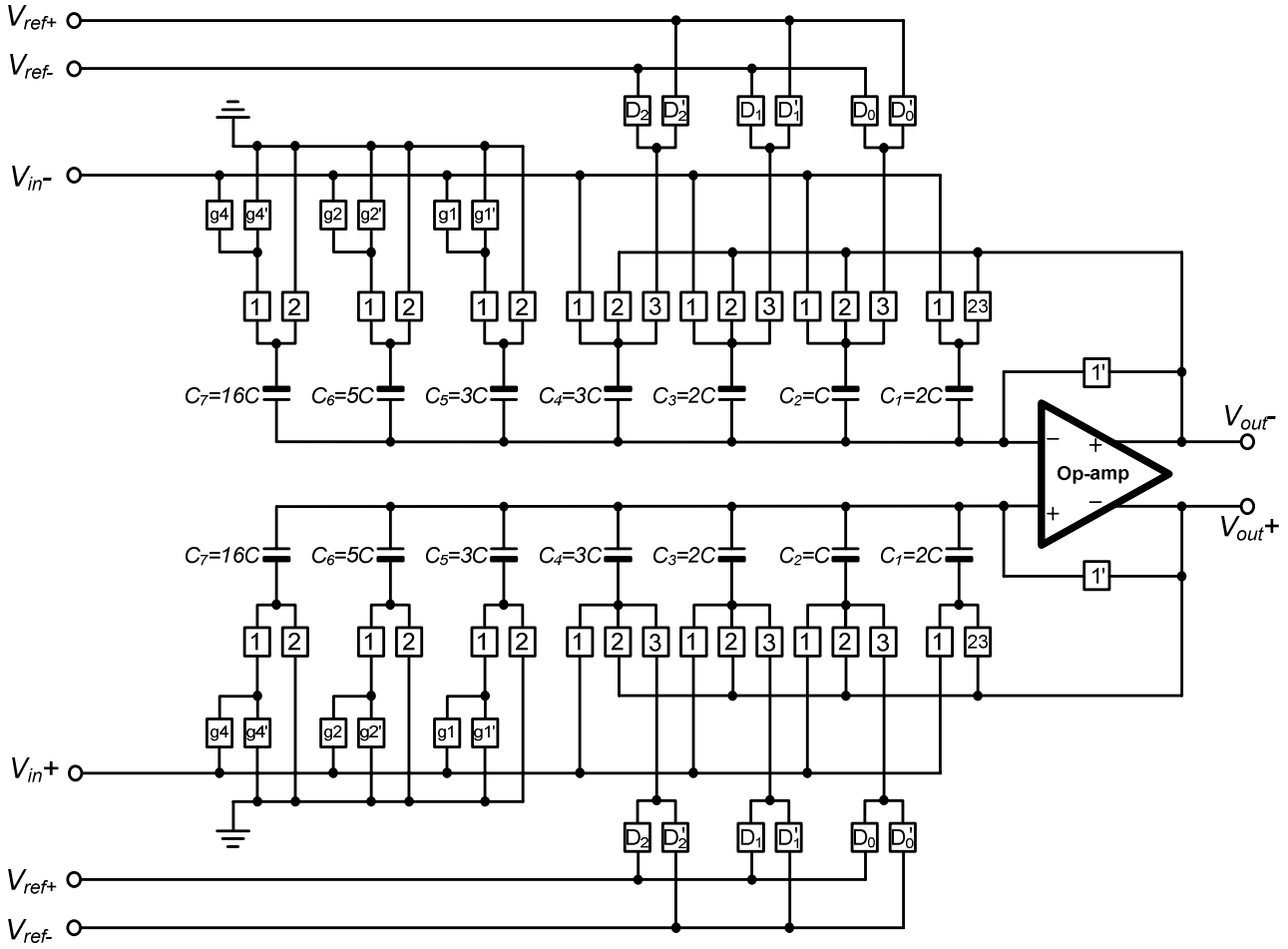

Fig. 3 The proposed combined PGA/SH/MDAC with embedded programmable gain amplification

TABLE 1: TRUTH TABLE OF PGA GAIN CONTROL LOGIC

	PGA gain	B1	B0	g4	g2	g1
1	**1**	0	0	0	0	0
2	**1.375**	0	1	0	0	1
3	**2**	1	0	0	1	1
4	**4**	1	1	1	1	1

subsequent preamplifiers. The six preamplifiers and 15 latches comprise the 2.8-b coarse stage [5] of the two-step ADC, where the 2.8-b technique is applied to simplify the digital error correction algorithm, so that only add-one process of the coarse and fine bits is needed. The fine stage includes 8 interpolated preamplifiers and 15 latches. The interpolation has been adopted to reduce the number of preamplifiers and to minimize power consumption [6]. The same set of preamplifiers and latches can operate through adequate switching in coarse or fine stages. An encoder including digital error correction logic combines the coarse and the fine bits together and converts them from thermometer code to binary code in each clock cycle.

III. CIRCUIT IMPLEMENTATION

The proposed ADC contains several building blocks which can be implemented as presented next:

A. Combined PGA/SH/MDAC

The proposed MDAC shown in Fig. 3 has a three operating phases: sampling, hold and amplification, corresponding to the number 1, 2 and 3, respectively. The phase 1' is litter bit shorter than phase 1 and phase 23 indicates an OR function of phase 2 and 3. In Fig.2, the feedback factor in the 3 different operating phases will be different, thus the opamp must be designed to guarantee stability with an appropriate phase margin (in this case 57°) In the capacitor array C_1 to C_4 realize the DAC function and instead of using a binary-weighted capacitor array, the 3 capacitors connected to the digital input are 3C, 2C, 1C. Since the 2.8-bit technique is used the 6 comparators in the coarse stage are implemented with the total capacitance of 6C from these 3 capacitors. For example, supposing that N of the 6 comparators outputs are at the digital-level '1' in the coarse A/D conversion phase, the transfer function between the 2nd and the 3rd phase will be:

$$8 \cdot V_{in} = 2 \cdot V_{out} + N \cdot V_{ref+} + (6 - N) \cdot V_{ref-} \qquad (1)$$

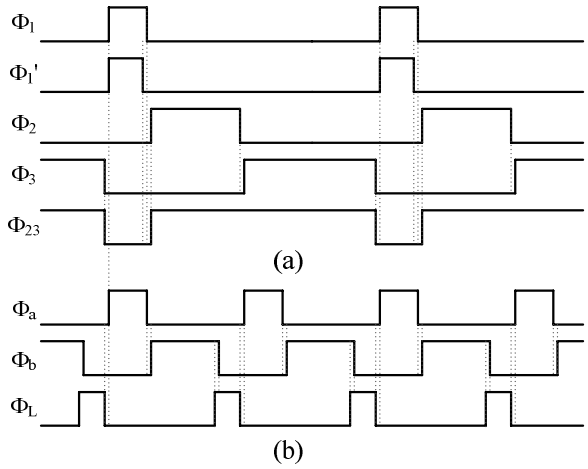

Fig. 4 Time diagram of (a) MDAC and (b) Quantizers

TABLE 2: 3-BIT DAC CONTROL CODE

In Decimal	DAC Control Code	Binary Code
6	111	110
5	110	101
4	101	100
3	011	011
2	010	010
1	001	001
0	000	000

On the other hand, the capacitor connected to the output is chosen as 2C in order that the sum of C_1 to C_4 is still a binary value, 2^3. Although doubling this capacitor will reduce the residue amplification gain to 1/2 and the fine comparators have to be designed to have higher resolution, the opamp's requirements can now be relaxed since the output voltage swing will be reduced. The accuracy of the fine comparators is also guaranteed by the pre-amplifiers.

The second phase (2) of the MDAC is originally a hold phase but here it corresponds also to an amplification phase with a selectable PGA gain of 4, 2, 1.375, and 1, for an input signal range between 0.25 and 1 to guarantee a full A/D conversion scale. Gains of 4, 2 and 1.375 can be obtained by adding 16C, 5C and 3C capacitors in phase 1, where their selection can be controlled by a 2-bit digital input. As shown in Table 1, the 2-bit digital input B1 and B0 will be transferred to control the switch g4, g2, g1 and their inverse by digital logic gates. Moreover, the capacitors C_5 to C_7 are floating in the third phase (3) to reduce the feedback factor so as to increase the close-loop gain and enhance the charging speed. Therefore, the bottom plate terminals of these capacitors have to be shielded carefully during the layout design.

From the timing diagram of Fig. 4(a) the pulse width of the clock-phases Φ_1, Φ_2, and Φ_3 are designed to be 1.7 ns, 3 ns, and 4.8 ns, and they can be generated from a reference clock using gm / C delay circuits [2]. Φ_1' must be a little shorter than Φ_1, with a pulse width of 1.6 ns to avoid charge injection. Φ_{23} is obtained from an

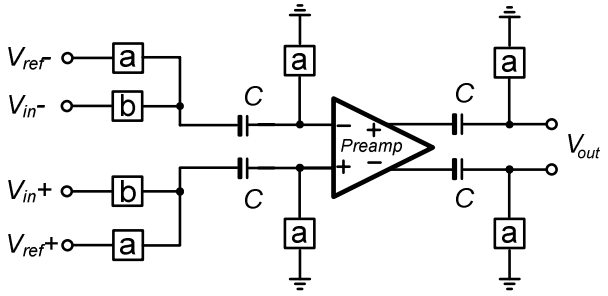

Fig. 5 Comparator with offset cancellation.

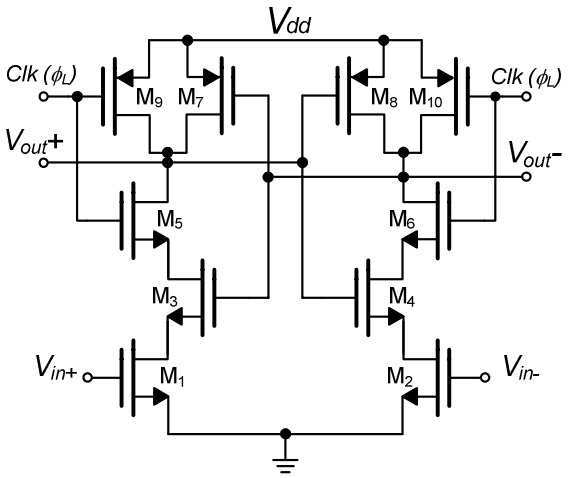

Fig. 6 CMOS implementation of the Latch.

OR function of Φ_2 and Φ_3 applied to the feedback 2C capacitor since it is connected to the output of the MDAC in both phases (2) and (3).

B. Comparator and Latch

The interpolation technique reduces the number of pre-amplifiers and then it will minimize the input capacitance, power consumption and die area of the ADC [6]. The circuit implementation of the comparator is depicted in Fig. 5, where the pre-amplifier, in open-loop connection, suffers from the offset voltage existing between its input pair. Therefore, a switched-capacitor circuit has to be added for offset voltage cancellation [7]. After the comparator subtracts the input signal from the reference voltage, the latch rapidly pulls the residue signal to V_{dd} or ground, by using a positive feedback. The dynamic latch circuit is shown in Fig.6, where there is a differential output but only the positive terminal is used since the inverse of the digital code is not necessary. The time diagram of the clocks in the comparator and latch are shown in Fig 4(b). Φ_b is non-overlapping with Φ_a but it overlaps with Φ_L.

C. Encoder

The encoder is basically composed by a digital logical code transferring system, with a particular aspect to be highlighted. At the end of the coarse A/D conversion, the encoder converts the thermometer code to the 3-bit DAC Control Code and forwards it to the MDAC for the fine A/D conversion. Since the capacitance array realizing the DAC function is not binary-weighted, the DAC control code can no longer be a binary code. Table 2 presents the 3-bit

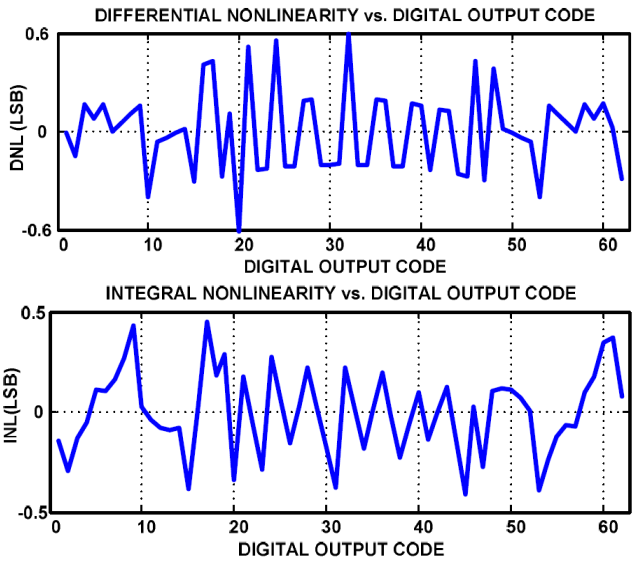

Fig. 7 Simulated DNL and INL of propose ADC at PGA Gain= 4

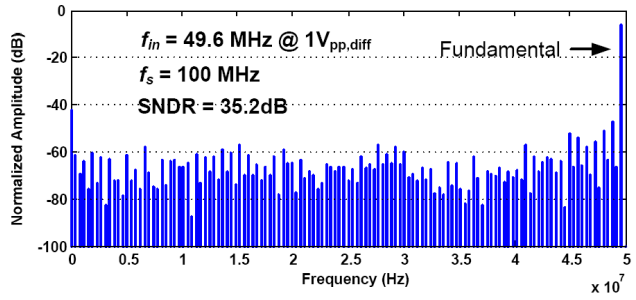

Fig. 8 FFT of a 49.6 MHz input signal sampled at 100 MS/s

DAC Control Code where a '1' needs to be added if its MSB is a digital '1'.

IV. Simulation Results

The proposed PGA shared recycling 2-step flash ADC was implemented using a 0.18-µm CMOS process and it was simulated at transistor-level. The PGA shared function has been verified by Spectre simulator for different PGA gains. To demonstrate the ADC's efficiency its performance with a PGA gain of 4 is typically referred here, since the effect of non-idealities such as mismatch or gain error will reach their maximum under this condition. Fig. 7 shows the simulation result of DNL and INL for a single case of Monte-Carlo simulations, where DNL is within ±0.6 LSB and INL is within ±0.5 LSB. Fig. 8 shows the dynamic performance of the whole ADC, with the SNDR of 35 dB @ f_{in} = 49.6 MHz and f_s = 100 MHz, thus verifying the functionality of the proposed PGA/SH/MDAC combined ADC. Table 3 summarizes the overall performance of the ADC.

V. Conclusions

In this paper, a PGA shared 6-bit 100-MS/s recycling two-step flash ADC has been presented. An embedded PGA/SH/MDAC function was proposed together with interpolation in the comparator stage to achieve power optimization. In the worst case condition of a PGA gain of 4, the DNL is ±0.6 LSB and INL is ±0.5 LSB with ENOB = 5.5 bit. Table 3 shows that the ENOB increases when PGA gain decreases, which demonstrates the previous assumption. The ADC including the clock generator consumes 12mW.

Table 3: Summary of the Proposed ADC

Sampling Frequency		100 MS/s
Resolution		6 Bit
Input Range		1 V_{PP}
Input frequency		49.6 MHz
ENOB	**(@ X1 PGA Gain)**	5.6
	(@ X1.375 PGA Gain)	5.6
	(@ X2 PGA Gain)	5.6
	(@ X4 PGA Gain)	5.5
SFDR	**(@ X4 PGA Gain)**	41 dB
DNL	**(@ X4 PGA Gain)**	±0.6 LSB
INL	**(@ X4 PGA Gain)**	±0.5 LSB
Power Consumption*		12 mW

*: Including clock generator and biasing circuits

Acknowledgment

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