A 1-V 2.5-mW Transient-Improved Current-Steering DAC using Charge-Removal-Replacement Technique

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***Abstract* – A charge-removal-replacement (CRR) technique is proposed to realize a low-voltage low-power current-steering digital-to-analog converter (DAC) for minimizing transition time in current switching. Implemented in a 0.18-µm CMOS process, the 10-bit 120-MS/s DAC focused on WLAN applications consumes only 2.5 mW from a single 1-V supply. The simulated monotonic performances achieve a mean value of |INL| < 0.14 LSB and |DNL| < 0.18 LSB, respectively. The averaged SFDR obtains 67.23/62.45 dB with/without the CRR technique.**

I. Introduction

The demand for high performance digital-to-analog converters (DACs) has obviously increased for the fast development of advanced telecommunication systems, e.g., wireless local area networks (WLANs). In view of that, most of data converters are desired to be fully integrated into a CMOS System-On-a-Chip (SoC) wireless transceiver with including RF transceiver, digital physical layer (PHY), corresponding media access controller (MAC) and all other analog baseband building blocks [1]. To avoid any supply-voltage constraints for the technology scaling, low-voltage building blocks with low-power consumption is highly required.

In practice, current-steering DAC is preferred for wireless communications due to its high sample rate, capability of driving resistive loads and relatively low-power consumptions. The current cells with cascoded topologies as shown in Fig. 1 are satisfactory for static and dynamic output-impedance requirements [2]-[3]. Alternatively, the cascoded-switch topology [4] presents as additional digital signal feedthrough isolation and output influence reduction through the insertion of two cascoded transistors (M_{cas+} and M_{cas-}). However, asymmetry in rising-falling transitions and long settling time will degrade the dynamic performance directly, especially applied in high speed and high resolution DAC which unit current is small. This paper proposes a *charge-removal-replacement* (CRR) technique that fixed those transient problems. For demonstrated purposes, a 1-V 10-bit 120-MS/s DAC with less than 1.3-µA unit current was designed and simulated, the current switching transient is highly reduced and the dynamic performances of the DAC are dramatically enhanced.

After this introduction, the proposed CRR technique will be presented in section II. In section III, it will be applied to a low-voltage current-steering DAC with a detailed description of each building block. In section IV, simulation results will be presented. Finally, the conclusions will be summarized in section V.

II. Charge-Removal-Replacement Technique

The main disadvantages of the conventional cascoded-switch current source (CSCS) topology are the long settling time and asymmetry settling time (falling settling time is slower than that in rising), which distorting output current of the DAC. The tarry falling settling time is caused by the node voltage, which below the off switch (M_{sw+}/M_{sw-}), is discharged exponentially until the

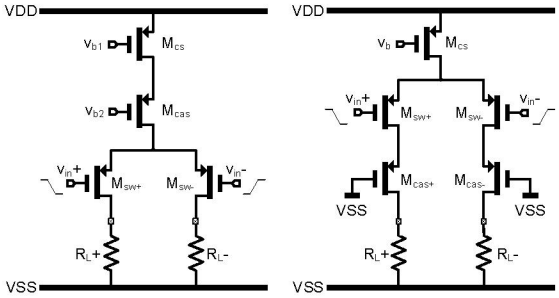

Fig. 1 (a) Cascoded-current-source and (b) cascoded-switch topology.

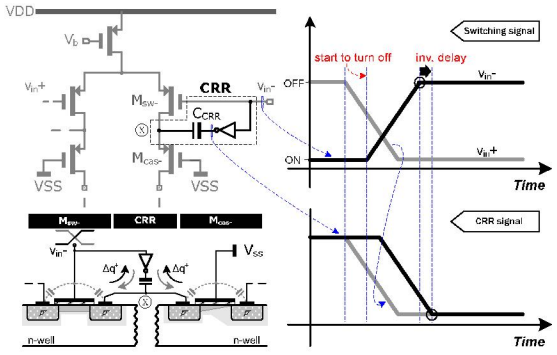

Fig. 2 (a) Operational principles of CRR technique and (b) the corresponding control signals.

cascoded switch (M_{cas+}/M_{cas-}) enters in the subthreshold region. As a result, an amount of current leaks into the path even if the corresponding switch is in the off stage. Such current is given by the subthreshold expression of the drain current (I_D),

$$I_D = I_0 \exp\frac{V_{SGcas}}{\varsigma V_T} \qquad (1)$$

where ς>1 is a nonideality factor and $V_T = kT/q$. Moreover, with parasitic capacitance present in the source terminal of cascoded-transistor M_{cas+}/M_{cas-}, the transition will be further extended.

Operational Principles – The CRR technique is depicted in Fig. 2(a), where a capacitor (C_{CRR}) driven by an inverter is inserted between the gate and drain terminals of the switched transistor. When the desired switch is turning off, the inverter generates an inverted control signal to draw out the positive charge (Δq^+) from the inversion layer and the ubiquitous parasitic capacitance at node X, such that any lengthy discharge procedure can be eliminated.

To avoid current sources from being turned off simultaneously, digital control signals with lower crossing point apply to the switch

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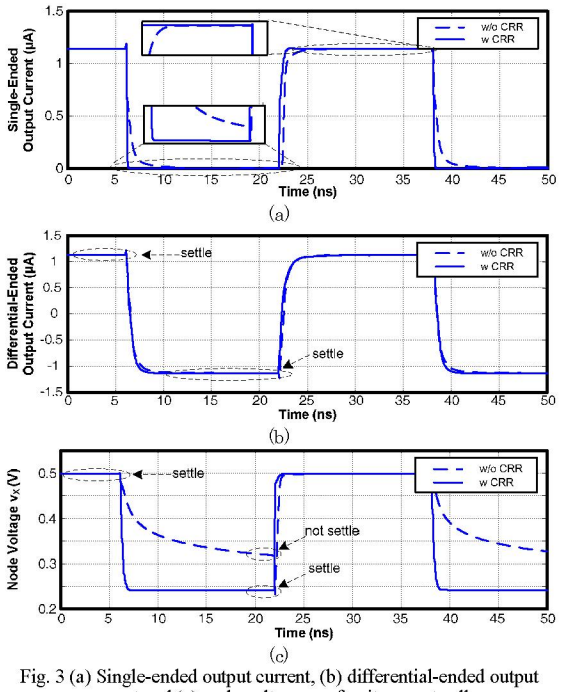


Fig. 3 (a) Single-ended output current, (b) differential-ended output current and (c) node voltage v_X of unit current cell.

inputs [Fig. 2(b)]. If the switching control signals directly cross-couple to the capacitor C_{CRR}, the charge Δq^+ will draw continuously when the path is turned off. Thus, the inverter is necessary required to generate a delayed control signal to balance the falling and rising transitions.

Timing Benefits – Two advantageous features are summarized below:

(a) Balanced Speed and Advanced Transition: The CRR technique improves the rising transition by replacing some positive charge, given that the node voltage v_X is faster settling to its steady-state value while the current path is turning on. On the other hand, when the current path is desirable turned off, the CRR technique removes the residual charge and prompts the node voltage v_X to steady state (i.e., v_X is leaded to reduce). Therefore, the cascoded switches no longer suffers from the critical exponential discharge problem, establishing balanced falling and rising speeds. As illustrated in Fig. 3(a), the falling transition of a single-ended output current is enhanced in terms of speed to achieve more balanced rising-falling characteristic. Even though a differential-ended output signal [Fig. 3(b)] can suppress even-harmonic distortion in the conventional CSCS structures, the transient nonlinear problem still exists, which can be solved by the CRR technique presented.

(b) Recovered Synchronization for Each Current Source: In the current-steering DAC, the digital control input signals switch the correspondent current paths on/off. Delay differences among active current paths create an input-data-dependent nonlinearity and increase the susceptibility to asynchronous glitches. The conventional CSCS endures input-data-dependent delay even the clock nets are perfectly synchronized. The reason is the node voltage v_X requires a long settling time, even though the output current has already settled [Fig. 3(b) and (c)]. The node voltage v_X,

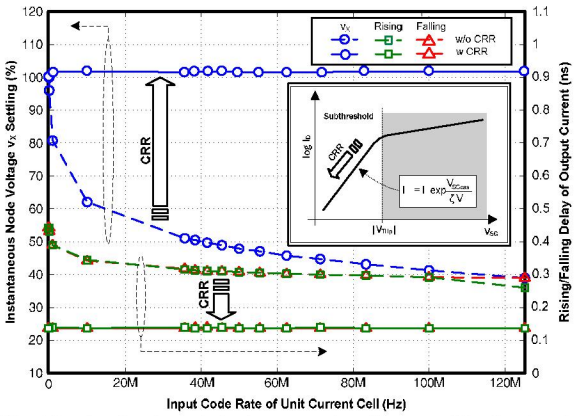


Fig. 4 Input code rate vs. instantaneous node voltage v_X settling level, and rising/falling delay of differential output current.

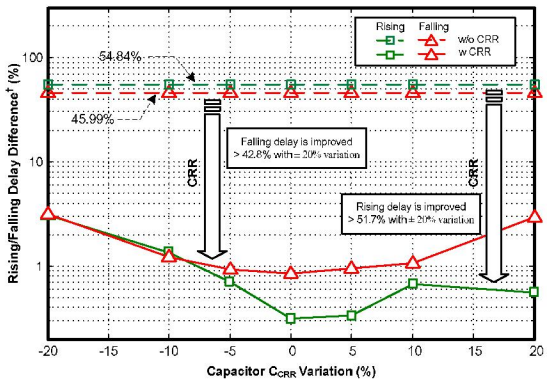


Fig. 5 Rising/Falling delay with capacitor variation.
(†: Calculated by [*different*] / [*average*] in the range of input code rate.)

thus, requires different charging time in every clock cycle, resulting in a non-constant rising delay for switching on the current path. As shown in Fig. 4, the CRR technique reduces the variation of v_X from the steady-state voltage for different switching rates, and it also leads the rising/falling delays of the differential output currents to be more independent of the input code rate. In fact, the difference between rising/falling delays is dependent on the capacitance of C_{CRR}. With capacitor variation, the performance is slightly degraded as shown in Fig. 5. However, the improvement is still significant when comparing with the performance of conventional structures. Furthermore, pushing the cascoded switches to the deep subthreshold region can eliminate the induced current, such that the accuracy of the D/A conversion will not be degraded.

Output-Impedance Influence – The output impedance of the current source affects both the static and dynamic linearity of the DAC. The output resistance of CSCS is given by [3],

$$R_{out} = g_{mcas} g_{msw} r_{0cas} r_{0sw} r_{0cs} \quad (2)$$

and the output impedance (Z_{out}) has two poles and two zeros as:

$$p_1 = \frac{1}{2\pi r_{ocs} C_0} \quad p_2 = \frac{1}{2\pi r_{osw} C_1} \quad z_1 = \frac{g_{msw}}{2\pi C_0} \quad z_2 = \frac{g_{mcas}}{2\pi C_1} \quad (3)$$

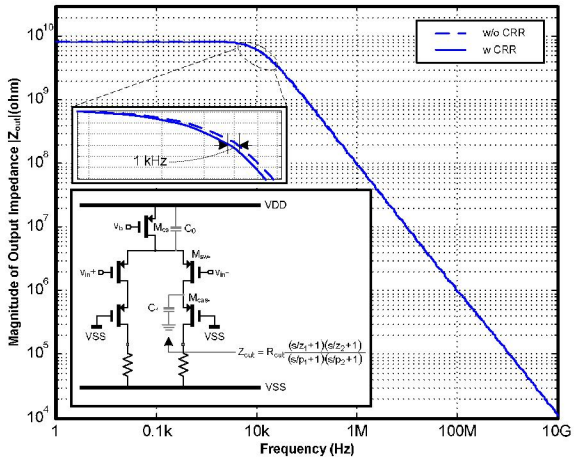


Fig. 6 Output impedance with and without CRR.

where g_m and r_o are the transconductance and output resistance of the corresponding transistors, respectively, as noted in Fig. 6.

The CRR technique inserts an additional capacitor C_{CRR} into the current cell, which is equivalent to an increase of the capacitance C_1 and a frequency shifting of the pole p_2 to a lower value. As illustrated in Fig. 6, this effect can be neglected (i.e., only 1-kHz difference) because the add-on capacitor C_{CRR} is typically small in size.

III. Design Example

A 1-V 10-bit 120-MS/s fully binary-weighted current- steering DAC with the CRR technique was designed for WLAN applications. The floor plan is shown in Fig. 7, where the circuit consists of a set of digital input buffer, a clock driver, a biasing circuit, a switch & latch array (SWATCH), and a current-source array (CSA). Utilizing a transimpedance output stage [5], which has a lower input impedance node, improves static and dynamic linearity concurrently. However, this current-to-voltage buffer is normally required to drive a smaller feedback resistor, imposing large power dissipation. For power saving, instead of using the transimpedance output buffer, the designed DAC drives a resistive load (R_L) directly [6].

Current Source Array (CSA) – In the conventional current-steering DAC, the segmented architecture improves the DNL and glitch performance by using more unary decodes. However, increasing the use of unary decoding occupies large chip area, increases power, digital noise, time skews and design complexity. In the design of a 10-bit DAC with an equal structure and a fully binary decode [7] is more attractive to achieve low power, high accuracy, linearity and speed, as well as size compaction.

The matching is critically determined by the area of the unit current source. In the behavioral-level simulation, a maximum relative standard deviation (σ_u/I_u) of a unit-current source is 0.2% for correct INL and DNL yields (99.7% yield for |INL| and |DNL|< 0.5 LSB). In fact, σ_u/I_u of a binary-weighed DAC is normally determined from the DNL yield. The minimum area $(W\cdot L)_{min}$ of the unit current source is estimated by [8],

$$(W \cdot L)_{min} = \frac{1}{2 \cdot (\sigma_u / I_u)^2} \left[A_\beta^2 + \frac{4 A_{VT}^2}{(V_{GS} - V_T)^2} \right] \qquad (4)$$

where A_β and A_{VT} are the matching parameters, and $(V_{GS}-V_T)$ is the overdrive voltage of the current source transistor.

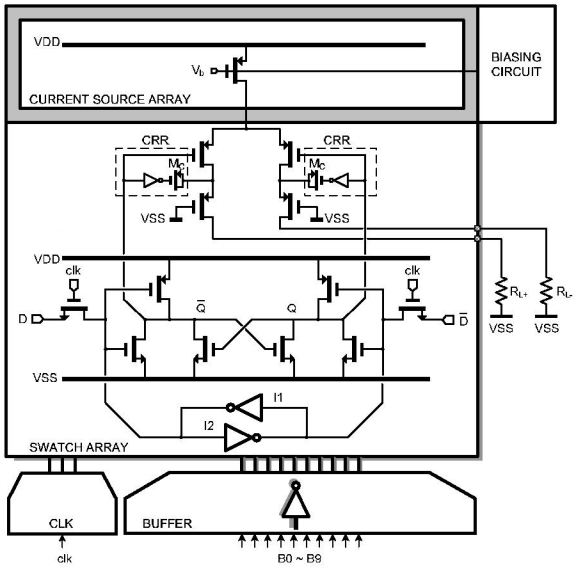


Fig. 7 Floor plan of the designed fully binary-weighted DAC.

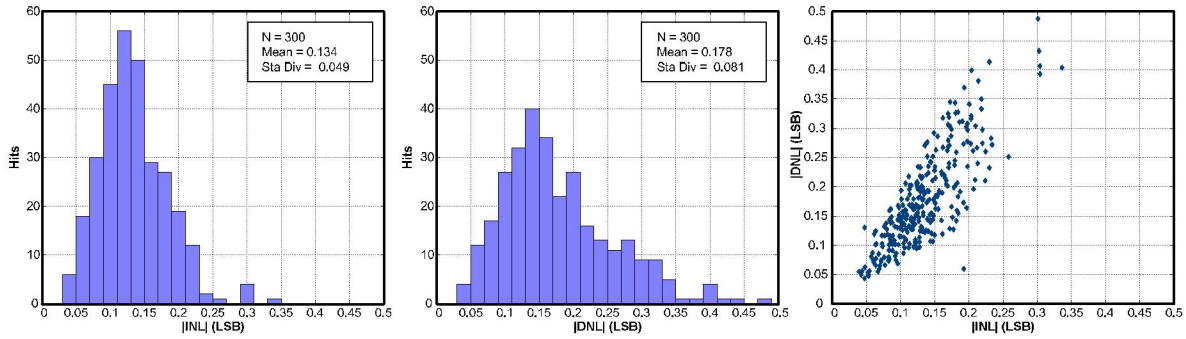
Switch + Latch (SWATCH) – The switch array of the DAC is constructed by cascoded switches to enhance the output impedance of the current sources. In practice, the length of the input (L_{sw}) and cascoded (L_{cas}) switches is chosen at minimum length to further reduce the digital feedthrough. Beside the effect of finite output impedance, the dynamic performance of a current-steering DAC is mainly limited by the imperfect synchronization of the control signals and the drain-voltage variation of the current source. For lowering the glitch errors as the current is switched to the desired output, it is essential that the driving signals exhibit a lower crossing point. The rise/fall-time-based latch [9] has been exploited for its high-speed capability [Fig. 7], and NMOS positive feedback loop exhibits a faster fall than rise time of the latch. Moreover, an additional feedback using small inverters (*I1* and *I2*) reduces the clock-feedthrough (CFT).

The CRR technique is embedded into the swatch array, and the PMOS capacitor (M_C) is utilized instead of capacitor C_{CRR} for area saving. In this way, not only the charge injection is reduced (similar to a dummy switch), but also removed/replaced the positive charge while improving the transient characteristic and dynamic performances.

In the designed DAC, the full-scale current is 1.25 mA and the resistive load R_L is 200 Ω. The resulted differential peak-to-peak output voltage is 0.5 V.

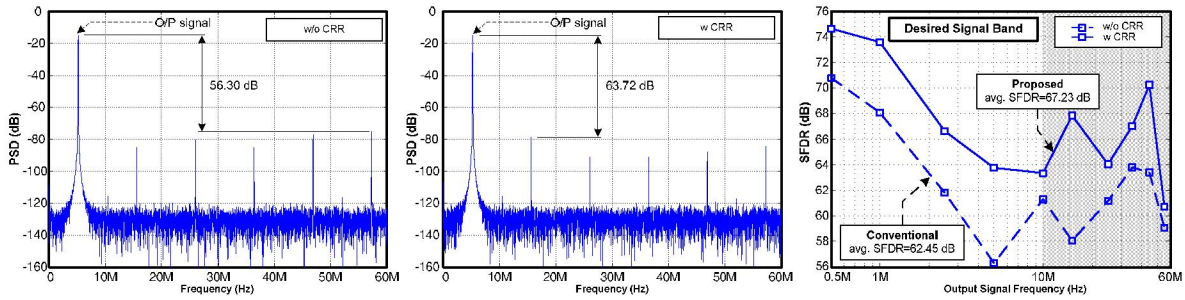
IV. Simulation Results

A 1-V 10-bit DAC simulated using 0.18-μm CMOS technology was designed to demonstrate the above technique. To evaluate the static linearity performance of the DAC, 300-time INL and DNL Monte-Carlo simulations are illustrated in Fig. 8(a) and (b), respectively. The statistical histograms show that the |INL| and |DNL| exhibit a [*mean, standard deviation*] of [0.134, 0.049] and [0.178, 0.081] LSB, respectively. The scatter plot obtained from the same Monte-Carlo simulations [Fig. 8(c)] clearly shows that the required specifications are met with the appropriate margin. As mentioned, the CRR technique can improve the switching behavior of the current cells. In order to compare the dynamic performance between the conventional and the proposed technique,



(a) (b) (c)

Fig. 8 Histogram of (a) INL, (b) DNL and (c) scatter plot of INL vs. DNL from a 300-time Monte-Carlo simulation.



(a) (b) (c)

Fig. 9 Simulated output spectrum at 5 MHz, 120 MS/s (a) without and (b) with CRR technique. (c) SFDR vs. output signal frequency.

the output spectrums are presented in Fig. 9 (a) and (b), respectively. With the new technique, the averaged SFDR is improved by 4.78 dB within the Nyquist band [Fig. 9(c)]. A summary of the simulation performances is listed in Table 1.

V. Conclusion

This paper presented a *charge-removal-replacement* (CRR) technique for improving the transient performances of current-steering DACs. Adopted in a 1-V 10-bit 120-MS/s fully binary-weighted current-steering DAC, the technique removes (replaces) the node charge when the desired current path is turned off (on). The discharging (charging) time is reduced leading to a higher speed in D/A conversion. Compared with the conventional cascoded-switch current source (CSCS) topology, the switching transition, asymmetry rising-falling settling and synchronization problems are minimized with negligible power (< 0.15 mW) and chip area overheads. In average, 4.78-dB improvement in SFDR is achieved within the Nyquist band.

Table 1 Summary of the DAC performance.

Specification	Unit	Value
Technology	-	0.18-μm CMOS
Number of bits	-	10
Sample rate	MS/s	120
Supply voltage (Analog & Digital)	V	1
Differential output signal	V	0.5
Load (R_L)	Ω	200
|INL| [*Mean, Sta Div*]	LSB	[0.134, 0.049]
|DNL| [*Mean, Sta Div*]	LSB	[0.178, 0.081]
SFDR @ Desired signal band	dB	> 63
Glitch energy	pV·s	0.4
Power consumption	mW	2.5‡

‡: Power Breakdown: 1.3 mW (Analog), 1.2 mW (Digital).

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