Design of a 1-V 10-bit 120-MS/s Current-Steering DAC with Transient-Improved Technique

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Abstract – **Implemented in a 0.18-μm CMOS process, a 10-bit 120-MS/s current-steering digital-to-analog converter (DAC), which is designed using a top-down design methodology, focused on WLAN applications consumes only 2.5 mW from a single 1-V supply. A charge-removal-replacement (CRR) technique is proposed to realize the low-voltage low-power DAC with minimizing transition time in current switching. The simulated monotonic performances achieve a mean value of |INL| of 0.134 LSB and |DNL| of 0.178 LSB, respectively. The averaged SFDR obtains 67.23/62.45 dB with/without the CRR technique.**

I. INTRODUCTION

The demand for high performance digital-to-analog converters (DACs) has significantly increased for the fast development of advanced telecommunication systems, e.g., wireless local area networks (WLANs). In view of that, most of data converters are desired to be fully integrated into a CMOS System-On-a-Chip (SoC) wireless transceiver with including RF transceiver, digital physical layer (PHY), corresponding media access controller (MAC) and all other analog baseband building blocks [1]. To avoid any supply-voltage constraints for the technology scaling, low-voltage building blocks with low-power consumption will be highly required.

In practice, current-steering DAC is preferred for wireless communications due to its high sample rate, high capability of driving resistive loads and relatively low-power consumptions. The current cells with cascoded topologies [Fig. 1] are satisfactory for static and dynamic output-impedance requirements [2]-[3]. Alternatively, the cascoded-switch topology in Fig. 1(b) [4] presents as advantages of additional digital signal feedthrough isolation and output influence reduction through the insertion of two cascoded transistors (M_{cas+} and M_{cas-}). However, asymmetry in rising-falling transitions and long settling time will degrade the dynamic performance. Especially in the implementation of high speed and high resolution DAC, current source with small unit current will intensify such problems significantly. This paper proposes a *charge-removal-replacement* (CRR) technique that improves those transient requirements. For demonstrated purposes, a 1-V 10-bit 120-MS/s DAC was designed and simulated achieving high reduction in current switching transient and also enhancing the dynamic performances dramatically.

After this introduction, the DAC architecture and the specification are described in section II. In section III, the constraint parameters will be identified in behavior-level consideration. Afterwards, the proposed CRR technique and all other building blocks will be described in section IV. In section V, simulation results will be presented. Finally, the conclusions will be summarized in section VI.

II. DAC ARCHITECTURE

In the conventional current-steering DAC, the segmented architecture improves differential non-linearity (DNL) and glitch performance by using more unary decodes. However, increasing the use of unary decoding occupies large chip area, increases power, digital noise, time skews and design complexity. In the design of a 10-bit DAC with an equal structure and a fully binary decode [5] is more attractive to achieve low power, high accuracy, linearity and speed, as well as size compaction. The simplified floor plan of the DAC is depicted in Fig. 2, it consists of a set of digital input buffer, a clock driver, a biasing circuit, a switch & latch array (SWATCH), and a current-source array (CSA). Utilizing a transimpedance output stage [6], which has a lower input impedance node, improves static and dynamic linearity concurrently. Nevertheless, this current-to-voltage buffer is normally required to drive a smaller feedback resistor, imposing large power dissipation. For power saving, the designed DAC drives a resistive load (R_L) directly [7] instead of using the transimpedance output buffer.

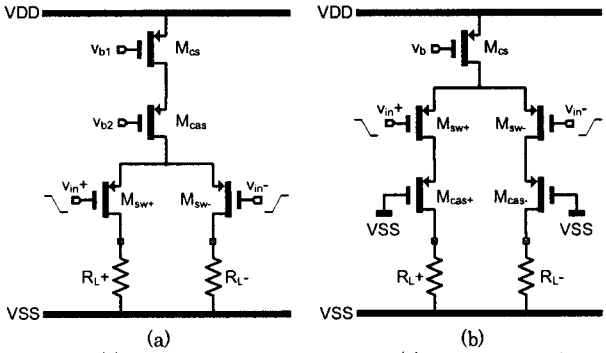


Fig. 1 (a) Cascoded-current-source and (b) cascoded-switch topology.

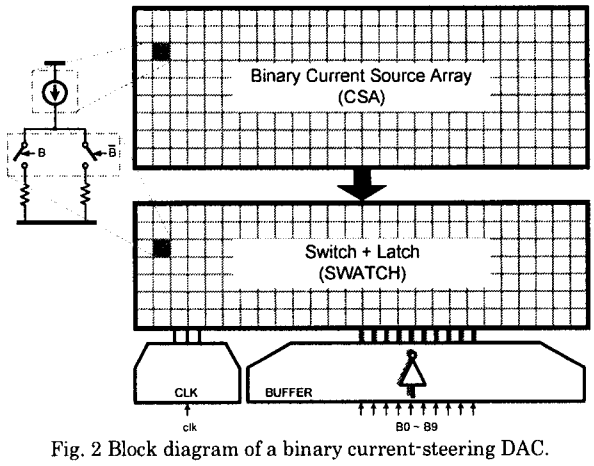


Fig. 2 Block diagram of a binary current-steering DAC.

The specification list for the current-steering DAC is given in Table 1. The specifications are divided into three parts: *environmental*, *static* as integral non-linearity (INL), DNL and

Table 1 General specification list for the current-steering DAC.

	Specification	Unit	Value
Environmental	Power supply	V	1
	Input BW	MHz	10
	Decode	-	binary
	Load (R_L)	Ω	200
	Output current	mA	1.25
Static	Number of bits	Bit	10
	INL	LSB	≤0.5
	INL Yield	%	99.7
	DNL	LSB	≤0.5
	DNL Yield	%	99.7
Dynamic	Sampling frequency	S/s	120
	SFDR	dB	≥60
	Settling time	ns	≤8

parameter yield, as well as *dynamic,* namely glitch energy, settling time, and spurious-free dynamic range (SFDR).

III. BEHAVIOR-LEVEL DESIGN

DAC performances are specified through static and dynamic performance. Afterwards, the implications and the dependent parameters of those constraints in the circuit-to-transistor level procedure of the DAC will be presented.

Statistic Performance – The dependencies of the DAC static performances on (a) *finite output resistance* of the current sources, (b) *systematic* and (c) *random mismatch errors.* Switching different resistances (i.e. output resistance of current source) to the output node introduces variations in the equivalent load resistance and hence produces input dependent non-linearity in the output voltage. The constraint in the output resistance can be expressed as:

$$|\mathrm{INL}| = \left| \frac{2^{2B}}{6} \frac{R_L/R_{out,u}}{2^B \cdot R_L/R_{out,u} - 1} \right| \qquad (1)$$

where B is number of bit, R_L is the load resistance, and $R_{out,u}$ is the output resistance of unit current source. Systematic errors caused by process, temperature, and gradient effect, which can be cancelled by proper layout techniques. In the case of random mismatch errors, the tolerable relative standard deviation of unit current matching (σ_u/I_u) can be calculated or simulated in the behavior-level Monte-Carlo simulation by using a Matlab program, the plot shows in Fig. 2. To achieve a yield of 99.7% (|DNL| and |INL| < 0.5 LSB), σ_u/I_u is chosen 0.2%.

Dynamic Performance – The dependencies of the DAC dynamic performances on (a) *output impedance* of the current sources and (b) *clock feedthrough* (CFT). The output impedance is one of factors to affect SFDR performance of current-steering DAC, the constraint in the output impedance can be estimated as:

$$\mathrm{SFDR} \approx -40 \cdot \log_{10}\left(R_L/|Z_{out,u}|\right) - 12(B-2) \qquad (2)$$

where $Z_{out,u}$ is the output impedance of unit current source. The limited output impedance also affects the settling time, and the CFT to the output is an important contribution to glitch energy. In practice, they can be optimized in the transistor level design.

IV. CIRCUIT-TO-TRANSISTOR LEVEL DESIGN

A 1-V 10-bit 120-MS/s fully binary-weighted current-steering DAC with the CRR technique is designed for WLAN applications. The complete floor plan is shown in Fig. 4.

- **Current Source Array (CSA)**

The matching of CSA is critically determined by the area of the unit current source. In the behavioral-level simulation, a maximum σ_u/I_u of a unit-current source is 0.2% for correct INL and DNL yields. In fact, σ_u/I_u of a binary-weighed DAC is normally determined from the DNL yield. The minimum area $(W \cdot L)_{min}$ of the unit current source is estimated by [8],

$$(W \cdot L)_{min} = \frac{1}{2 \cdot (\sigma_u / I_u)^2} \left[A_\beta^2 + \frac{4 A_{VT}^2}{(V_{GS} - V_T)^2} \right] \qquad (3)$$

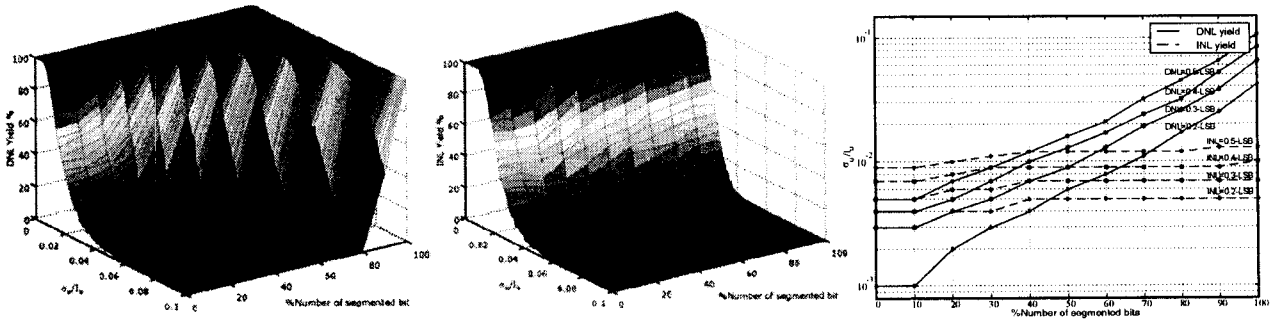
where A_β and A_{VT} are the matching parameters, and $(V_{GS}-V_T)$ is the overdrive voltage of the current source transistor.

- **Switch + Latch (SWATCH)**

The switch array of the DAC is constructed by cascoded switches to enhance the output impedance of the current sources. Normally, the length of the input (L_{sw}) and cascoded (L_{cas}) switches is chosen at minimum length to further reduce the digital feedthrough. Beside the effect of finite output impedance, the dynamic performance of a current-steering DAC is mainly limited by the imperfect synchronization of the control signals and the drain-voltage variation of the current source. For lowering the glitch errors as the current is switched to the desired output, it is essential that the driving signals exhibit a lower crossing point. The rise/fall-time-based latch [9] has been exploited for its high-speed capability [Fig. 4], and NMOS positive feedback loop exhibits a faster fall time of the latch. Moreover, an additional feedback using small inverters (*I1* and *I2*) reduces the CFT.

- **Charge-Removal-Replacement (CRR) technique**

The main disadvantage of the conventional cascoded-switch



(a) (b) (c)

Fig. 3 Behavior-Level Monte-Carlo simulations of (a) DNL yield (b) INL yield, and (c) σ_u/I_u requirement to achieve yield of 99.7% vs. different number of segmented bit. [In fully binary-weighted DAC, %Number of segmented bits=0]

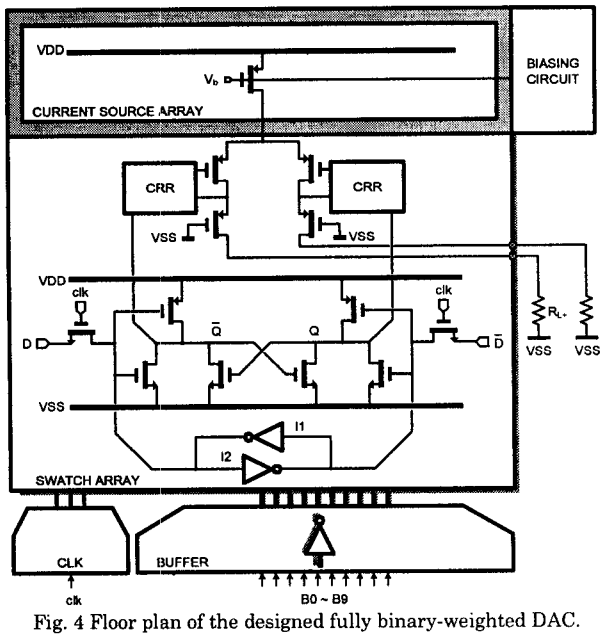


Fig. 4 Floor plan of the designed fully binary-weighted DAC.

current source (CSCS) topology is the settling problem, which the falling settling time is slower than that in rising, causing distortion in the output current of the DAC. The tarry falling settling time is caused by the node voltage, which below the off switch (M_{sw+}/M_{sw-})[Fig. 5], is discharged exponentially until the cascoded switch (M_{cas+}/M_{cas-}) enters in the subthreshold region. As a result, an amount of current leaks into the path even if the corresponding switch is in the off stage. Such current is given by the subthreshold expression of the drain current (I_D),

$$I_D = I_0 \exp\frac{V_{SGcas}}{\varsigma V_T} \qquad (4)$$

where ς>1 is a nonideality factor and $V_T = kT/q$. Moreover, with parasitic capacitance present in the source terminal of cascoded-transistor M_{cas+}/M_{cas-}, the transition will be further extended.

The CRR technique is depicted in Fig. 5(a), where a capacitor (C_{CRR}) driven by an inverter is inserted between the gate and drain terminals of the switched transistor. When the desired switch is turning off, the inverter generates an inverted control signal to draw out the positive charge (Δq^+) from the inversion layer and the ubiquitous parasitic capacitance at node X, such that any lengthy discharge procedure can be eliminated.

To avoid current sources from being turned off simultaneously, digital control signals with lower crossing point apply to the switch inputs [Fig. 5(b)]. If the switching control signals directly cross-couple to the capacitor C_{CRR}, the charge Δq^+ will draw continuously when the path is turned off. Thus, the inverter is necessary required to generate a delayed control signal to balance the falling and rising transitions.

Timing Benefits – Two advantageous features are summarized below:

(a) Balanced Speed and Advanced Transition: The CRR technique improves the rising transition by replacing some positive charge, given that the node voltage v_X is faster settling to its steady-state value while the current path is turning on. On the other hand, when the current path is desirable turned off, the CRR technique removes the residual charge and prompts the

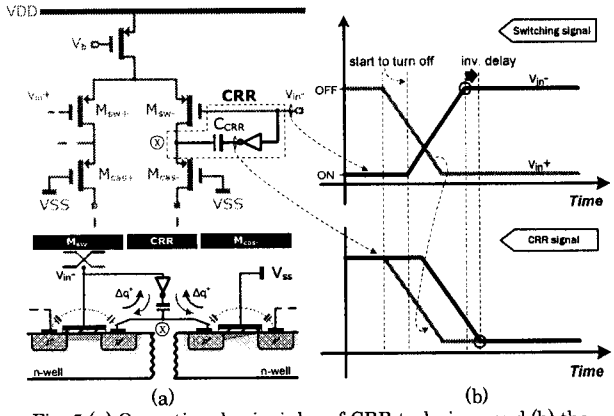


Fig. 5 (a) Operational principles of CRR technique and (b) the corresponding control signals.

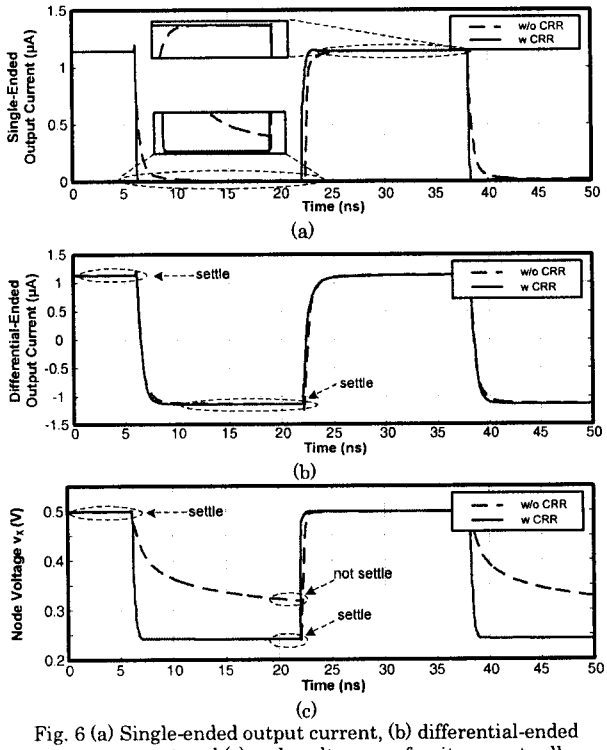
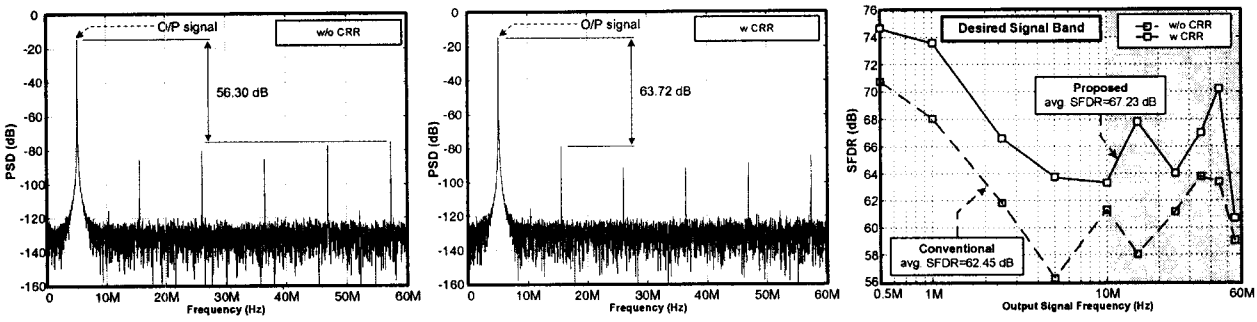


Fig. 6 (a) Single-ended output current, (b) differential-ended output current and (c) node voltage v_X of unit current cell.

node voltage v_X to steady state (i.e., v_X is leaded to reduce). Therefore, the cascoded switches no longer suffers from the critical exponential discharge problem, establishing balanced falling and rising speeds. As illustrated in Fig. 6(a), the falling transition of a single-ended output current is enhanced in terms of speed to achieve more balanced rising-falling characteristic. Even though a differential-ended output signal [Fig. 6(b)] can suppress even-harmonic distortion in the conventional CSCS structures, the transient nonlinear problem still exists, which can be solved by the CRR technique presented.

(b) Recovered Synchronization for Each Current Source: In the current-steering DAC, the digital control input signals switch the correspondent current paths on/off. Delay differences among active current paths create an input-data-dependent non-linearity



(a) (b) (c)

Fig. 7 Simulated output spectrum at 5 MHz, 120 MS/s (a) without and (b) with CRR technique. (c) SFDR vs. output signal frequency.

Table 2 Summary of DAC simulated performance.

Specification	Unit	Value
Technology	-	0.18-μm CMOS
Number of bits	-	10
Sample rate	MS/s	120
Supply voltage (Analog & Digital)	V	1
Differential output signal	V	0.5
Load (R_l)	Ω	200
|INL| [*Mean, Sta Div*]	LSB	[0.134, 0.049]
|DNL| [*Mean, Sta Div*]	LSB	[0.178, 0.081]
SFDR @ Desired signal band	dB	> 63
Glitch energy	pV·s	0.4
Power consumption	mW	2.5‡

‡: Power Breakdown: 1.3 mW (Analog), 1.2 mW (Digital).

and increase the susceptibility to asynchronous glitches. The conventional CSCS endures input-data-dependent delay even the clock nets are perfectly synchronized. The reason is the node voltage v_X requires a long settling time, even though the output current has already settled [Fig. 6(b) and (c)]. The node voltage v_X, thus, requires different charging time in every clock cycle, resulting in a non-constant rising delay for switching on the current path. The CRR technique is embedded into the swatch array [Fig. 4], and the PMOS capacitor is utilized instead of capacitor C_{CRR} for area saving. In this way, not only the charge injection is reduced (similar to a dummy switch), but also removed/replaced the positive charge while improving the transient characteristic and dynamic performances.

In the designed DAC, the full-scale current is 1.25 mA and the resistive load R_L is 200 Ω. The resulted differential peak-to-peak output voltage is 0.5 V.

V. SIMULATION RESULTS

A 1-V 10-bit DAC simulated using 0.18-μm CMOS technology was designed to demonstrate the above technique. To evaluate the static linearity performance of the DAC, 300-time INL and DNL Monte-Carlo simulations are applied. The simulations show that the |INL| and |DNL| exhibit a [*mean, standard deviation*] of [0.134, 0.049] and [0.178, 0.081] LSB, respectively. As mentioned, the CRR technique can improve the switching behavior of the current cells. In order to compare the dynamic performance between the conventional and the proposed technique, the output spectrums are presented in Fig. 7 (a) and (b), respectively. With the new technique, the averaged SFDR is improved by 4.78 dB within the Nyquist band [Fig. 7(c)]. A summary of the simulation performances is listed in Table 2.

VI. CONCLUSION

A 10-bit 120-MS/s current-steering DAC has been designed using a systematic top-down design methodology (with architecture-level, behavior-level and circuit-to-transistor level design). A *charge-removal-replacement* (CRR) technique for improving the transient performances of current-steering DACs are presented and adopted in a 1-V fully binary-weighted DAC, the technique removes (replaces) the node charge when the desired current path is turned off (on). The discharging (charging) time is reduced leading to a higher speed in D/A conversion. Compared with the conventional cascoded-switch current source (CSCS) topology, the switching transition, asymmetry rising-falling settling and synchronization problems are minimized with negligible power and chip area overheads. In average, 4.78-dB improvement in SFDR is achieved in the Nyquist band.

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REFERENCES

[1] S. Mehta, *et al.*, "An 802.11g WLAN SoC," in *IEEE ISSCC, Digest of Technical Papers*, pp. 94-96, Feb. 2005.

[2] B. Razavi, *Principles of Data Conversion System Design*. IEEE Press, 1995.

[3] A. V. D. Bosch, *et al.*, "SFDR-Bandwidth Limitations for High Speed High Resolution Current Steering CMOS D/A Converters," in *Proc. of ICECS*, VOL. 3, pp. 1193-1196, Sept. 1999.

[4] H. Takakura, *et al.*, "A 10 bit 80MHz Glitchless CMOS D/A Converter," in *Proc. of CICC*, pp. 26.5.1-26.5.4, May 1991.

[5] J. Deveugele, *et al.*, "A 10b 250MS/s Binary-Weighted Current-Steering DAC," in *IEEE ISSCC, Digest of Technical Papers*, pp. 362-532, Feb. 2004.

[6] K. -H. Ao Ieong, *et al.*, "A Frequency Up-Conversion and Two-Step Channel Selection Embedded CMOS D/A Interface," in *Proc. of ISCAS*, pp. 392-395, May 2005.

[7] N. Ghittori, *et al.*, "A Low-Power, Low-Voltage (11mW/8.4mW, 1.2V) DAC+Filter for Multistandard (WLAN/UMTS) Transmitters," in *Proc. of VLSI Circuits*, pp. 334-337, Jun. 2005.

[8] M. J. M. Pelgrom, *et al.*, "Matching properties of MOS transistor", *IEEE JSSC*, VOL. 24, NO. 5, pp. 1433-1439, Oct. 1989.

[9] A. V. D. Bosch, *et al.*, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE JSSC*, VOL. 36, NO.3, pp. 315-324, Mar. 2001.