NOVEL TIMING-SKEW-INSENSITIVE, MULTI-PHASE CLOCK GENERATION SCHEME FOR PARALLEL DAC AND N-PATH FILTER

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ABSTRACT

This paper presents a comprehensive analysis of mismatch-insensitive clock generation techniques for two types of parallel (time-interleaved) sampled-data systems, namely D/A conversion systems and sampled-data filters. A novel class of multi-purpose, low-jitter, multi-phase clock generator scheme will be proposed. The platform has the advantages of being insensitive to timing mismatches, having a simple and highly robust architecture such that the clock generator can be generalized not only for an arbitrary number N of time-interleaved (TI) paths, but also can be applied to these two types of parallel sampled-data systems, such as time-interleaved DACs, interpolation filters and N-path filters.

KEY WORDS

Time-Interleaved, DAC, N-path, Timing-Jitter, Timing-Skew, Clock Generator.

1. INTRODUCTION

The rapid evolution of electronic instruments and data communication demands high-speed data acquisition and conversion channels as well as signal processing units, like for example, the single-chip CMOS transceiver [1], the digital oscilloscope and RGB-LCD display conversion [2]. Time-Interleaved (TI) architectures are one of the most effective ways to boost the maximum speed of the analog electronics devices in current process technology, but they suffer from periodic timing skew that produces modulation images at frequency locations of multiples of f_s/M (f_s-overall sampling rate, M-period of timing skew), which are caused by timing mismatches in different time-interleaved paths [3]. These images will severely affect, especially, the dynamic range of TI-sampled data systems in very high-speed applications. As the sampling frequency increases beyond 100MHz, the design of a low-jitter, non-overlapping clock generator becomes a critical task to ensure a satisfactory performance of such high-speed systems.

Various techniques had been reported in the literature to produce low-jitter sampling clocks. One of such techniques uses Delay Lock Loop (DLL) to compensate the timing-jitter [4], but it suffers from complex control and delay sensing circuitry, and the clock de-skew performance is also limited by the speed of the DLL. A more accurate technique comprises the utilization of precise clock edges, such as those from master clock [2-7], to reduce the timing skew. In this paper, a novel class of multi-purpose, low-jitter multi-phase non-overlapping clock generation platform will be proposed. This new platform is generalized for different applications in D/A conversion paths or more general sampled-data systems, including TI DACs, interpolating filters and N-path sampled-data filtering. It presents significant advantages due to the simple circuit architecture and the high robustness that allows its extended operation to multi-phase with a low hardware cost.

2. CLOCK EDGES REQUIREMENTS

The sampling instants of sampled-data systems are defined either at the rising or falling edges of the sampling clock, thus implying that the clock edges inaccuracy would be directly related to the timing jitter. Considering, for example, a Switched-Capacitor (SC) output multiplexer circuit from a D/A conversion path to produce a high-speed output [6], as shown in Fig. 1(a), that is a typical example of a TI sampled-data system with N paths. As it is common in SC circuits, they usually require multi-phase non-overlapping clock signals $\phi_1 \ldots \phi_N$ and $\phi_1' \ldots \phi_N'$ to control the analog switches. Thus, in order to minimize the effect of signal-dependent charge injection and clock feedthrough errors [2] in the sampling capacitors $C_1 \ldots C_N$, the switches controlled by pre-phases $\phi_{1p} \ldots \phi_{Np}$ will be opened slightly earlier than the post-phases $\phi_1 \ldots \phi_N$, which means that the falling edges of the pre-phases should appear slightly earlier than that of the post-phases as shown in Fig. 2(a). On the other hand, for certain applications with higher accuracy, the rising edges of the pre-phases could be placed also slightly earlier than that of post-phases to further suppress the charge injection errors (with small loss on the available settling time of the opamp) [8]. Inaccurate sampling

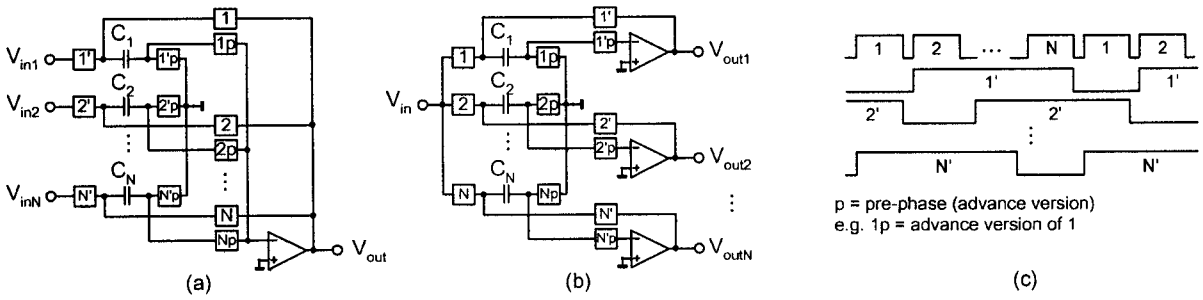

Fig. 1: SC multiplexer and sampled-and-hold circuits used in time-interleaved sampled-data systems: (a) Output multiplexer circuit; (b) Input S/H circuit; (c) Timing-diagram of both circuits
Dashed lines point out critical edges

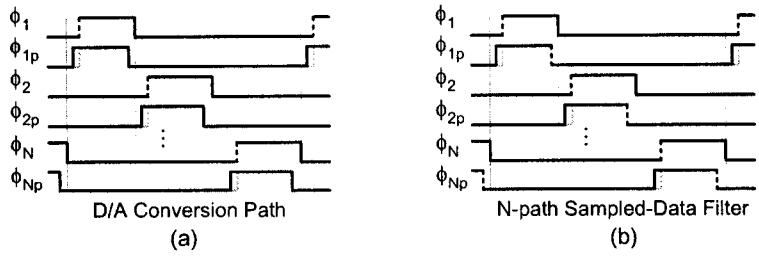

Fig. 2: Timing diagram to illustrate the critical clock edges: (a) D/A conversion & (b) N-path sampled-data filtering

clock edges produce periodic timing skew with period M=N and for the TI D/A conversion path, since the charges in the capacitors are transferred to the outputs once the switches $\phi_1 \ldots \phi_N$ are turned on, the critical edges are the **rising edges** of the **post-phases** (or both-phases if they rise together) to be controlled for avoiding timing skew in the **D/A conversion path**, as presented in Fig. 2(a) [6].

On the other hand, for **general sampled data systems** such as N-path filters, both TI S/H (Fig. 1(b)) and multiplexer are utilized for input sampling and output play-out, implying that **both the rising edges** of the **post-phases** and the **falling edges** of the **pre-phases** described previously will become critical edges. Fig. 2 summarizes the clock waveforms and critical sampling edges for these two different cases.

3. A NOVEL LOW-JITTER CLOCK GENERATION PLATFORM

The timing skew effects can be greatly reduced by using a method called "Clock Edge Reassignment", in which all the critical sampling edges are assigned by only one of the accurate master clock edges (either falling or rising, or both). This method imposes the reduction of the effect of timing skew by accurate control of the clock edge timing. Such accurate clock sampling will considerably reduce the timing skew and it allows the use (without any modifications) of traditional S/H or multiplexer circuits, as in Fig. 1.

Using the previous mentioned techniques a novel, multi-purpose platform for generation of low-jitter, multi-phase non-overlapping clock phases has been developed. This platform can be applied to TI D/A conversion systems (including interpolators) and N-path sampled-data filtering. Fig. 3 shows the block and timing diagrams of the proposed clock generator, which assigns both the rising edges of the post-phases and the falling edges of the pre-phases from the accurate master clock. Although this platform can also be applied to A/D conversion systems which require accurate falling edges of pre-phases, [9] presents a simpler implementation. Fig. 4 exhibits the clock generator platform containing the following building blocks:

A. Master-slave D-flip-flop with master output

Fig. 4(a) shows a master-slave D-flip-flop (DFF) with an additional master output that is extracted from the master latch. With such arrangement the master (M) output signal always leads the slave (Q) quadraturely.

B. Self-starting mod-N ring counter

The self-starting mod-N ring counter is designed to provide shifted negative pulses, which serve as envelopes of various multi-phase clock signals to ensure a non-overlapping operation. Fig. 4(b) shows an example of self-starting mod-4 ring counter, where dummy gates are used to balance the loading conditions of Q and M outputs.

C. Edge Decision Block (EDB)

Since the clock generator is to be used in D/A converters (or interpolators) or N-path filters, both the rising edges of the post-phases (or both phases) and the falling edges of the pre-phases become critical. These two critical edges can be controlled simultaneously by the use of Edge Decision Block (EDB as shown in Fig. 4(c)). The rising edges of both phases are determined by the falling edges of the post-DFF-clk, while the falling edges of the pre-phases are assigned by the rising edges of pre-clk. Since both the pre-clk and post-DFF-clk are delayed versions (by d_0 and d_2 respectively) of the master clock, the N-phases produced are accurate in the

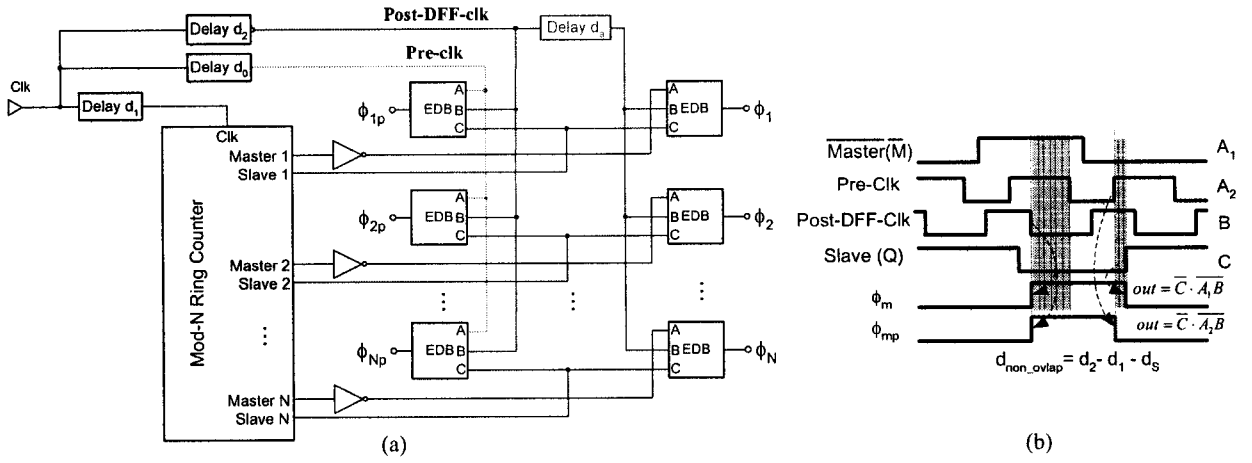

Fig. 3: (a) Block diagram & (b) Timing diagram of proposed low-jitter multi-phase clock generation platform for D/A conversion and N-path filtering.

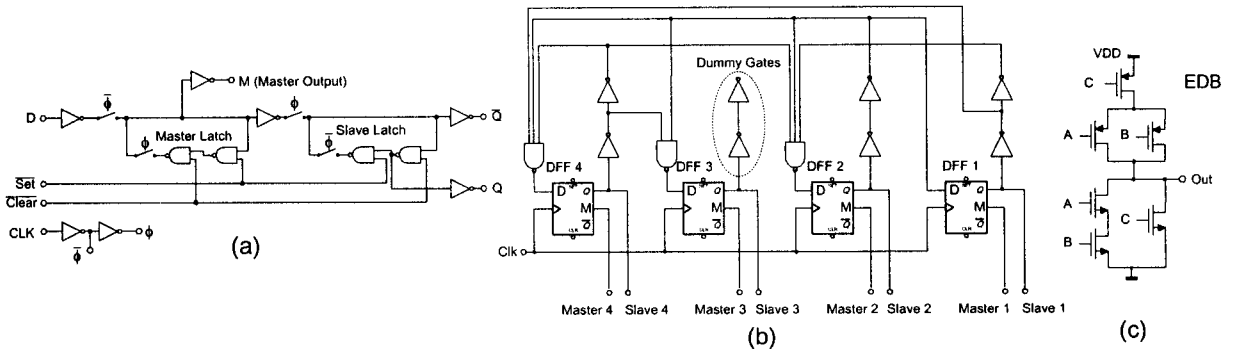

Fig. 4: Building blocks of the proposed clock generator platform:
(a) Master-slave DFF with master output; (b) Self-starting mod-4 ring counter; (c) Edge Decision Block (EDB)

rising edges of both phases and in the falling edges of the pre-phases, thus suitable in DAC applications, interpolating filters, and *N*-path sampled-data filters. The bubble on the delay d_2 indicates a logic inversion of the delay output. However such assignment is not possible as it can be verified for example in the two shaded areas of the Fig. 3b, where the pre-clk signal is equal to 1 and the slave (Q) is 0 in both areas while the output ϕ_m is dissimilar. In order to identify separately these two regions a master output M from the DFF serves as a boundary between the shaded areas. It can be shown that this clock-edge reassignment can be achieved by the following EDB logic:

$$out = \overline{C} \cdot \overline{AB} \qquad (1)$$

4. SIMULATION RESULTS

In order to verify the effectiveness of the proposed clock generation platform, a 4-phase version of the clock generators were simulated with Hspice with the master clock frequency set at 160 MHz (also the overall sampling rate).

The designed clock generators are used to drive the switches in the TI S/H or multiplexer circuits, to sample or play out a 75 MHz sinusoidal signal with the overall sampling frequency of 160 MHz. Fig. 5(a) shows the FFT output spectrum with the 4-phase version of the conventional clock generator from [10] that has no control over clock edge accuracies. The spectrum shows 3 mismatch-induced image tones appearing at frequency 5, 35, 45 MHz, respectively, and only 46.75 dB SNR is achieved, corresponding to 13 ps timing mismatches by the formula derived in [3]. Fig. 5(b) shows the corresponding spectrum with the proposed clock generator and the image tones are effectively reduced with an SNR 66.6 dB (less than 2 ps timing mismatches), corresponding to 19 dB improvement and thus demonstrating the effectiveness of the proposed techniques. Fig. 6 also shows a 100-run Monte-Carlo simulation on the timing skew performance in phase 2-4 (the timing-skew are reference to phase 1), with the rms value of timing-skew of 1.56 ps only.

5. CONCLUSIONS

A thorough and generalized analysis on multi-phase clock generation techniques to reduce timing skew effects in parallel or time-interleaved sampled-data systems has been presented. Then, a novel multi-purpose, low-jitter, multi-phase non-overlapping clock generation platform is proposed. The platform can be applied to TI D/A conversion systems as well as general sampled-data systems such as N-path filters, and is generalized to any number of path N. Simulations with

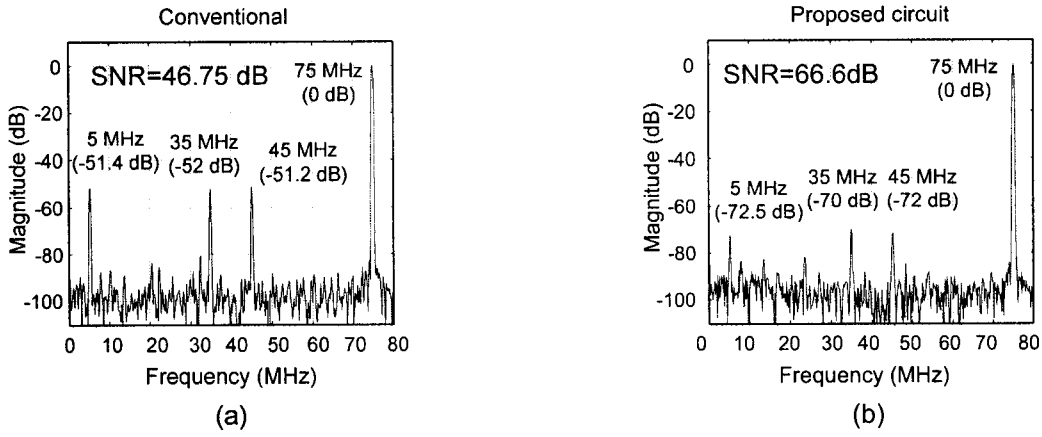

Fig. 5: Hspice FFT simulation results for: (a) conventional; (b) proposed clock generator.

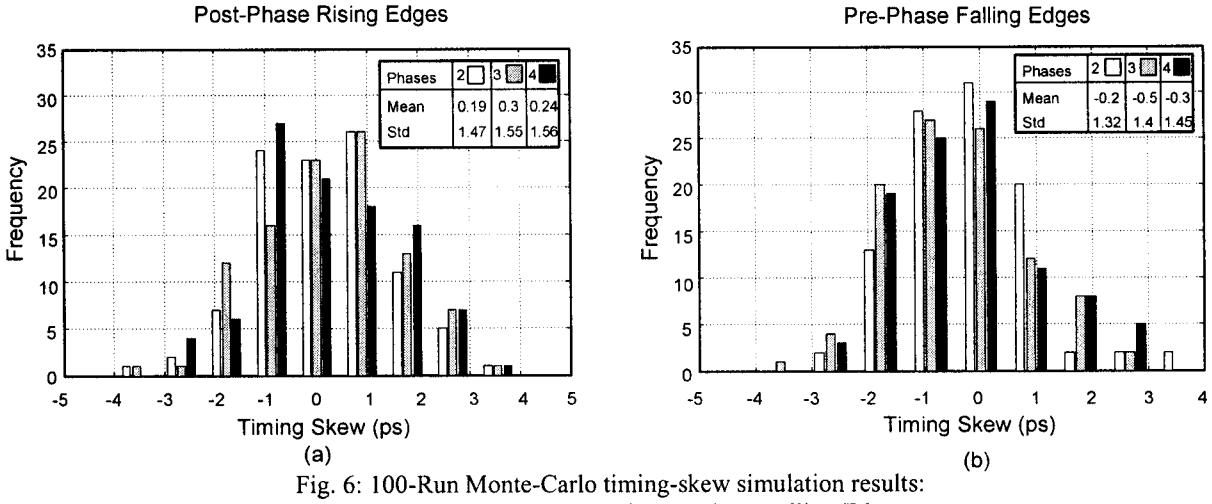

Fig. 6: 100-Run Monte-Carlo timing-skew simulation results:
(a) Post-Phase Rising Edges; (b) Pre-Phase Falling Edges

Hspice are performed to verify the effectiveness of the proposed clock generation techniques. Hspice simulation results shows 17 dB improvement in SNR compared with the conventional clock generator as verified by the FFT analysis of the simulated results.

6. ACKNOWLEDGEMENT

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