A Novel Architecture of Comparator-Mismatch-Free Multi-bit Pipeline ADC

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***Abstract*—This paper presents a novel architecture of inherent monotonic, multi-bit pipeline ADC without resorting from sample-and-hold and calibration technique. A breakthrough of its high linearity is realized by employing SAR instead of flash ADCs on top of the digital error correction scheme. Additional sampling branch of MDAC stage is exploited to deliver a half-period delay for the time-lag feature of SAR conversion. The proposed architecture does not sacrifice the conversion speed and its efficiency is validated through the macro model of a 10-bit pipeline ADC using 3.5-bit per stage.**

I. INTRODUCTION

The rapid evolution in wireless communications and electronics equipments like HDTV flat panel displayers has resulted in the demand of high-definition and power-efficient analog-to-digital converter (ADC). Pipeline ADC, primarily, is a favor choice for such applications in leveraging speed, resolution and power [1]. The impairments in circuit implementation such as capacitor mismatch [3] and OpAmp offset [4] can be minimized through circuit solutions and calibration algorithm [2]. Besides, the power optimization of pipeline ADC based on various resolution per stage also addressed throughout the years [5, 6]. They revealed that multi-bit stage performs better than single-bit one in term of power and area. Yet, the sub-ADC (flash topology) of multi-bit stage suffers from unavoidable comparator mismatch. The resulting pitfall is a non-linear progressing signal, limiting the linearity of the entire ADC. Till now, there is no on-chip analog circuitry solution proposed eliminating such comparator mismatch in multi-bit architecture.

In this paper, a novel multi-bit pipeline ADC is proposed to avoid inherently comparator mismatch. The advantage of using multi-bit per stage architecture in power criteria is addressed in Section II. The circuit implementation and simulation results of a 10-bit pipeline ADC with 3.5-bit per stage are described in Section III & IV, respectively. The conclusions are drawn in Section V.

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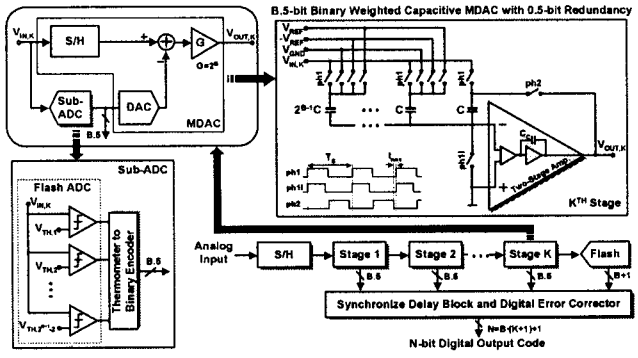

Fig. 1 Circuit implementation of conventional pipeline ADC.

II. DESIGN OF POWER EFFICIENT PIPELINE ADC

In conventional switched capacitor pipeline ADC, flash ADC is employed as the sub-ADC to assist the multiplying digital-to-analog converter (MDAC) for instantaneous digitalization, as shown in Fig. 1. According to the digital output codes of the sub-ADC, each sampling capacitor requires either $-V_{REF}$, V_{GND} or $+V_{REF}$ value to control the current stage output signal within the next stage input swing, so as to accomplish the stage-to-stage pipelining digitization. By employing digital error correction scheme, the redundancy bit at each stage leave margin for the offset from its sub-ADC and MDAC. Thus, it avoids signal overflow during stage-to-stage progression which results in missing code.

The choice of effective bit per stage determines the number of MDACs required, their specifications, and thus has a significant impact on the total power consumption. For a two-stage amplifier, the total current at the second stage that accommodates sufficient slew-rate (SR) with a capacitive load C_L can be express as,

$$I_{SR} = SR \cdot [C_L + C_{FB} \cdot (1-\beta)] \quad (1)$$

where the feedback capacitor C_{FB} equals the unit capacitor C and the feedback factor $\beta=2^{-B}$ (Fig. 1). The sampling capacitors of the next MDAC (B.5-bit is assumed) become

the load of the current stage: $C_L = 2^B C$. In practice, non-linear slewing of a full-scale voltage (V_{FS}) occupies one-third of the settling time, yielding,

$$SR = \frac{6V_{FS}}{T_S \cdot F_M} \tag{2}$$

where T_S is the sampling period and F_M is the margin factor to encounter the process and temperature variation. The remaining two-third of the settling time leaving for linear settling influenced by the gain-bandwidth product (GBW). For a two-stage amplifier with compensation capacitor C_C, the essential tail current of the first stage differential pair to provide adequate GBW can be derived as:

$$I_{GBW} = \frac{(2\pi \cdot C_C \cdot GBW)^2}{2K_p \cdot (W/L)} \tag{3}$$

where K_P, W and L is the transconductance parameter, width and length of the input differential pair, respectively. In order to guarantee the precision of MDAC stage, the necessary GBW to maintain the settling error smaller than ε can be calculated as:

$$GBW = \frac{-3\ln\varepsilon}{2\pi \cdot \beta \cdot T_S \cdot F_M} \tag{4}$$

Based on (1-4), the current consumption of a MDAC stage can be expressed as:

$$I_{MDAC} = I_{SR} + I_{GBW} = \frac{1}{\beta \cdot T_S \cdot F_M} \cdot \left[6V_{FS} \cdot C \cdot \left(1 - \beta - \beta^2\right) + \frac{(C_C \cdot \ln\varepsilon)^2}{2K_p \cdot \beta \cdot T_S \cdot F_M \cdot (W/L)} \right] \tag{5}$$

According to (5), the total current consumption of an N-bit ADC consists of only 3.5-bit or 1.5-bit stages is contoured in Fig. 2. It illustrates 3.5-bit stages can achieve higher resolution than 1.5-bit stages under the same conversion frequency and current consumption, due to the accuracy relaxation to the back-end stages. Furthermore, multi-bit stages configuration allows aggressive scaling of capacitors in the pipelining stages, and thus the power consumption can be further optimized.

The comparator mismatch of the sub-ADC can be corrected through digital error corrector for 1.5-bit stages while it is not the case in multi-bit stages. Although digital error corrector can facilitate the progressing signal within the conversion range of the next stage, the linearity degradation cannot be avoided as 1.5-bit stages do. As a result, the inherent constraint of flash ADCs gives an upper limit for the stage resolution, in order to assure the pipeline ADC meets the specification.

III. Circuit Implementation of the Proposed ADC

The proposed pipeline ADC employs successive approximation register (SAR) ADC as the sub-ADC instead of flash. The most power consuming S/H stage can be eliminated attributable to the sample/track-and-hold feature of SAR. Since only one comparator is involved in a SAR

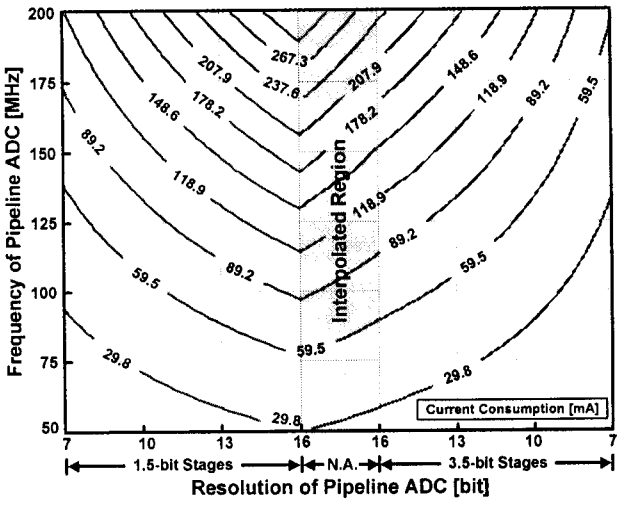

Fig. 2 Current consumption contour of a 1.5-bit and 3.5-bit per stage pipeline.

ADC, the comparator mismatch simply imposes a constant threshold voltage shifting. Applying digital error correction scheme, such threshold shifting of B.5-bit stages can be corrected as long as they are within the correction range $V_{REF}/2^{B+1}$. In spite of the inherent low conversion frequency of SAR ADC, it is suitable to assist pipeline ADC which resolution at each stage is respectively low (usually 2-4 bits). Therefore, a half sampling period of the entire ADC is adequate for the comparison iteration of such low resolution SAR. Comparing with flash, SAR ADC occupies an extra half period latency at each stage for digitalization. An additional sampling branch is used to synchronize the stage's input with the SAR ADC's output, thus, avoiding non-idealities beside comparator mismatch come from other analog delay block. The operation of a 10-bit pipeline ADC with three 3.5-bit stages followed by a 4-bit SAR ADC [Fig. 3(a)] is presented below.

A. *Last stage SAR ADC*

The two critical elements in SAR ADC are DAC and comparator. Since SAR requires a held signal for comparison iteration capacitive DAC is a favor choice for its track and hold attribute. Capacitive DAC employs the principle of charge conservation to generate an input related analog voltage V_X for comparison. For a 4-bit SAR ADC, its capacitive DAC consists of four binary weighted capacitors together with one least significant bit (LSB) capacitor as shown in Fig. 3(c).

During the sampling phase ph1, the capacitor array traps the potential difference between the input signal and $-V_{REF}$. The first iteration is ready after the most significant bit (MSB) capacitor connects to V_{FS} while all others connect to V_{GND}, driving $V_Y = -V_{IN} - V_{REF} + V_{FS}/2$. If the input signal is larger than V_{GND}, the comparator output will be logic "1" revealing V_Y is greater than the comparator reference voltage V_{GND}. The comparator output of the first iteration is stored in a shift

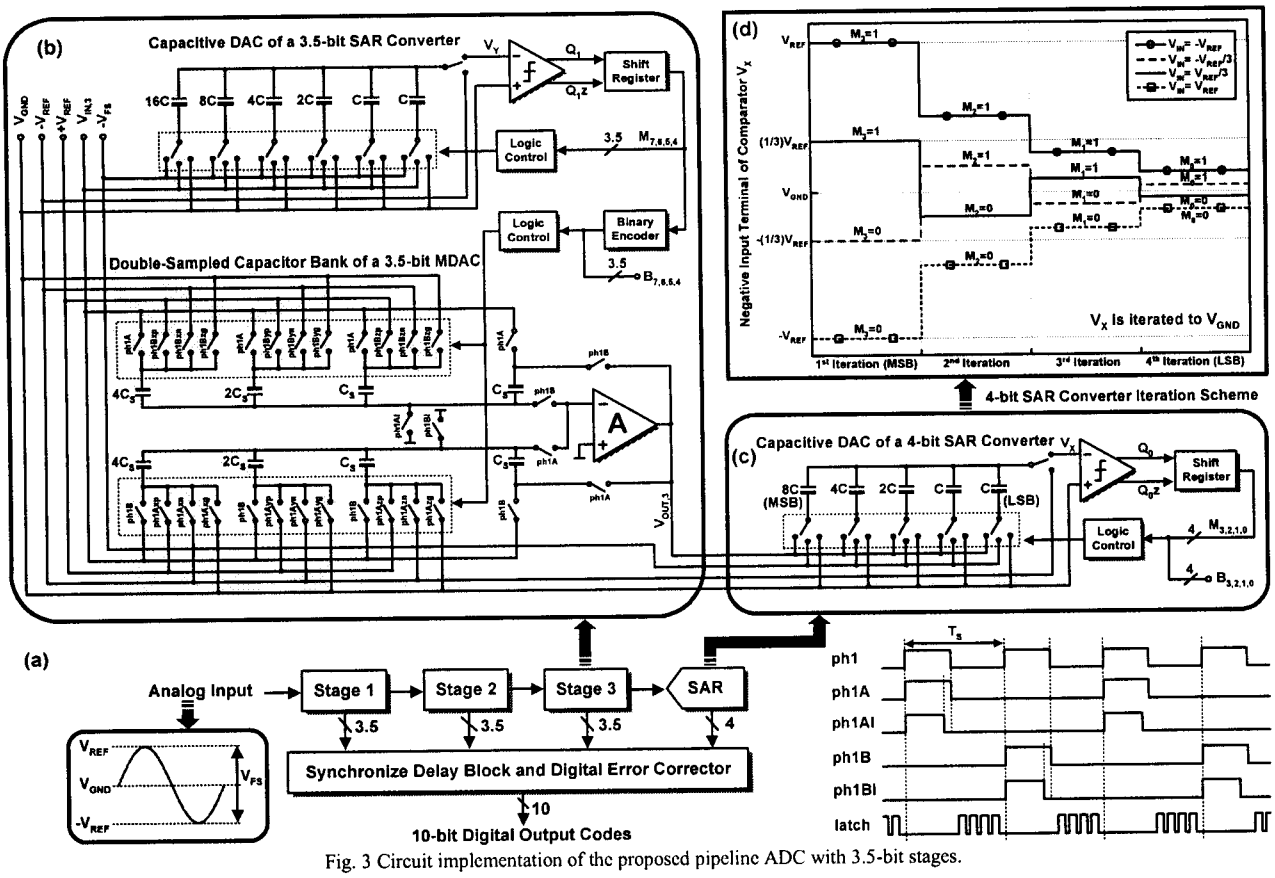

Fig. 3 Circuit implementation of the proposed pipeline ADC with 3.5-bit stages.

register and the control logic governs the MSB-1 capacitor either connects to V_{FS} or V_{GND} regarding to the previous output code. This route continues until all binary codes are determined. The operation of a 4-bit SAR ADC is demonstrated in Fig. 3(d).

B. Sub-ADC

SAR ADCs basically implement a binary searching algorithm. Thus, the realization of 0.5-bit redundancy cannot be directly achieved by the typical SAR ADC mentioned in Section III-A. The circuit implementation of a 3.5-bit SAR ADC is presented in Fig. 3(b). It illustrates the capacitive DAC of SAR exhibits a load of the previous stage. Nevertheless, the unit capacitance of the SAR can be minimized and aggressive scaling down in the subsequent stages due to its low resolution (2-4 bits) and superior capacitor matching.

The operation of a B.5-bit SAR still follows the principle of searching scheme while the capacitor array and the logic control are modified. The first iteration is completed by weighing V_{GND} against $V_X=-V_{IN}-V_{REF}+(17/32)V_{FS}$. The searching algorithm of a 3.5-bit SAR is revealed in the A/D transfer curve as shown in Fig. 4. A binary encoder is desired after the sub-ADC, owing to the existence of the redundancy bit.

C. MDAC

In order to synchronize the binary codes from the sub-ADC, double sampling technique is employed in the MDAC

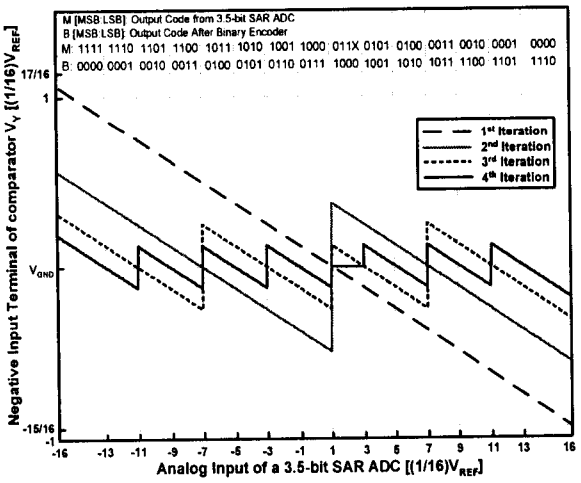

Fig. 4 Iteration searching algorithm of a 3.5-bit SAR ADC.

implementing an analog delay, as presented in Fig. 3(b). During ph1A, the analog input is sampled by the capacitive arrays of MDAC [upper branch in Fig. 3(b)] and SAR. The sub-ADC performs comparison route in ph2 and provide 3.5-bit digital codes at the end of ph2. During ph1B, the MDAC executes multiply and substrate functions to the analog input according to the digital codes from the SAR ADC. While the MDAC is amplifying in ph1B, the next digitalization begins and a new analog signal from the previous stage is sampled by another sampling branch [lower branch in Fig. 3(b)] of the current stage. The main drawback of this approach is the capacitor mismatch which leads to gain error among the adjacent samples. Notwithstanding, the specification can be met by proper selection of the capacitor size.

IV. Simulation Results

Based on the architecture discussed in Section III, a macro-model of a 10-bit pipeline ADC with 3.5-bit per stage [Fig. 3(a)] is built in Matlab environment. Consider only comparator mismatch, performances of the proposed and traditional pipeline ADC are compared in Fig. 5. Flash ADC badly suffered from comparator mismatch which leads to non-linear stage-to-stage progression [Fig. 5(a)], and thus affects the linearity of conventional pipeline ADC [Fig. 5(b&c)]. For the proposed one, the comparator mismatch results in a constant shifted threshold voltage [Fig. 5(d)], such threshold shifting can be corrected by digital error corrector and thus turns out a highly linear output [Fig. 5(e&f)].

V. Conclusions

A novel comparator-mismatch-free multi-bit pipeline ADC is proposed by employing SAR instead of flash-type ADC. A double sampled MDAC is utilized to synchronize the time lag of the SAR converter while accommodates the same conversion frequency. Inescapable comparator mismatch becomes tolerable as long as the resultant offset is within the correction range of the digital error corrector. The macro model demonstrated the highly linear stage progression and the well-perform pipeline ADC achieved by the proposed architecture.

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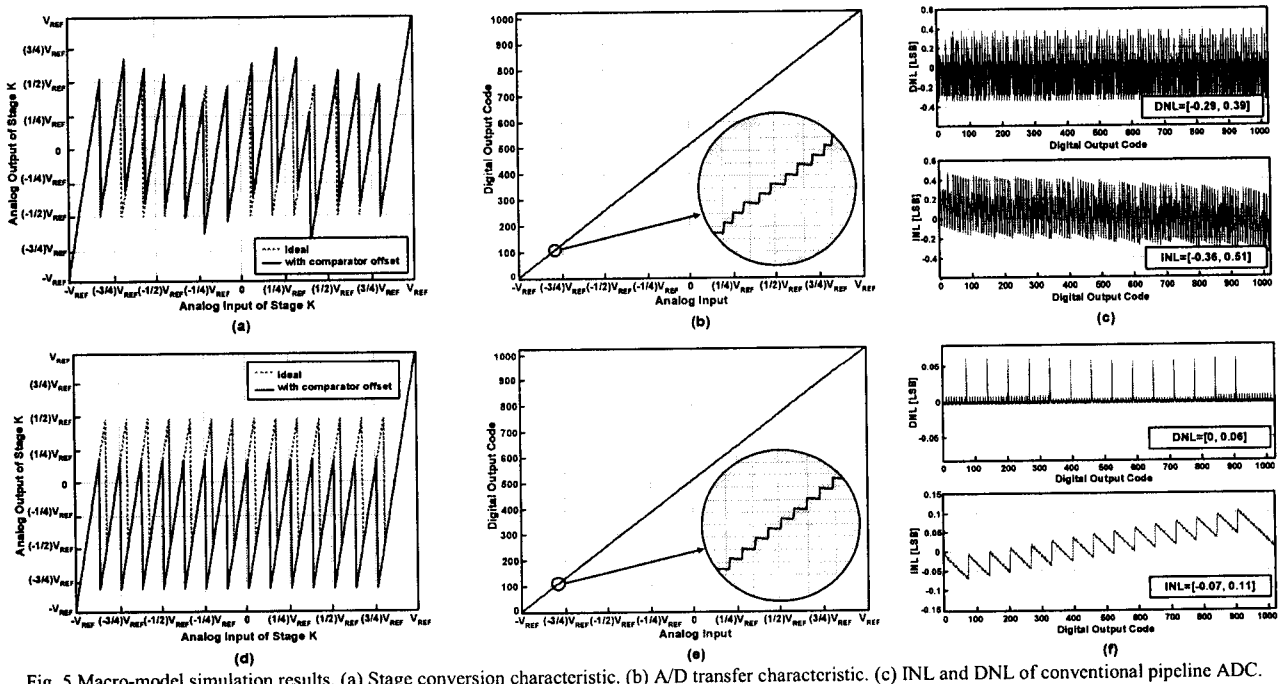

Fig. 5 Macro-model simulation results. (a) Stage conversion characteristic. (b) A/D transfer characteristic. (c) INL and DNL of conventional pipeline ADC. (d-f) The same as (a-c) in the proposed pipeline ADC.