A NOVEL N-TH ORDER IIR SWITCHED-CAPACITOR DECIMATOR BUILDING BLOCK WITH OPTIMUM IMPLEMENTATION

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Abstract

A novel N-th order IIR Switched-Capacitor (SC) decimator building block with optimum implementation has been developed for realizing arbitrary baseband and anti-aliasing amplitude responses using a minimum number of switching waveforms and employing operational amplifiers with relaxed speed requirements. Alternative topologies can be adopted depending on the acceptable capacitance spread and total capacitor area in the circuit as well as the performance under non-ideal characteristics of the amplifiers. Practical designs of a 3rd. order and a 4th. order IIR SC decimator building blocks with different factors of sampling rate reduction are presented for illustration purposes.

1. INTRODUCTION

Switched-Capacitor (SC) decimators are specialised multirate networks that implement, together with an appropriate filtering function, the reduction of the sampling rate from a high value MF_S to a lower value F_S. SC decimators can have Z-transfer functions with either Finite Impulse Response (FIR) or Infinite Impulse Response (IIR), depending on the specifications of the application. FIR SC decimators are more adequated for applications that require multinotch stopband approximations [1], whereas IIR SC decimators are usually employed in high selectivity applications on account of the reduced complexity of the resulting circuit [2].

In recent work we have developed 1st. and 2nd. order IIR SC decimators which, in comparison to traditional implementations, efficiently reduce the speed requirements of the operational amplifiers (OA's) as well as the capacitance spread and total capacitor area [3,4]. For high selectivity applications we have further developed an appropriate multistage design methodology whereby a number of such 1st. and 2nd. order IIR SC decimators are cascaded to meet the specified sampling rate reduction and amplitude response requirements [5]. This approach is primarily intended for achieving the desired baseband amplitude response with minimum capacitor area and power consumption. For achieving the required anti-aliasing amplitude response, however, an excessive number of switching waveforms might be needed, thus rendering the approach less attractive for IC implementation.

To overcome the above limitation, we propose in this paper a novel N-th order IIR SC decimator building block which allows the realization of arbitrary baseband and anti-aliasing amplitude responses using a minimum number of switching waveforms and employing OA's with reduced speed requirements. We describe a systematic approach to the design of the proposed building block, including the determination of the circuit Z-transfer function and the corresponding capacitance ratios, as well as the definition of the multiple switching waveforms that control the operation of the circuit in such a way that the OA's have the maximum time to settle. A simple set of design rules is presented to determine the most efficient topology that should be adopted yielding acceptable values of the capacitance spread and total capacitor area in the circuit, as well as an optimum performance under non-ideal characteristics of the OA's. For the purpose of illustration we present practical designs of a 3rd. order and a 4th. order IIR SC decimator building blocks with different factors of sampling rate reduction.

2. N-TH ORDER IIR SC DECIMATOR BUILDING BLOCK

General Architecture : The general architecture of the novel N-th order IIR SC decimator building block is presented in Fig.1. This can be divided into two major parts, namely one high selectivity recursive network primarily responsible for the implementation of the denominator polynomial function and one low selectivity polyphase network determining the numerator polynomial function. The recursive network can realize an arbitrary N-th order combination of real and complex conjugate poles determining the total number of OA's in the circuit, all of which operate at the low output sampling rate F_S. The polyphase network, on the other hand, is formed by a varying number of simple SC branches depending both on the sampling rate decimation factor M and on the complexity of the numerator polynomial function.

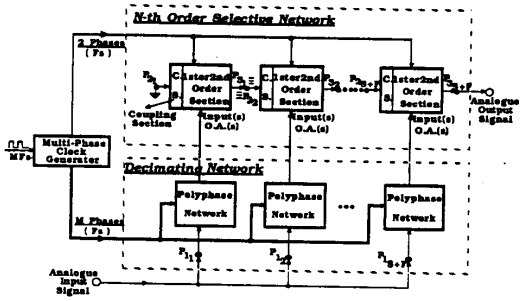

Fig.1: General N-th order IIR SC decimator building block with optimum implementation.

General Z-Transfer Function : The original Z-transfer function of the decimator can be expressed as

$$H(z)=\frac{\sum_{j=0}^{N_p} a_j \cdot z^{-j}}{\prod_{i=1}^{S}(1-2r_{p_i}\cos(\theta_{p_i})\cdot z^{-1}+r_{p_i}^2\cdot z^{-2})\cdot\prod_{i=1}^{F}(b_{0_i}-z^{-1})} \quad (1)$$

where the unit delay period corresponds to the sampling period $1/MF_S$ at the input of the decimator. The numerator polynomial function can have an arbitrary order N_P+1. The order of the denominator polynomial function is N=2S+F, where S and F represent, respectively, the number of 2nd. and 1st. order sections. A well known modification of the original Z-transfer function (1) leads to [6]

$$\bar{H}(z)=\frac{\sum_{m=0}^{N_p+2S(M-1)+F(M-1)} \bar{a}_m \cdot z^{-m}}{\prod_{i=1}^{S}(1-2r_{p_i}^{M}\cos(M\theta_{p_i})\cdot z^{-M}+r_{p_i}^{2M}\cdot z^{-2M})\cdot\prod_{i=1}^{F}(b_{0_i}^{M}-z^{-M})} \quad (2)$$

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The above modified numerator polynomial function is expressed by

$$\sum_{m=0}^{N_p+2S(M-1)+F(M-1)} \bar{a}_m z^{-m} = \sum_{i=0}^{N_z} (a_i z^{-i}) \cdot \prod_{i=1}^{S} (\sum_{k=0}^{2(M-1)} \alpha_{k_i} r_{p_i}^{k} z^{-k}) \cdot \prod_{i=1}^{F} (\sum_{l=0}^{M-1} b_{l_i} z^{-l}) \quad (3)$$

where the coefficients α_k depend both on the poles of the original Z-transfer function (1) (described by the polar coordinates r_{p_i} and θ_{p_i}) and on the decimating factor M [4].

SC Implementation : In the block diagram of Fig.1, the N-th order recursive network implements the denominator of the modified Z-transfer function (2). In general, this is formed, by the cascade of three types of basic sections, namely a 1st. order section, a 2nd. order section and a coupling section. The 1st. order section (Fig.2-a) is a classical damped integrator with an input polyphase network [2-4]. The 2nd. order section (Fig.2-b) employs a Two Integrator Loop (TIL) structure and two different sets of polyphase networks, each connected to the virtual ground of an OA [2-4]. For this section, we can adopt alternative topologies, depending on the type of damping, which can be either capacitive (E-Damping) or resistive (F-Damping) and even a combination of both, and on the accessible output, which can be from either amplifier 1 or amplifier 2. For the coupling between sections (Fig.2-c), we can also select either a Toggle Switched Inverter (TSI) branch (positive coupling) or an Open Floating Resistor (OFR) branch (negative coupling) [7]. For simplicity, we represent the branches of the input polyphase networks by polygonal symbols (Fig.2-d), where we indicate the time slot for input signal sampling, the time slot for charge transfer, and the equivalent capacitance value of the branch. Parasitic-Compensated Toggle Switched-Capacitor (PCTSC) and OFR branches have an equivalent negative capacitance value, whereas TSI branches have an equivalent positive capacitance value.

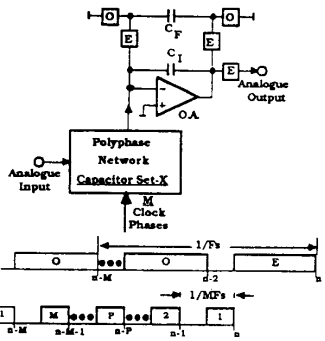

Fig.2-a: General SC structure and time frames of a first order SC decimator section.

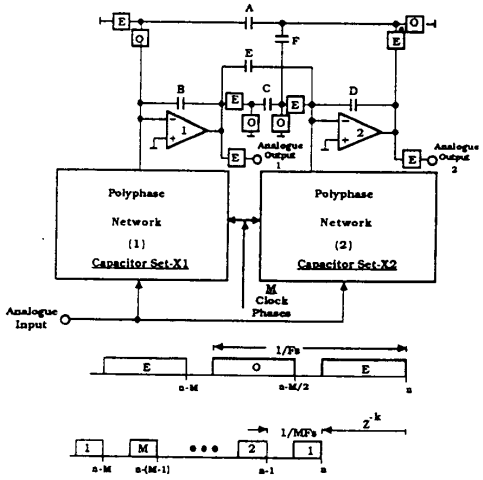

Fig.2-b: General SC structure and time frames of a second order SC decimator section.

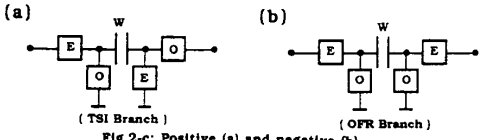

Fig.2-c: Positive (a) and negative (b) coupling sections.

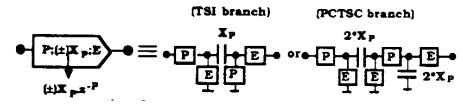

Fig.2-d: Symbolic representation of input polyphase SC branches [TSI (positive), PCTSC (negative)].

The overall Z-transfer function of the resulting circuit can be obtained from the partial Z-transfer functions associated with each section. In general, for each section we can write

$$\frac{V_{3_i}}{V_{in}}(z) = T_{31_i}(z) + T_{32_i}(z) \cdot \frac{V_{3_{i-1}}}{V_{in}}(z) \quad (4)$$

where $T_{31_i}(z)$, $T_{32_i}(z)$ are Z-transfer functions relating, respectively, the terminals 3 and 1 or 3 and 2 of section i, and $[(V_{3i-1})/(V_{in})](z)$ is related to the previous section(s) in the cascade. The expressions of $T_{31_i}(z)$ and $T_{32_i}(z)$ can be written as

$$T_{31_i}(z) = \frac{k_i}{D_i(z)} \cdot N_{31_i}(z) \quad (4\text{-a})$$

and

$$T_{32_i}(z) = W_i(z) \cdot [\frac{k_i}{D_i(z)} \cdot N_{32_i}(z)] \quad (4\text{-b})$$

where k_i, $D_i(z)$, $N_{31_i}(z)$ and $N_{32_i}(z)$ depend on the order of the section and $W_i(z)$ is the equivalent Z-transfer function of the coupling section . For 1st. order sections, the constant coefficient and denominator polynomial function are given by [3,4]

$$k_i = 1 \quad (5\text{-a})$$

$$D_i(z) = [\delta_i - \varepsilon_i z^{-M}] = [(C_{I_i} + C_{F_i}) - C_{I_i} z^{-M}] \quad (5\text{-b})$$

whereas for the numerators polynomial functions we have

$$N_{31_i}(z) = X_{j1}(z) = X_{j0} + X_{j1} z^{-1} + X_{j2} z^{-2} + \ldots + X_{jM} z^{-M} \quad (5\text{-c})$$

and

$$N_{32_i}(z) = 1 \quad (5\text{-d})$$

For 2nd. order sections the terms k_i and $D_i(z)$ become [3,4]

$$k_i = \frac{1}{(1+F_i)} \quad (6\text{-a})$$

and

$$D_i(z) = [1 + \beta_i z^{-M} + \gamma_i z^{-2M}] = \quad (6\text{-b})$$

$$= [1 + (\frac{A_i C_i - B_i D_i + B_i (D_i + F_i)(A_i E_i - B_i D_i)}{B_i (D_i + F_i)}) z^{-M} + (\frac{B_i D_i - A_i E_i}{B_i (D_i + F_i)}) z^{-2M}]$$

whereas for the numerators polynomial functions we have

$$N_{31_i}(z) = [(D_i + F_i) X_{j,l}(z)] + [A_i X_{(j-1),l}(z) - D_i X_{j,l}(z)] z^{-M} \quad (6\text{-c})$$

and

$$N_{32_i}(z) = (D_i + F_i) - D_i z^{-M} \quad (6\text{-d})$$

when the output is taken from terminal 1, and

$$N_{31_i}(z) = [B_i X_{(j+1),l}(z) - (C_i + E_i) X_{j,l}(z)] + [E_i X_{j,l}(z) - B_i X_{(j+1),l}(z)] z^{-M} \quad (6\text{-e})$$

and

$$N_{32_i}(z) = E_i z^{-M} - (C_i + E_i) \quad (6\text{-f})$$

when the output is taken from terminal 2.

The terms $X_{jl}(z)$ of the numerator polynomial functions represent the equivalent transfer functions of the input SC branches, where j is the order of the OA in the section and *l* is the order of the coefficient (example: X_{23} is the coefficient of z^{-3} in the input capacitor set of OA **2**). For the coupling sections $W_i(z)$ can be expressed by

$$W_i(z) = W_i \cdot z^{-M} \quad (7\text{-a})$$

for positive coupling, and

$$W_i(z) = -W_i \quad (7\text{-b})$$

for negative coupling.

Considering that the input terminal (P_{21}) of the first section is grounded ($T_0(z)=0$), the overall Z-transfer function of an N-th order SC decimator can be written as

$$T(z) = \frac{V_{3_{i+S+F}}}{V_{in}}(z) \cdot \frac{k_{S+F}}{D_{S+F}(z)} \cdot [N_{31_{S+F}}(z) + W_{S+F}(z) \cdot N_{32_{S+F}}(z) \cdot \frac{V_{3_{S+F-1}}}{V_{in}}(z)] \quad (8)$$

The overall Z-transfer function of the circuit is customized according to the topology of each section and which, in turn, is selected depending on the resulting capacitor area, capacitance spread and also the performance robustness under non-ideal characteristics of the amplifiers. The design equations giving the capacitance values of the circuit are determined by equating (2) to the overall Z-transfer function (8) after customization.

3. PREFERRED TOPOLOGIES FOR MINIMUM AMPLIFIER GAIN-BANDWIDTH EFFECTS

One of the fundamental aspects determining the selection of preferred circuit topologies for the proposed SC decimator building block is the performance behaviour under non-ideal characteristics of the amplifiers, namely finite DC-Gain and Bandwidth (GB). This can be evaluated by considering the relative weight of the capacitive network connected to each OA during the operating phases of the circuit [8] and which can be defined by the parameter

$$a_{ij} = \frac{\sum C_{fi} + \sum C_{fn}}{\sum C_{ii} - \sum C_{ni}} \quad (9)$$

where the C_{fi} represent all feedback capacitors from the output of OA **i** to the inverting input of OA **j**, and C_{fn} represent all feedback capacitors from the output of OA **i** to the non-inverting input of OA **j**. C_{ii} represent all capacitors connected to the inverting input of OA **j** and C_{ni} represent all capacitors connected to the non-inverting input of OA **j**. Capacitive networks such that $a_{ii}=1$ and $a_{ij}=0$ have reduced sensitivity with respect to the finite GB of the amplifiers. On the contrary, if $a_{ii}=0$ and $a_{ij}=1$, the sensitivity to the finite GB of the amplifiers is high [8].

Since the parameters a_{ij} are topology-dependent, their values can be appropriately controlled in order to achieve the desired performance robustness against the non-ideal characteristics of the amplifiers. The choice of a particular topology is therefore restricted by some constraints, the most important of which can be summarized as follows:

-**Coupling between sections** must be of type positive (7-a), to decouple OA's in the same phase and thus eliminating the terms a_{ij} that relate output of OA **i** in one section to input of OA **j** in the other.

-**Damping of 2nd. order sections** must be of type resistive (F-Damping), to decouple OA's in the loop by eliminating the term a_{12} relating output of OA **1** and input of OA **2**.

4. DESIGN EXAMPLES AND RESULTS

3rd. Order SC Lowpass Decimator With M=2 : Based on a computer aided filter synthesis tool [9] we obtained the bilinear discrete-time coefficients given in Table 1 for the Z-transfer function of a 3rd. order Tchebyshev lowpass decimator prototype filter, with cut-off frequency of 2 MHz, maximum passband ripple of 0.1dB and 15 MHz input sampling frequency ($2F_s$). According to the procedure previously described we obtained the following modified Z-transfer function for the SC decimator with M=2

$$\bar{H}(z) = \frac{\sum_{m=0}^{6} \bar{a}_m \cdot z^{-m}}{[1 - 2r_{p_1}^2 \cos(2\theta_{p_1}) z^{-2} + r_p^4 z^{-4}] \cdot [b_{0_2}^2 - z^{-2}]} \quad (10)$$

whose coefficients are given in Table 2. The SC decimator circuit for implementation is shown in Fig.3, together with the

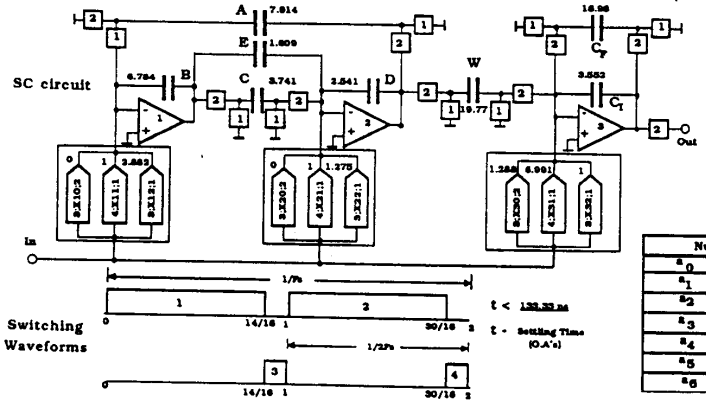

Fig.3: Third order IIR SC decimator building block (M=2, Fs=7.5 MHz)

Numerator	
k	0.0571641
$2r_{o_1}\cos(\theta_{o_1})$	2
$r_{o_1}^2$	1
b_{o_2}	1.048755
Denominator	
$2r_{p_1}\cos(\theta_{p_1})$	1.949583
$r_{p_1}^2$	0.953557

Table 1: Bilinear discrete-time coefficients of the 3rd. order SC decimator prototype filter

Numerator	
a_0	1.000566
a_1	6.492742
a_2	15.97234
a_3	20.95950
a_4	15.47355
a_5	6.009567
a_6	1.000048

Denominator	
$2r_{p_1}^2\cos(2\theta_{p_1})$	1.893758
$r_{p_1}^4$	0.909272
$b_{o_2}^2$	1.000888

Table 2: Coefficients of the 3rd. order SC decimator

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Further information can be obtained from Dr. W. Kenneth Jenkins.

capacitance values obtained after scaling for maximum dynamic range. The resulting capacitance spread is lower than 20 and the total capacitor area is less than 90 capacitor units. The nominal computer simulated passband and overall amplitude responses are illustrated in Fig.4.

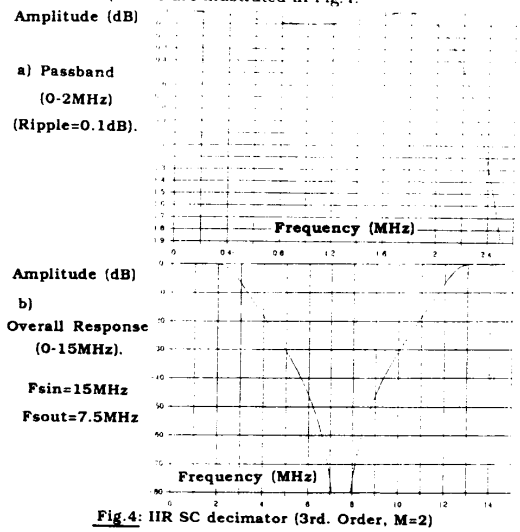

Fig.4: IIR SC decimator (3rd. Order, M=2)

4th. Order SC Lowpass Decimator With M=4 : In Fig.5 we present the SC circuit corresponding to a 4th. order lowpass decimator, with M=4. The amplitude response is defined by

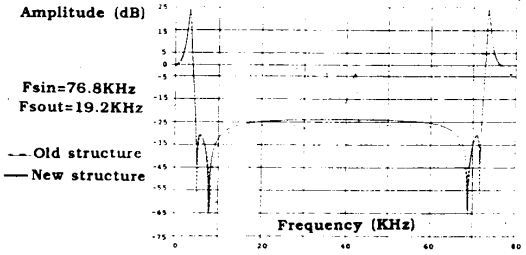

Fig.6: IIR SC decimator (4th. Order, M=4)

two complex conjugate pole pairs with pole frequencies at 3.08KHz and 3.43KHz and pole Q-factors of, respectively, 3.91 and 15.42, and two complex conjugate zero pairs placed at 5.11KHz and 8.15KHz, with infinite Q-factor. After scaling for maximum dynamic range the resulting capacitance spread and total capacitor area are, respectively, 18 and 120 capacitor units. In Fig.6 we can compare the computer simulated amplitude response of this decimator whith that of a previous design implemented by the cascade of two 2nd. order SC decimator building blocks with M=2 [5]. This clearly shows the improved anti-aliasing performance of the proposed novel building block, which is achieved with values of the capacitance spread and total capacitor area that are similar to the previous implementation, while all the OA's have to operate only at F_s (instead of two at $2F_s$ and other two at F_s as in the previous design). The total number of switching waveforms is also reduced from 8 in the previous design to 6 using the proposed novel building block.

5. CONCLUSIONS

In this paper we describe a novel N-th order IIR SC decimator building block with optimum implementation which can realize arbitrary baseband and anti-aliasing amplitude responses using a minimum number of switching waveforms and employing OA's with relaxed speed requirements. We derived the overall Z-transfer function of the circuit, and presented a set of simple rules that should be adopted for obtaining a preferred circuit topology which exhibits low sensitivity of the amplitude response against the non-ideal characteristics of the amplifiers while achieving an acceptable capacitance spread and total capacitor area for IC implementation. Two practical examples were considered to illustrate the design of the proposed novel building block as well as the resulting improvement over previous implementations.

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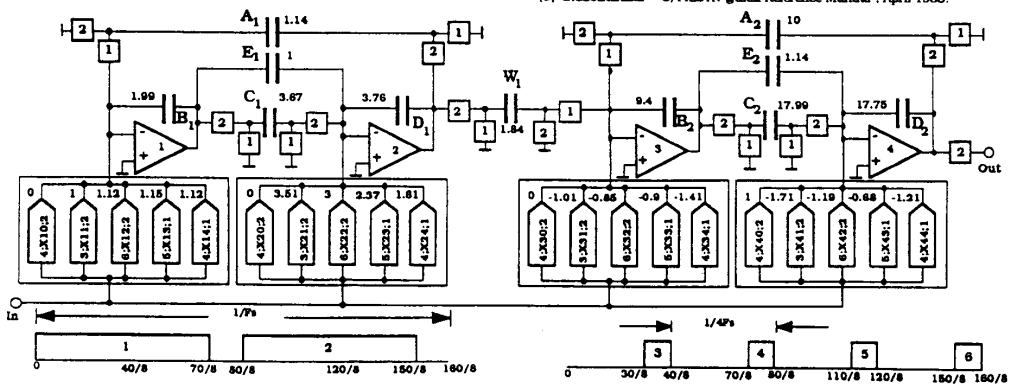

Fig.5: Fourth order IIR SC decimator building block (M=2, Fs=19.2 KHz) (SC circuit and Switching Waveforms).