A Expandable and Extendable High-order Semi-MASH Sigma-Delta Modulator

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ABSTRACT

This paper presents a high-order semi-MASH oversampling modulator which based on the application of stage feedback and using appropriate error cancellation logic. The modulator can spread the Noise Transfer Function (NTF) zero of first-order noise-shaping per stage and keep constant overload region regardless of the stage number. Furthermore, the proposed semi-MASH sub-stage will transfer to bandpass counterpart and combine with an existed optimize 2-1Lmb topology to achieve an expandable and extendable architecture. Behavioral simulations with MATLAB and SIMULINK demonstrate the performance of the proposed architecture.

KEY WORDS

Sigma Delta Modulation, MASH, Analog-to-Digital Converter

1. INTRODUCTION

Modern electronic systems used in wireline and wireless communications require both high data rate and low power consumption for portable commercial products. The analog-to-digital converter is being pushed to operate at several to tens of MHz bandwidth with 10- to 16- bit resolution and low power consumption. Traditionally, Nyquist-rate ADC using pipeline technology is well suited for MHz range applications [1]. However, when resolution and linearity increase, the design headroom becomes tighter, multi-standard is necessary and cost optimization is more relevant. Pipeline technology will become insufficient and inefficient to fulfill the specification. As small oversampling ratio is always needed to relax the analog frond-end, low OSR sigma-delta technology is another technique that can be used to implement such high-resolution wide-bandwidth ADC [2].

Cascade oversampling modulator (MASH) is one of the popular low OSR sigma-delta technologies [3-6]. Comparing it with single-stage sigma-delta technology, it doesn't suffer from the unconditional stability causing large systematic SNR loss and overload region. MASH topology comprises noise-shaping and error-cancellation techniques, which leads to a greater system relaxation since the unconditional stability doesn't occur. However, traditional MASH topology suffers from several problems, namely, stage overload, noise-shaping extension (spread NTF zero) and sensitive to weight mismatch. If the first and successive stages are second-order SDM, the effect of weight mismatch will be reduced and the NTF zero can be spread, resulting in higher SNQR [7] (Figure 1). However, more attenuation will be needed in the signal being transmitted from stage to stage to prevent the problem of overload. This will cause systematic SNQR loss and the overload point will be larger as the number of stages increases. If the successive stages are of first-order, the overload of each stage will be relaxed, but NTF zero is forced into DC and more sensitive to the weight mismatch. There exists a trade-off between the mismatch sensitive, noise-shaping extension and stage overload in traditional MASH topology.

A novel semi-MASH topology (1+1-...) will be presented in this paper that solves both stage overload and noise-shaping extension, simultaneously [8, 9]. It follows a new structural principle of introducing feedback within each MASH stage that has first-order noise-shaping. It merges two individual first-order MASH stages with feedback that will become an equivalent second-order noise-shaping with a pair of controllable NTF zeros. Furthermore, the proposed semi-MASH technique can be transfer to the bandpass counterpart. Combined with existed optimize 2-1Lmb topology [3], an high-order extendable and expandable bandpass noise-shaping can be achiebed. In section II the proposed lowpass semi-MASH architecture will study and simulation results will presente. In section III, an high-order extendable and expandable bandpass noise-shaping will design. Conclusions will be drawn in section IV.

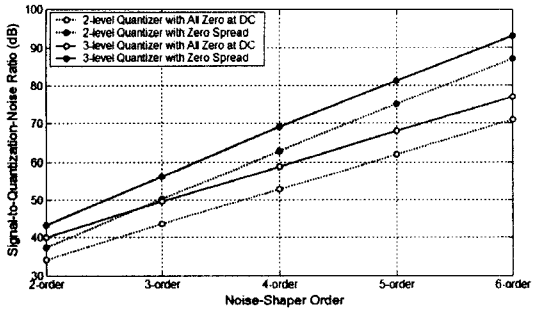

Figure 1. Peak SNQR vs. Noise-Shaper order with 8xOSR

2. Architecture Study

The proposed novel architecture of a semi-MASH sub-stage is shown in Figure 2. The analog part of a high-order sigma–delta modulator includes a chain of Semi-MASH sub-stages, each of them consisting of two first-order sigma-delta modulators. These comprise a half-delay integrator in the forward path and a half-delay in the feedback path. The minimum-noise-shaping-per-stage is used to minimize the overload region to 0dB independently of the number of stages. It results in an expandable architecture [2]. Traditionally, MASH architectures that are obtained from the combination of first-order sigma-delta modulators will force all zeros to be located at DC. Moreover, the pattern noise and tone in the first stage is very large due to the usage of one-order noise-shaping. If imperfect digital cancellation occurs, the color noise and tone will leak to the final output and will imply a larger distortion.

In the proposed Semi-MASH topology (1+1-...), a stage feedback path is applied to merge these two first-order SDM stages. It can spread two NTF zeros from DC by appropriate control of the feedback and using adequate error cancellation logic. On the other hand, the feedback acts as dithering for the first stage SDM to suppress the pattern noise and tone. Imperfect cancellation will only cause white noise leakage but not distortion. If perfect cancellation occurs, the signal transfer function and noise transfer function of the proposed Semi-MASH are obtained as presented in (1) ~ (3). The digital cancellation logic used to cancel the internal quantizer error can be expressed as (4) ~ (5). Where the NTF zero location is given by (6) and if N is odd, one additional NTF zero appears at DC. The overall modulator output is the summation of all sub-stage output multiply by the corresponding cancellation logic.

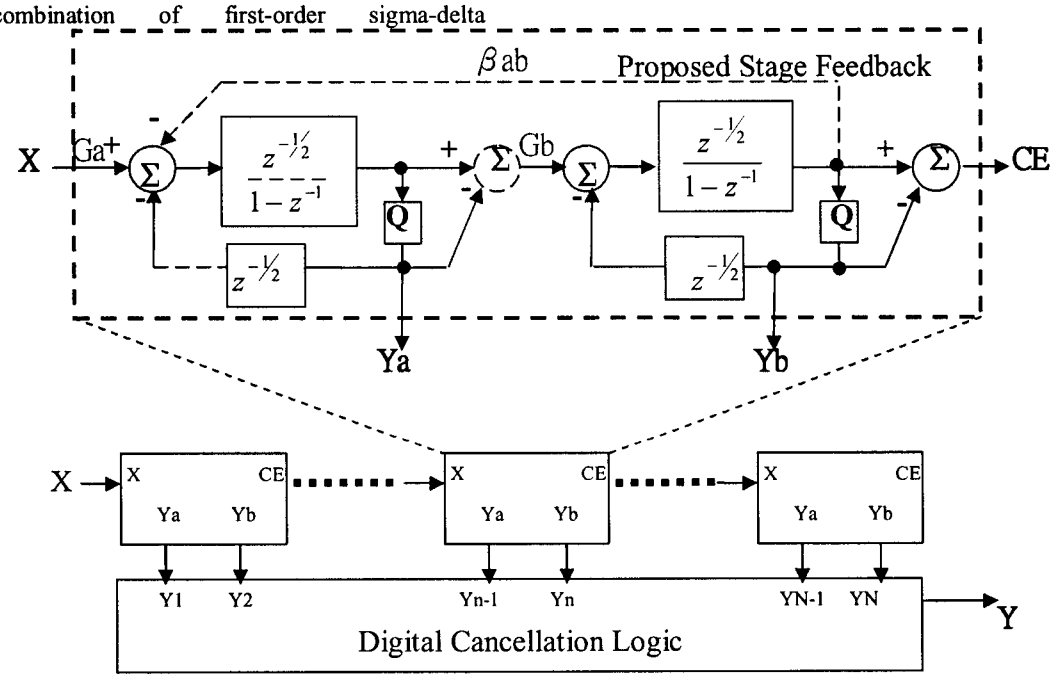

Figure 2. Block Diagram of a Semi-MASH sub-stage.

$$STF = G_1 \times \left(z^{-1/2}\right)^N \quad (1)$$

$$NTF_N|_{N\ is\ odd} = \left(1 - z^{-1}\right) \times \frac{\prod_{i=1}^{(N-1)/2} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{N} G_i} \quad (2)$$

$$NTF_N|_{N\ is\ even} = \frac{\prod_{i=1}^{N/2} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{N} G_i} \quad (3)$$

$$Hy_n|_{n\ is\ odd} = \left(z^{-1/2}\right)^{(N-n)} \times \frac{\prod_{i=1}^{(n-1)/2} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{n} G_i} \quad (4)$$

$$Hy_n|_{n\ is\ even} = \left(z^{-1/2}\right)^{(N-n)} \times \frac{\prod_{i=1}^{n/2-1} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{n} G_i} \times \left(1 + (G_n\beta_{(n-1)n} - 1)z^{-1}\right) \quad (5)$$

$$f\theta_i = \pm \frac{fs}{2\pi} \cos^{-1}\left(1 - \frac{G_{2i}\beta_{(2i-1)2i}}{2}\right) \quad for \quad i = 1 \sim floor\left(\frac{N}{2}\right) \quad (6)$$

$$Y = \sum_{i=1}^{N} (H_i \times Y_i) = X \times STF + E_N \times NTF_N \quad (7)$$

The designation of semi-MASH will stand for two stages not individualized and merged into a half-MASH structure. The notation 1+1 stands for the following meaning: two first-order noise-shaping are added together to become a second-order noise-shaping (1+1=2). This Semi-MASH topology contains two main benefits: firstly, it reduces the systematic loss by using minimize-noise-shaping-per-stage to keep 0 dB overload point regardless of the number of stages; secondly, it extends the noise-shaping by appling a feedback within each stage and using appropriate error cancellation logic to spread the NTF zero within the bandwidth. The color noise due to first-order noise-shaping will also be suppressed by the stage feedback. When compared with traditional MASH designs and their corresponding trade-offs, the proposed topology will result in a higher performance and more systematic design flow, with a higher degree of design flexibility and optimization.

Behavior simulations have been done in MATLAB and SIMULINK to verify the novel proposed architecture, using 8x OSR and 1.5-bit internal quantizer. The input level is normalized to the quantizer full swing which minimizes the quantization error. The sampling frequency is normalized to 1 and bandwidth to 0.0625. In Figure 3, the plus marker stands for MASH 1-1-... from 2 to 6 numbers of stages and circle marker stands for Semi-MASH 1+1-... from 2 to 6 numbers of stages. The proposed Semi-MASH is more efficient increasing SNQR when compared with the traditional architecture. The overload point occurs after 0 dB for both architectures due to the use of minimum-noise-shaping-per-stage.

An 8xOSR 1.5-bit 5th-order cascade SDM will be explored as a design example. Figure 4 shows the in-band output PSD and SNQR from MASH 1-1-1-1-1 with input signal level swept. All zeros are forced to be located at DC and the peak SNQR is 67dB whereas the peak SFDR is 76dB. Figure 5 shows the in-band output PSD and SNQR from Semi-MASH 1+1-1+1-1 with input signal level swept. The NTF zero is spread equally within the signal bandwidth and results in lower noise floor. The peak SNQR is 81dB and the peak SFDR is 88dB. More than 14dB SNQR and DR, and 12dB SFDR is gained from the Semi-MASH architecture. The proposed semi-Mash will not suffer form the stability problem.

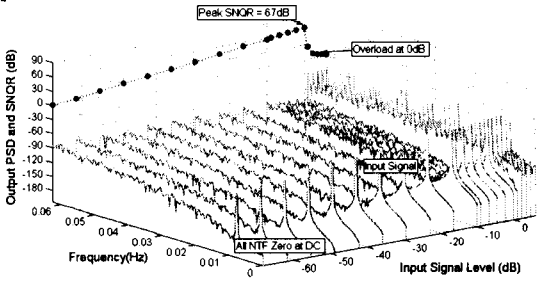

Figure 3. In-band Output PSD and SNQR vs. Input Signal Level with all 5 NTF zero locate at DC.

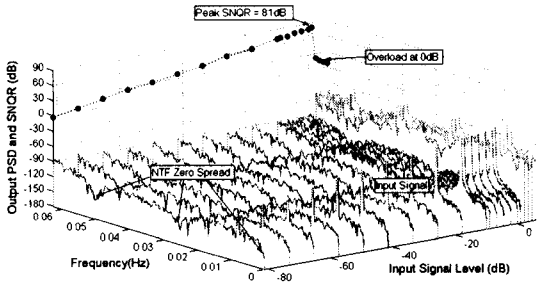

Figure 4. In-band Output PSD and SNQR vs. Input Signal Level with 5 NTF zero equally spread within the bandwidth.

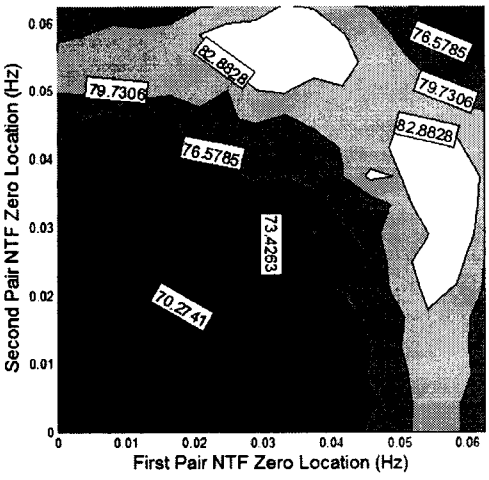

Figure 5. SNQR vs. NTF Zero Location (Contour Plot).

As shown in Figure 1, the SNQR of a 5th order 1.5-bit semi-MASH is higher than a 6th order 1.5-bit MASH. The proposed Semi-MASH architecture reduces one stage and increases power efficiency. We can sweep the NTF zero location to get the optimized NTF zero location. Figure 6 shows the contour plot of SNQR vs. two pair of NTF zero location that is controlled by the stage feedback coefficient β. Since this is a 5th order modulator, one zero is located at DC. As shown in Figure 6, the contour plot is symmetrical and the maximum SNQR occurs at the NTF zero near equally spread. When we have the NTF zero location, we can get the value of the stage feedback coefficient β using (6). The proposed topology introduces an idea to extend the SNQR by add a feedback within two stages.

3. Exbandable and Expandable Bandpass Modulator

The new idea of stage feedback can be extended to other existing sigma-delta topologies such as bandpass, complex, parallel and continuous cascade single/multi-bit SDM to achieve an optimum design. This section will present an example which transfer the proposed semi-MASH sub-stage to bandpass counterpart and combined with existed 2-1Lmb topology. The block diagram of the proposed expandable and extendable high-order bandpass semi-MASH sigma-delta modulator is shown in Figure 1 including the gains associated to different blocks. It is a combination of a bandpass version of 2-1Lmb [2] and semi-MASH technique. The analog part comprises a 4th-order bandpass sigma-delta modulator as the first stage followed by a chain of semi-MASH sub-stages. The first stage quantization gain is 4 to reduce the internal resonator swing and its noise transfer function (NTF) has two zeros at fs/4. On the other hand, its quantizer error will be attenuated by a factor of 2 and also asymmetric coupling will be provide to the subsequent stage in order to minimize the overload region, introducing a systematic loss of 2, i.e., 1-bit loss into the overall noise attenuation. Each semi-MASH sub-stage consists of two 2nd-order bandpass sigma-delta modulators with a feedback sum in between. A quantization gain of 2 is introduced in each modulator to reduce the internal resonator swing.

$$Y = \sum_{i=1}^{N}(H_i \times Y_i) = X \times STF + E_N \times NTF_N \quad (8)$$

$$H_0 = z^{-n} \times \left(1 + \left(1 + z^{-2}\right)^2\right) \quad (12)$$

$$STF = z^{-n} \quad (9)$$

$$H_i|_{even} = 2 \times z^{-(n-i)} \times \left(1 + z^{-2}\right)^2 \times \left(1 + \left(1 - \beta_{(n-1)n}\right)z^{-2}\right) \times \prod_{1}^{i/2-1}\left(1 + \left(2 - \beta_{(2i-1)2i}\right)z^{-2} + z^{-4}\right) \quad (13)$$

$$NTF_n|_{odd} = \left(1 + z^{-2}\right)^3 \times \prod_{1}^{(n-1)/2}\left(1 + \left(2 - \beta_{(2i-1)2i}\right)z^{-2} + z^{-4}\right) \quad (10)$$

$$H_i|_{odd} = 2 \times z^{-(n-i)} \times \left(1 + z^{-2}\right)^2 \times \prod_{1}^{(i-1)/2}\left(1 + \left(2 - \beta_{(2i-1)2i}\right)z^{-2} + z^{-4}\right) \quad (14)$$

$$NTF_n|_{even} = \left(1 + z^{-2}\right)^2 \times \prod_{1}^{n/2}\left(1 + \left(2 - \beta_{(2i-1)2i}\right)z^{-2} + z^{-4}\right) \quad (11)$$

$$f\theta_i = 0.25\,fs \pm \frac{fs}{4\pi}\cos^{-1}\left(1 - \frac{\beta_{(2i-1)2i}}{2}\right) \quad (15)$$

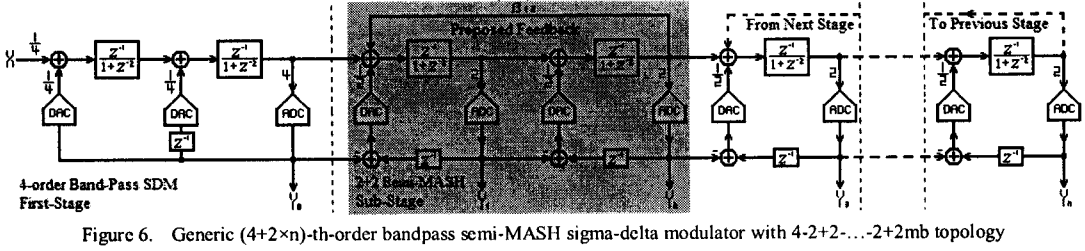

Figure 6. Generic (4+2×n)-th-order bandpass semi-MASH sigma-delta modulator with 4-2+2-...-2+2mb topology

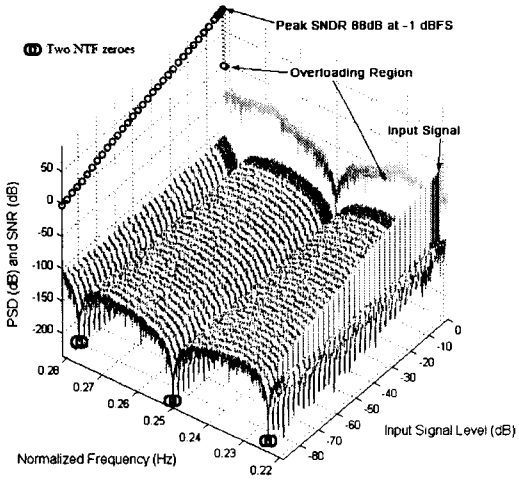

Figure 7. SNQR vs. loop order with different topology for 8xOSR

In the proposed architecture, the feedback within the sub-stage can spread the two NTF zeros away from fs/4 though appropriate control and using the adequate error cancellation logic. If perfect cancellation occurs, the signal (STF) and noise (NTF) transfer functions of the proposed semi-MASH can be obtained as presented from (8) ~ (11), where the digital cancellation logic, used to eliminate the internal quantizer error can be expressed by (12) ~ (14). The location of the NTF zero location is given by (15) and if n is odd, one additional NTF zero occurs at fs/4 as express in (10).

Based on the above architecture and corresponding equations an 8xOSR 12th-order (4+2×4) 1.5-bit band-pass semi-MASH sigma-delta modulator has been designed to demonstrate the superior behavior of the proposed structure. To maximize the SNQR and minimize the coefficient spread, a gain weight of 1/9 is selected for both β12 and β34. Totally 6 NTF zeroes (3 double-zeros) will exist which are located at [0.25-0.0267, 0.25, 0.25+0.0267]×fs. Figure 7 shows the 3D plot of the SNQR versus the input signal level and the PSD within the bandwidth. The SNR curve shows that -1dBFS overloading point is achieved and 90% of the modulator full scale can be used. The output PSD shows that the proposed topology will not be affected by stability since the input signal level is less than -1 dBFS. Comparing the results of this semi-MASH architecture with a 4-2Lmb topology, a more aggressive noise shaping is obtained, on the other hand, comparing it to 4-4Lmb topology, the overload region is now smaller and the systematic loss is avoided due to scaling down the inter-stage quantizer error coupling gain.

Figure 8 shows the SNQR curves and a detailed zoom view for different MASH topologies, with Table I showing their performances summary for 8xOSR. The gray dotted line (a~b) are 12th-order 4-24mb MASH with all NTF zeros forced to DC with (a) having 1-bit internal quantizer and -5 dB overloading point (OL) and (b) having 1.5 bit internal quantizer with -1 dB overloading point. Since a 3-level DAC is inherently linear in differential implementation, comparing it to 1-bit internal quantizer, it will be more effective to use a 1.5 bit internal quantizer in order to minimize the overload region. Then, (c) represents a 12th-order semi-MASH with all β gains equal to 1/9, resulting in a larger 17 dB SNQR gain when compared to (a); (d~f) are obtained from 8th-, 10th- and 12th-order Semi-MASH architectures with 1.5-bit internal quantizers, when led to -1dB constant overload point. In the case of the proposed topology (f) it achieves 88dB SNQR with a gain of 18dB SNQR over the traditional 4-2Lmb topology (b).

Just like most of MASH-type sigma-delta modulators, the inter-stage quantization error leakage is the main drawback that might damage the overall performance. There are three main paths contributing to mismatch leakages: the resonator's feed-forward path gains, the DAC's linearity and the feedback factor β's. Since all resonator's gains of the semi-MASH sub-stage are set to unity, the mismatch in the signal path can be avoided by applying a mismatch-free technique, which will be presented next. The 4th-order bandpass sigma-delta modulator used as first stage contributes for the suppression of all mismatches leakages through a 4th-order band-pass noise shaping. Figure 9 shows the histogram of SNR of -1 dBFS input with different capacitor ratio mismatch standard deviation of the DAC's and the feedback factor β's with 100 Monte-Carlo simulations. Worst case 78-dB SNR is achieved for 0.1% standard deviation in capacitor ratio. Dynamic element matching and calibration technique could be applied to suppression the mismatch leakage. A band-pass DEM technique can also be applied to the DAC, which will be equivalent to apply a high-order noise-shaping (first-stage with a 4th-order noise shaping and a band-pass DEM noise-shaping) for the suppression of the DAC's linearity leakages more effectively.

TABLE I PERFORMANCE SUMMARY FOR DIFFERENCE TOPOLOGY

Topology	SNQR	OL
a. 4-2-2-2-2 MASH; 1-bit	60 dB	-5 dB
b. 4-2-2-2-2 MASH; 1.5-bit	70 dB	-1 dB
c. 4-2+2-2+2 semi-MASH; 1-bit	77 dB	-5 dB
d. 4-2+2 semi-MASH; 1.5-bit	62 dB	-1 dB
e. 4-2+2-2 semi-MASH; 1.5-bit	73 dB	-1 dB
f. 4-2+2-2+2 semi-MASH; 1.5-bit	88 dB	-1 dB

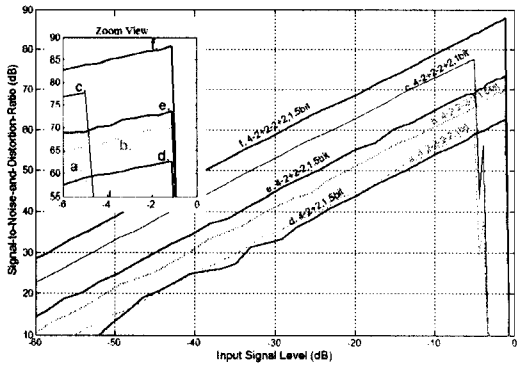

Figure 8. SNQR vs. loop order with different topology for 8xOSR

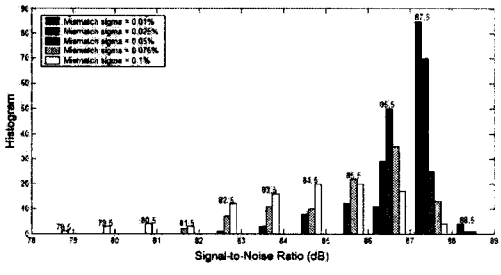

Figure 9. SNQR vs. weight mismatch standard deviation

4. CONCLUSION

By adding feedback within individual MASH sub-stage, the proposed semi-MASH architecture provides the opportunity to spread the NTF zero and minimize the stage overload. Based on the proposed principle, an expandable and extendable architecture can be achieved by combined the exist approach. Furthermore, it can be transfer to bandpass counterpart. The design results in both higher modulator performance and systematic approach. Future work will be continuous develop the proposed principle to other possibility and implement a high-bandwith high-resolution ADC with proposed architecture.

4. ACKNOWLEDGEMENT

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