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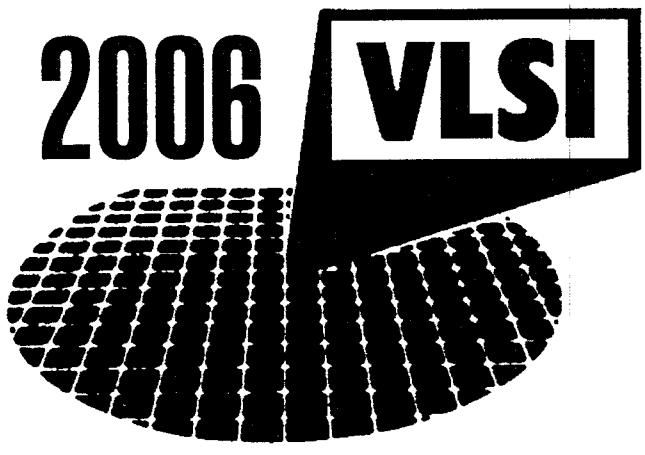
June 15 - 17, 2006 / **HONOLULU**

2006 SYMPOSIUM ON VLSI CIRCUITS

DIGEST OF TECHNICAL PAPERS

20th Anniversary



♦ The IEEE Solid-State Circuits Society

♦ The Japan Society of Applied Physics

SESSION 26

RF Front Ends and Baseband Processing

Saturday, June 17, 10:50 a.m.
Tapa III

Chairpersons: A. Abidi, University of California, Los Angeles
M. Ito, Renesas Technology

26.1 – 10:50 a.m.
A 0.5 V 900 MHz CMOS Receiver Front End, N. Stanic, P. Kinget, Y. Tsividis, Columbia University, New York, NY

26.2 – 11:15 a.m.
Multi-band (1-6GHz), Sampled, Sliding-IF Receiver With Discrete-Time-Filtering in 90nm Digital CMOS Process, H. Lakdawala, J. Zhan, A. Ravi, S. Anderson, B.R. Carlton, R.B. Nicholls, N. Yaghini, R.E. Bishop, S.S. Taylor, K. Soumyanath, Intel Corp., Hillsboro, OR

26.3 – 11:40 a.m.
A Cartesian-Feedback Linearized CMOS RF Transmitter for EDGE Modulation, L. Tee, E. Sacchi*, R. Bocock, N. Wongkomet, P.R. Gray, University of California, Berkeley, CA, *STMicroelectronics, Pavia, Italy

26.4 – 12:05 p.m.
A 1V 14mW-per-Channel Flexible-IF CMOS Analog-Baseband IC for 802.11a/b/g Receivers, P.-I. Mak, S.-P. U*, R.P. Martins**, University of Macau, Macao, China, *Chipidea Microelectronics, Ltd., Macao, China, **Instituto Superior Tecnico, Lisbon, Portugal

26.5 – 12:30 p.m.
A 31.2mW UWB Baseband Transceiver with All-Digital I/Q-mismatch Calibration and Dynamic Sampling, J.-Y. Yu, C.-C. Chung, H.-Y. Liu, Y.-W. Lin, W.-C. Liao, T.-Y. Hsu, C.-Y. Lee, National Chiao-Tung University, Taiwan

A 1V 14mW-per-Channel Flexible-IF CMOS Analog-Baseband IC for 802.11a/b/g Receivers

Pui-In Mak, Seng-Pan U [1] and R. P. Martins [2]

Analog and Mixed-Signal VLSI Laboratory, FST, University of Macau, Macao, China (E-mail: p.i.mak@ieee.org)
1 – Chipidea Microelectronics (Macao) Ltd., 2 – On leave from Instituto Superior Técnico (IST)/UTL, Lisbon, Portugal

Abstract

Presented is a low-voltage low-power analog-baseband IC featuring a *two-step channel-selection* architecture for a flexible-IF reception of 802.11a/b/g. In circuits, it integrates innovatively *series-switching* mixers for a precise I/Q demodulation; an *inside-OpAmp* dc-offset cancellation for area savings and switchability, a *switched-current-resistor* programmable-gain amplifier for a transient-free constant-bandwidth gain adjustment. Fabricated in a 0.35μm CMOS process, each channel consumes 14mW from 1V, while measuring <1μs gain-switched transient, 32/90dB stopband rejection at 20/40MHz and 15.2dBm IIP3.

Introduction

Low-voltage circuits are the key to enabling fully integrated wireless transceivers in finer CMOS processes for cost and power reductions. Unlike previous low-voltage works mainly developed at block level for single application (e.g., [1]), this work integrates all essential analog-baseband (BB) functions for 802.11a/b/g receivers on a single chip. The use of a flexible-IF architecture with *two-step channel selection* [2] and certain voltage-/power-/area-conscious circuit techniques enable, to our knowledge, the lowest voltage (i.e., 1V) implementation of filtering, amplification, I/Q demodulation and dc-offset cancellation for 802.11a/b/g WLAN, while using a 0.35μm CMOS process (in [3], 1.4V is used in 90nm CMOS). Without resorting to any process option like low-threshold devices, the described techniques are directly migratable to forthcoming sub-1V standard processes, in which the threshold voltages, forecasted by *the International Technology Roadmap of Semiconductors* (ITRS) [4], will be within 0.2 ~ 0.3V for wireless.

Architectural Techniques

Fig. 1 shows the block diagram of the implemented analog-BB IC. The BB signal conditioning for 802.11a/b/g is coordinated at a 10/0/12.5MHz IF, respectively. The zero-IF (ZIF) in brief is to satisfy 802.11b with the simplest structure, whereas the low-IFs (LIFs) are to alleviate the tradeoff between response time and intersymbol interference in highpass filtering, and save the essential for an automatic frequency control [5]. In LIF mode, a preselect filter with a dual-channel bandwidth (BW) prevents the residual in-band channels and out-of-band white noise, in the subsequent IF-to-BB downconversion, from aliasing to the BB. A double-quadrature down-converter (DQDC), made up of quad series-switching (SS) mixers, is driven by a mixed-mode clock generator (CLKGEN) to generate an I/Q signal with precise quadrature matching. In order to complete the second step of channel selection, the DQDC is designed to have sideband selectivity [i.e., switch the phase (0°, 180°) of its I/Q-coupled paths]. The downconversion is performed upstream the filtering and amplification, such that the mode reconfigurations from LIF to ZIF are halving the BW of the preselect filter and disabling the DQDC and CLKGEN. For power and area savings, a 3-stage 17-MHz-constant-BW programmable-gain amplifier (PGA) is adopted instead of a wideband (>100 MHz) PGA. Thus, without sacrificing the constancy of the selectivity against gain, a 2-fold relaxation of the LPF from 5th to 3rd order is achieved. A distributed dc-offset cancellation (DOC) scheme is realized by embedding in each LPF's and PGA's OpAmp a switchable DOC loop, by which the differential signal is locally balanced and the composite highpass pole is fast switchable to a higher/lower frequency value to deal with short preamble/normal reception. The gain, BW and mode are controlled digitally. Built-in setup for block-level testability is integrated.

Circuit Techniques

Fig. 2 shows the I-channel preselect filter and DQDC. The BW of the preselect filter is controlled via switching the capacitor C_{PF} between the ground and differential branches. Subsequent to filtering, R_{PF} converts linearly the input voltage to current for the current-mode doubled-balanced DQDC. The swapper and mixer-switch S_M, driven by the CLKGEN, generate 2 rail-to-rail amplitude-matched quasi-I/Q sequences: I= [...1, 0, -1, 0...] and Q= [...0, 1, 0, -1...]. Within the tolerable timing errors, $T_{AE1}\leq$ 25/20ns and $T_{AE2}\leq$50/40ns for 10/12.5MHz IF, no phase mismatch occurs. Since the swapper is activated only when S_M is in open-state, it does not impose charge injection and avoids self-mixing in overall. The reset-switch S_{RS} reduces the conversion loss and memory effect during swapping of the differential branches. The IF channel selection is executed transparently by switching the phases SW_Q and SW_Q' inside the CLKGEN. The input common-mode feedback (CMFB) biases the virtual ground to 0.1V for operating OpAmp's transistors in moderate inversion.

The filtering and amplification are co-performed by a 3rd-order (uniquad +biquad) Butterworth LPF and a 3-stage PGA as shown in Fig. 3. Through iterative simulations and with a positive zero (R_{ff} and C_z) added in the PGA's 3rd-stage, the simulated group-delay peaking at the band edge is 14.8ns. The resistor R_{BW} is a resistor array for tuning the BW digitally. A 52dB-gain-switched transient of 1μs is achieved by using a switched-current-resistor (SCR) bank (Fig. 3 lower right), i.e., the current sources $[I_{fb,1}\cdots I_{fb,n}]$ replace the OpAmp to deliver the dynamic dc currents for the gain-tuning resistors $[R_{fb,1}\cdots R_{fb,n}]$, and the grounded resistors $[R_{x,1}\cdots R_{x,n}]$ sink the same currents out from the virtual ground. The fixed dc current $I_{fb,dc}$ in the feedback resistor R_{ff}, thereby stabilizes the dc operating points of the OpAmp and I/O CMFBs. $[I_{fb,1}\cdots I_{fb,n}]$ are generated by a linear resistor-to-current converter to ensure process spread, temperature and mismatch immunities. The corresponding design equation is given by,

$$\beta = \frac{V_{cm,in}}{V_{cm,out}} = \frac{R_{ff} \,//\, R_{x,1} \cdots // \, R_{x,n}}{R_{ff} \,//\, R_{x,1} \cdots // \, R_{x,n} + R_{fb} \,//\, R_{fb,1} \cdots // \, R_{fb,n}} \quad (1)$$

where β is the feedback factor and $V_{cm,in}/V_{cm,out}$ are the I/O common-mode levels of the OpAmp. With $V_{cm,in}$=0.1V, $V_{cm,out}$=0.5V, R_{fb}=4·R_{ff} and $R_{fb,n}$=4·$R_{x,n}$ for n=1,2,3..., any gain step of 6dB shows a β of 0.2. Without the technique, β will vary between 0.2 (at 12 dB) and 0.8 (at -12 dB), resulting in a BW variation as large as 400%.

Each OpAmp has a built-in switchable DOC loop (Fig. 3 lower left) such that in closed loop the frequency of the highpass pole will be lowered by an amount of loop gain. Such a technique, along with the use of subthreshold-biased-transistor current amplifiers (CAs) and dual parallel-compensated PMOS capacitors in circuit, implements a composite 3kHz lower -3dB point in 0.1mm^2. Convergent speed is doubled by interfacing the OpAmp with a sink/source-exchangeable current device. The feedback node is of inherent low impedance dividing the transconductance (TCA) and transimpedance (TIA) amplifier stages for transient-free switching. Because the DOC loop is preceded by the TCA and is operated inside the LPF's or PGA's feedback loop, its input-referred noise is of minor level.

Experimental Results and Benchmarks

Fig. 4 shows the stable BW responses for 802.11b (left) against gain, and the gain responses for 802.11a and g (right). The tunable BW is 2.4MHz. The standard deviation of the upper/lower -3dB point over 52dB gain range is 8.6%/12.4%. The dynamic performances with all DOC loops switched on/off and a 52dB gain-step applied are shown in Fig. 5(a) and (b), respectively. No noticeable transient was observed. The IC consumes 14mW per channel. Excluding the blocks for testability, 3mm^2 active area is measured. Overall performance is summarized in Table 1 and the chip micrograph is showed in Fig. 6. A specific bypass setup and floor plan with dual matched test buffers enables both full-chip and block-net-response tests that are independent to the off-chip I/O test networks and test buffers.

Comparing this work with the state-of-the-art analog-BB ICs in Table 2, it employs the lowest supply voltage up to date without increasing the power, degrading the linearity and noise, or using leading-edge technologies. In addition, this work features a flexible-IF operation and a two-step channel selection to simplify the overall structure.

References

[1] L. Leung *et al.*, *Symp. on VLSI Circuits*, pp. 252-255, Jun. 2005.
[2] P.-I. Mak *et al.*, *T-CAS I*, vol. 52, No. 7, pp. 1302-1315, Jul. 2005.
[3] M. Elmala *et al.*, *Symp. on VLSI Circuits*, pp. 302-303, Jun. 2005.
[4] ITRS, http://www.itrs.net/Common/2004Update/ 2004_04_Wireless.pdf
[5] A. Behzad *et al.*, *ISSCC*, pp. 356-357, 499, Feb. 2003.

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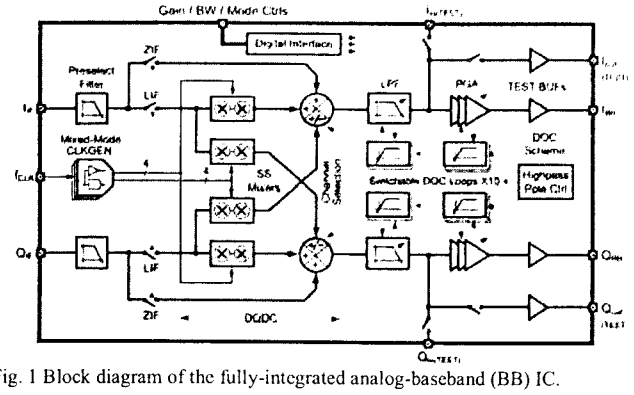


Fig. 1 Block diagram of the fully-integrated analog-baseband (BB) IC.

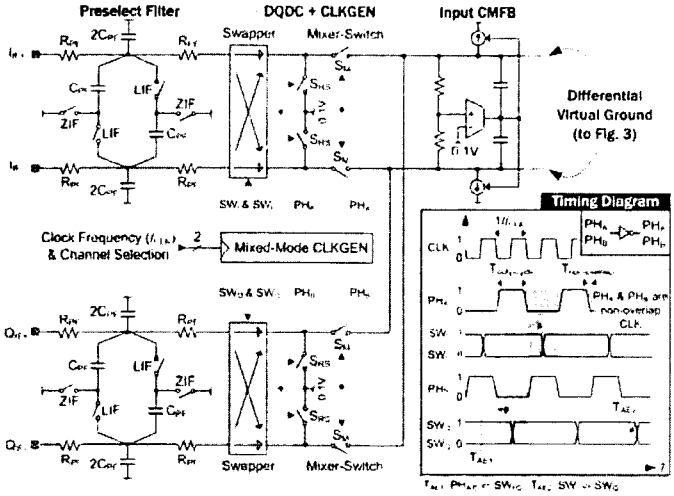


Fig. 2 I-channel preselect filter and double-quadrature downconverter (DQDC).

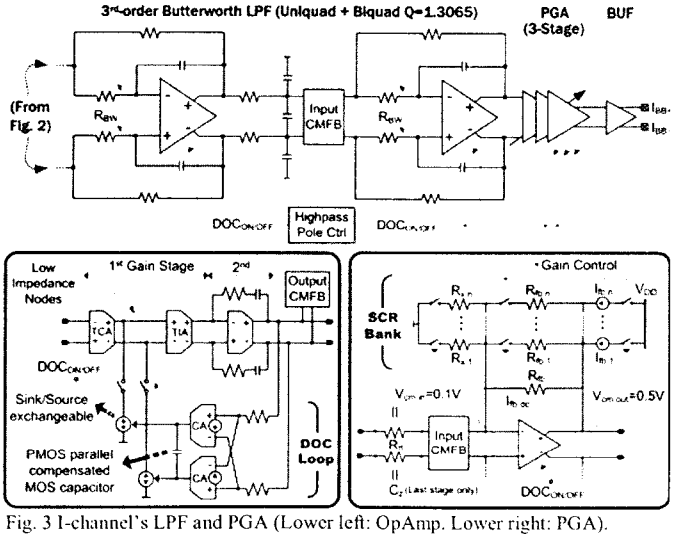


Fig. 3 I-channel's LPF and PGA (Lower left: OpAmp. Lower right: PGA).

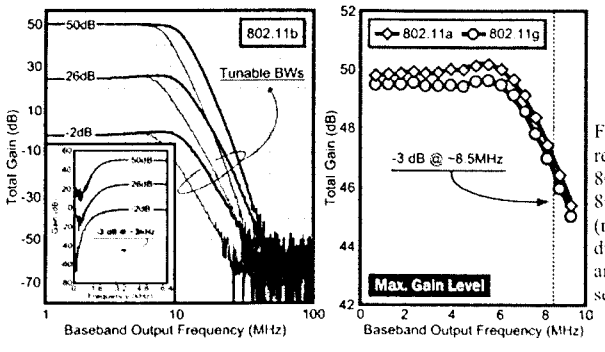
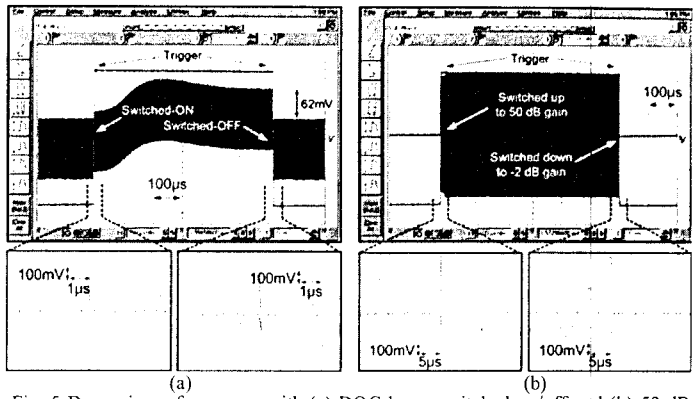


Fig. 4 Gain responses for: 802.11b (left), 802.11a and g (right), with different gain and BW settings.



(a) (b)

Fig. 5 Dynamic performances with (a) DOC loops switched on/off and (b) 52-dB gain step applied.

Table 1 Chip summary.

Parameter		Value
Supported Intermediate Frequencies for 802.11a/b/g		10 / 0 / 12.5 MHz
Supported Modulations / Bands	802.11a	OFDM / 5.15 - 5.725 GHz
	802.11b	CCK / 2.40 - 2.58 GHz
	802.11g	OFDM, CCK / 2.40 - 2.58 GHz
Power Supply		1 V ±10%
Voltage-Gain Range		-2 dB ... +50 dB (2 dB/step)
Upper / Lower -3 dB Point (upper one is tunable)		6.54 - 8.95 MHz / 3 kHz
St. Dev. (σ) of Upper / Lower -3 dB Point over 52 dB Gain Range		8.6 / 12.4 %
Gain-Switched Transient Time (tested by a 52 dB gain step)		< 1 µs
IF Channel-Selection Transient Time		0.38 µs
In-Band IIP3 at Min. Gain (referred to 50 Ω)		15.2 dBm
Stopband Rejection at 20/40 MHz offset (8.5 MHz BW, max. gain)		32.05 / 90.6 dB
I/Q Isolation		> 60 dB
Averaged In-Band I/Q Impairment in 802.11a/g Mode	Amplitude	0.175 / 0.158 dB
	Phase	0.39 / 0.7 °
Averaged In-Band Image Rejection Ratio in 802.11a/g Mode		40.19 / 39.74 dB
Input-Referred Noise Spectral Density / Noise Figure (white)		22.5 nV/√Hz / <30 dB
Power per channel at 0.9 / 1 / 1.1 V (excluded the test buffers)		13 / 14 / 16.5 mW
Technology		0.35µm 4M2P CMOS
Active Core Area (I/Q PGAs + I/Q LPFs + Preselect filter & DQDC + CLK + Other Blocks)		3.06 mm² (1.44+1.12+0.25+0.05+0.2)

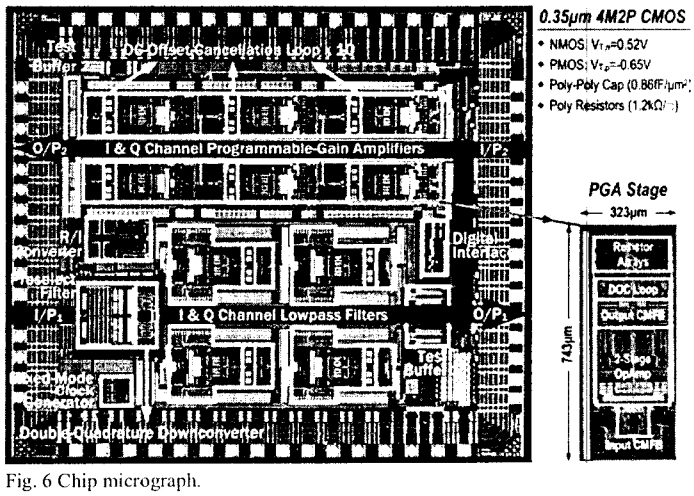


Fig. 6 Chip micrograph.

Table 2 Brief comparsions of state-of-the-art analog-BB ICs.

	W. Schelmbauer *et al.* RFIC'02 *	H. Elwan *et al.* T-CAS II'02 **	M. Elmala *et al.* VLSI Circuits '05 [3]	This Work
Applications	WCDMA	Bluetooth	WLANs	WLANs
Supply Voltage	2.7 V	3 V	1.4 V	1 V
Power per channel	19.4 mW	3.6 mW	13.5 mW	14 mW
Input-referred Noise Density	8 nV/√Hz	43.2 nV/√Hz	19 nV/√Hz	22.5 nV/√Hz
IIP3 (minimum gain)	+20.6 dBV_{rms}	+12.2 dBm	+2 dBm	+15.2 dBm
Stopband Rejection	43 dB @ 3.1 MHz	62 dB @ 15 MHz	N/A	32 dB @ 20 MHz
Gain Range	-15.5...+48.5 dB	+12...+30 dB	+13.5...+67.5 dB	-2...+50 dB
Technology	75 GHz BiCMOS	1.2 µm CMOS	90 nm CMOS	0.35 µm CMOS

*: W. Schelmbauer *et al.*, *Symp. on RFIC*, pp. 267-270, Jun. 2002.

**: H. Elwan *et al.*, *T-CAS II*, vol. 49, no. 8, pp. 545-554, Aug. 2002.