A Novel Low-Voltage Finite-Gain Compensation Technique for High-Speed Reset- and Switched-Opamp Circuits

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***Abstract*— This paper proposes a novel finite-gain compensation technique that can be applied to low-voltage high-speed reset- and switched-opamp circuits. The proposed technique utilizes an Auxiliary Differential-Difference Amplifier (A-DDA) that senses and corrects the finite-gain error from the virtual ground of the main opamp (with the effective gain in the order of βA^2), thus allowing the use of high-speed single-stage low-gain opamps (instead of usual low-speed two-stage amplifier with large power consumption) to achieve high-speed operation. Simulations of a reset-opamp 10-bit 100 MHz pipelined ADC in 1.2-V supply voltage are presented using 0.18μm CMOS, with the Signal-to-Noise-and-Distortion Ratio (SNDR) improved from 46.77 dB to 58.51 dB and thus verifying the effectiveness of the proposed circuit.**

I. Introduction

Decreasing supply voltage imposed by down-scaling of technology as well as the increasing demands of battery devices continuously placed more stringent requirements on CMOS analog and mixed-signal integrated circuits [1-5]. The main difficulties in very low-voltage circuit designs include the inability to turn on the floating switches [5], and also the hard task of designing low-voltage opamps due to the limited voltage headroom [3]. In order to alleviate the floating switch problem, two truly low-voltage state-of-the-art techniques, namely reset-opamp [3,5] and switched-opamp [2,4], are available to deal with such problems in modern low-voltage designs. In addition, two low-voltage circuit techniques have also been recently proposed [6,7] that further allow the implementation of power efficient fully-differential opamps and input interfaces, by using low-voltage SC-CMFB (Switched-Capacitor Common-Mode Feedback) [6] and cross-coupled passive sampling circuits [7]. The combination of both techniques will result in significant savings in opamp power consumption by avoiding pseudo-differential opamps (two-single-ended opamps) [6] and the extra Track-and-Reset (T/R) interfaces [7].

Nevertheless, due to the low supply voltage the design of opamps is still restricted to traditional two-stage opamps [3,6], which by their nature have lower speed (due to the additional high-impedance node that needs miller compensation) and higher power consumption (as a result of more current branches). Using single-stage opamps with low gain can cause serious systematic errors like nonlinearity in MDACs of pipelined ADCs or poles and zeros deviations in SC filters or sigma-delta modulators, unless the produced finite-gain error can be compensated, with, for example, traditional Correlated Double Sampling (CDS) techniques [8,9]. However this cannot be applied in a low-voltage environment due to (a) limitations caused by the floating switch problems and (b) the fact that the opamp is switched off or reset in one clock phase, which implies that it would not be idle and cannot be used to compensate the gain error. To overcome these drawbacks a low-voltage finite-gain compensation technique can be used [4], but it has also a restriction of narrow-band operation (typically a bandpass sigma-delta modulator) that limits the signal band to be located only narrowly at $f_s/4$.

In this paper a novel low-voltage finite-gain-compensation technique is proposed. It utilizes an Auxiliary Differential-Difference Amplifier (A-DDA) to measure and compensate the finite-gain errors from the virtual ground of the main opamps, thus allowing the use of low-power high-speed single-stage opamps in both the main and the auxiliary amplifier to achieve low-voltage and high-speed operation. The effectiveness of the proposed technique is independent of the signal or the sampling frequency, and is valid in a wide input bandwidth up to the Nyquist frequency of the system. The principle is applicable to both reset- and switched-opamp circuits, as well as to various types of low-voltage SC circuit building blocks such as the integrators in SC filters, sigma-delta converters and MDACs in pipelined ADCs. Simulations of a 1.2-V 10-bit 100 MHz reset-opamp pipelined ADC are presented to verify the effectiveness of the proposed technique.

II. Low-Voltage Finite-Gain Compensation

To demonstrate the idea of low-voltage finite-gain compensation, consider the proposed reset-opamp low-voltage MDAC used in a pipelined ADC, as shown in Fig. 1. Although the foregoing analysis is presented for a reset-opamp MDAC circuit, the principle can also be applied to various types of low-voltage SC building blocks such as the Sample-and-Hold (S/H), integrators, as well as switched-opamp circuits. In the figure only a single-ended version is shown for simplicity, although the real implementation is fully-differential. The upper part of Fig. 1 is the main MDAC amplifier, which performs its function as usual. Due to low supply voltage the reference voltage V_{ref} cannot be inserted directly into

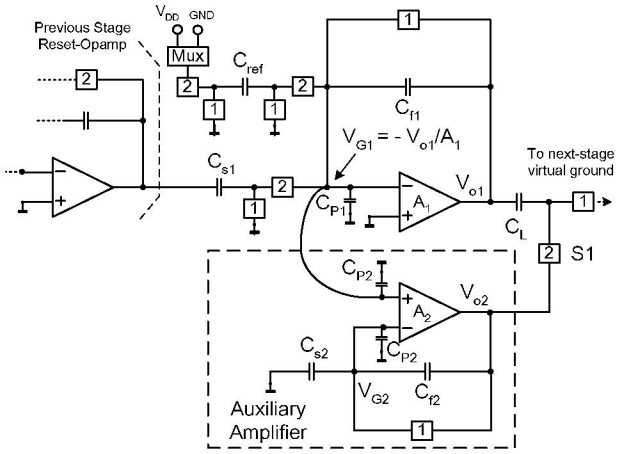

Fig. 1: The proposed finite-gain compensated reset-opamp MDAC with main and auxiliary amplifier.

the signal path, and a multiplexer is used with a switched-capacitor C_{ref} to inject the reference voltage into the virtual ground, as similar to previous implementations [5]. At phase 1, the input signal from the previous stage is sampled in C_{s1}, while in phase 2 the previous stage's opamp reset to discharge the sampling capacitor C_{s1} to virtual ground. Without considering the proposed auxiliary amplifier, it can be derived that the MDAC performs the following arithmetic function (including the effects of input parasitic capacitance C_{P1} and finite gain A_1):

$$V_{o1} = \frac{C_{s1}}{C_{f1}} V_{in} - mV_{DD}\frac{C_{ref}}{C_{f1}} + \frac{1}{\beta_1}\left(-\frac{V_{o1}}{A_1}\right) \tag{1}$$

where

$$\beta_1 = \frac{C_{f1}}{C_{s1} + C_{f1} + C_{ref} + C_{P1}} \tag{2}$$

is the feedback factor and m is equal to either 1, 0, or -1 depending on the sub-ADC decision. In the right-hand side of (1) the V_{o1} term will not be moved and combined with V_{o1} in the left-hand side because the term

$$-V_{o1}/A_1 = V_{G1} \tag{3}$$

actually corresponds to the virtual ground voltage of A_1 and it is clearly evident now that the virtual ground error voltage is being amplified by the inverse of the feedback factor ($1/\beta_1$) to the output, which is the origin of finite-gain error. As demonstrated in Fig. 1, the fundamental idea of the proposed solution is to sense the main opamp virtual ground voltage by an auxiliary amplifier in non-inverting configuration, amplify it by the same feedback factor, and then to feed it into the bottom plate of C_L to cancel the gain error.

The output of the auxiliary amplifier can be derived as:

$$V_{o2} = \frac{C_{s2} + C_{f2} + C_{P2}}{C_{f2}} V_{G2} = \frac{1}{\beta_2} V_{G2} \tag{4}$$

and

$$V_{G2} = V_{G1} - V_{o2}/A_2 \tag{5}$$

which means that the gain of the auxiliary amplifier will also contribute to the total gain error. Substituting (5) into (4) yields

$$V_{o2} = \frac{1}{\beta_2} V_{G1} - \frac{V_{o2}}{\beta_2 A_2} = \frac{V_{G1}}{\beta_2[1+1/(\beta_2 A_2)]} = -\frac{V_{o1}}{\beta_2 A_1[1+1/(\beta_2 A_2)]} \tag{6}$$

Now for the main amplifier, the feedback factor should be modified to account for the input parasitic C_{P2} from the auxiliary amplifier:

$$\beta_1' = \frac{C_{f1}}{C_{s1} + C_{f1} + C_{ref} + C_{P1} + C_{P2}} \tag{7}$$

and first assuming that $\beta_1' = \beta_2 = \beta$, which means that the main and the auxiliary amplifiers would have the same feedback factor. Then, the equivalent output voltage that is sampled into the capacitor C_L in phase 2, as shown in Fig. 1, is

$$\begin{aligned} V_{o1} - V_{o2} &= \frac{C_{s1}}{C_{f1}} V_{in} - mV_{DD}\frac{C_{ref}}{C_{f1}} + \frac{1}{\beta}\left(-\frac{V_{o1}}{A_1}\right) - \frac{-V_{o1}}{\beta A_1[1+1/(\beta A_2)]} \\ &= \frac{C_{s1}}{C_{f1}} V_{in} - mV_{DD}\frac{C_{ref}}{C_{f1}} + \frac{-V_{o1}}{\beta^2 A_1 A_2[1+1/(\beta A_2)]} \\ &\approx \frac{C_{s1}}{C_{f1}} V_{in} - mV_{DD}\frac{C_{ref}}{C_{f1}} + \frac{1}{\beta}\left(\frac{-V_{o1}}{\beta A_1 A_2}\right) \\ &\approx \frac{C_{s1}}{C_{f1}} V_{in} - mV_{DD}\frac{C_{ref}}{C_{f1}} + \frac{1}{\beta}\left[\frac{-(V_{o1}-V_{o2})}{\beta A_1 A_2}\right] \end{aligned} \tag{8}$$

assuming $\beta A_2 >> 1$ and $\beta A_1 >> 1$ such that V_{o2} is small compared with V_{o1} as indicated by (6). Also comparing (8) with (1) it can be deducted that the effective gain has been boosted from A_1 to $\beta A_1 A_2$ with the proposed technique.

To achieve the proposed gain compensation, the feedback factor of both the amplifiers should be matched as follows:

$$\frac{C_{s1} + C_{ref} + C_{P1} + C_{P2}}{C_{f1}} = \frac{C_{s2} + C_{P2}}{C_{f2}} \tag{9}$$

Note that C_{P1} and C_{P2} depend on the biasing condition of the differential pairs of both amplifiers. However, (9) can be easily satisfied by using the same sizes and biasing conditions for both of the input differential pairs (that makes C_{P1}=C_{P2}) and by choosing the following capacitor ratios:

$$C_{s1} + C_{ref} = 2C_{s2},\ C_{f1} = 2C_{f2} \tag{10}$$

Actually, several alternatives satisfying (9) can be used, like for example a scaled-down version of the differential pair in the auxiliary amplifier, as well as the choice of the corresponding capacitor ratios according to (9).

In Fig. 1 a switch S1 is used in the auxiliary opamp output to disconnect C_L at phase 1, such that C_L can be discharged to next stage virtual ground. This switch can be turned on and off without any problem since the auxiliary amplifier is processing the gain error from the main opamp as shown in (6), which has relatively small signal swing in the order of a few mV. Similarly, the nonlinearity produced by its on-resistance is also negligible.

III. The Auxiliary Differential-Difference Amplifier

It might seem that the proposed technique will double the power consumption since an additional amplifier is needed. However, the additional power consumption is traded-off with the significant increase of the single-stage opamps' Gain-Bandwidth Product (GBW). Moreover, a low-voltage SC-CMFB circuit [6] can be used to allow fully-differential operation, which can further cut half of the opamps' power.

The traditional implementation of a fully-differential non-inverting auxiliary amplifier is not possible, since both opamp

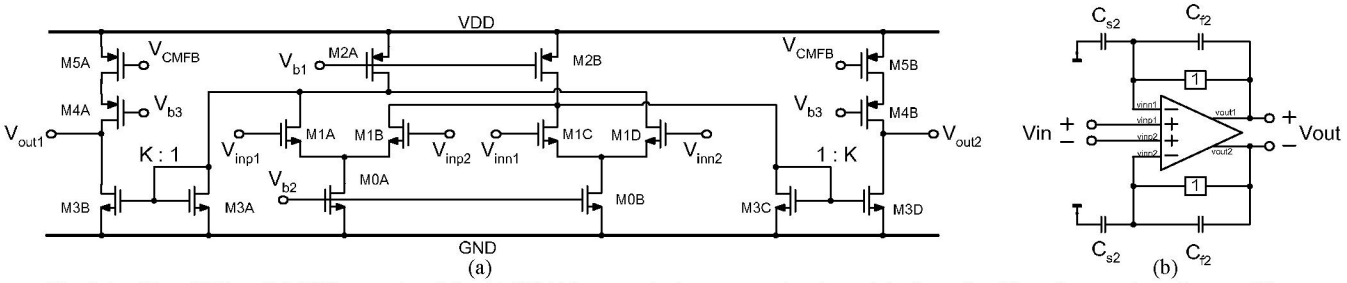

Fig. 2 Auxiliary Differential-Difference Amplifier (A-DDA) in current mirror opamp topology: (a) schematic; (b) used as non-inverting amplifier.

inputs are used as virtual grounds in the differential circuit. Differential-Difference Amplifier (DDA) can be used to implement the fully-differential non-inverting amplifier [10], and Fig. 2a presents the Auxiliary Differential-Difference Amplifier (A-DDA) in current-mirror opamp topology which will be used in the simulations of the subsequent section. The A-DDA consists of two differential pairs with 4 inputs (2 for virtual grounds and 2 for non-inverting inputs, as shown in Fig. 2b), with their currents sum at the drain of M2A and M2B, and afterwards folded into the diode M3A and M3B and eventually mirrored to the output. The output voltage and GBW of the opamp can be expressed as follows [4, 10]:

$$V_{out1} - V_{out2} = Kg_{m1}[(V_{inp1} - V_{inp2}) - (V_{inn1} - V_{inn2})]R_{out} \quad (11)$$

$$GBW = Kg_{m1}/(2\pi C_{Ltot}) \quad (12)$$

where R_{out} represents the equivalent output resistance, K is the current mirror ratio and C_{Ltot} is the total capacitive load.

Several special techniques are applied to the A-DDA in Fig. 2 to further improve its speed, namely: (a) the NMOS differential pairs have inherently larger transconductance than their PMOS counterparts and their drain current is folded into the diode M3A and M3B, which are also NMOS such that the phase margin is not degraded significantly by this current mirror pole in the signal path. Such configuration can achieve potentially higher speed than the traditional current mirror opamp with NMOS differential pair and PMOS current mirror; (b) Cascode transistors M4A and M4B are added into the output current branch to shield the PMOS current source transistors M5A and M5B from the Miller multiplication of the output node, which can significantly increase the input capacitance of the CMFB feedback point and thus slow down the common-mode response. Also, due to the cascode, it is possible to use minimum length transistors in M5A and M5B to further reduce their input parasitics. The cascode transistor may approach the vicinity of triode region in a low-voltage environment, but since the output resistance is dominated by the NMOS side (M3B and M3D), the resulting nonlinearity will be suppressed. Such arrangement can still provide a 6 dB benefit to the gain as the output resistance now becomes $r_{o,M3B}$ rather than $r_{o,M3B} // r_{o,M5A}$.

IV. Simulation of a 1.2V 10-bit 100MHz Pipelined ADC

To verify the proposed gain-compensation circuit, a 1.2 V, 10b, 100MHz reset-opamp pipelined ADC was designed (using a 0.18 μm CMOS process with V_{thn} = 0.49V and V_{thp} = - 0.48V) and simulated in transistor-level with BSIM3v3 model. With the traditional 1.5b/stage architecture, the pipelined ADC is implemented in a fully-differential architecture, using a low-voltage SC-CMFB technique [6]. In addition, the front-end Sample-and-Hold (S/H) utilizes a passive cross-coupled sampling circuit [7] to allow a passive interface to the input continuous time signal, eliminating the need for a T/R stage. The full scale differential input range is $1.2V_{PP}$ meaning that V_{ref} = 0.6V, and $C_{ref} : C_{f1} : C_{s1} = 1:2:4$ to realize the desired reference voltage injection and 2x MDAC gain as presented in (1), with the auxiliary amplifier capacitor ratios specified by (10). Only the 5 stages of the front-end MDACs have utilized the auxiliary amplifier to compensate the gain error, and the finite-gain error in the S/H will only imply an overall gain error of the ADC, which can be tolerated in most applications. All the auxiliary amplifiers use the A-DDA topology from Fig. 2a, and all the main amplifiers are current mirror opamps (with a structure similar to the circuit of Fig. 2a but with only one differential pair). The sampling capacitors as well as the opamps are scaled down along the pipelined stages to save power. Table I summarizes the simulated performance of the 1st stage MDAC opamps, with DC gains of 50 dB and 51 dB for the main and the auxiliary amplifiers only. For traditional designs without gain compensation, the required DC gain for the opamp in 1st MDAC would be at least 72 dB with β= 0.24 and a considerable margin should be added to ease the settling requirement. The total power consumption of the main and the auxiliary amplifier is only 12mW, which is comparable to state-of-the-art designs in higher supply voltage (e.g. V_{DD}=1.8V) with only the main opamps of similar GBW performance.

Fig. 3 shows the simulated DNL and INL of the ADC, with and without the auxiliary amplifier gain compensation. The IND/DNL simulation is obtained by traditional sine-wave histogram method. The gain-compensation circuit improved the DNL from +0.63/ -1 LSB (33 missing codes) to +0.56/-0.5 LSB and INL from +3.12/ -3.04 LSB to +1/-0.93 LSB, respectively. Fig. 4 shows the spectrum plots of the pipelined ADC with an input signal of 53.17 MHz and -1dBFS, and the SNDR has been improved from 46.77 dB to 58.51 dB, which clearly demonstrates the effectiveness of the proposed technique. Table II summarizes the overall performance of the pipelined ADC, with the one without compensation consuming 44 mW (since no auxiliary opamps are used) while the compensated ADC consumes only 68 mW.

V. Conclusions

A novel low-voltage finite-gain compensation technique has been proposed in this paper, which can be effectively applied in low-voltage high-speed reset- and switched-opamp circuits. Using an Auxiliary Differential-Difference Amplifier to sense and correct the finite-gain error of the main opamp, the proposed technique allows the use of high-speed single stage opamps in low-voltage environment, which can achieve higher bandwidth than the traditional widely used low-voltage two-stage amplifier. Simulated results of an 1.2V, 10b, 100MHz reset-opamp pipelined ADC are presented, with 1 LSB DNL (33 missing codes), 3.12 LSB INL and 46.77dB SNDR at a 53.17MHz input without gain compensation,

and 0.56 LSB DNL, 1 LSB INL, and 58.51dB SNDR with finite-gain error correction, showing the efficiency of such technique.

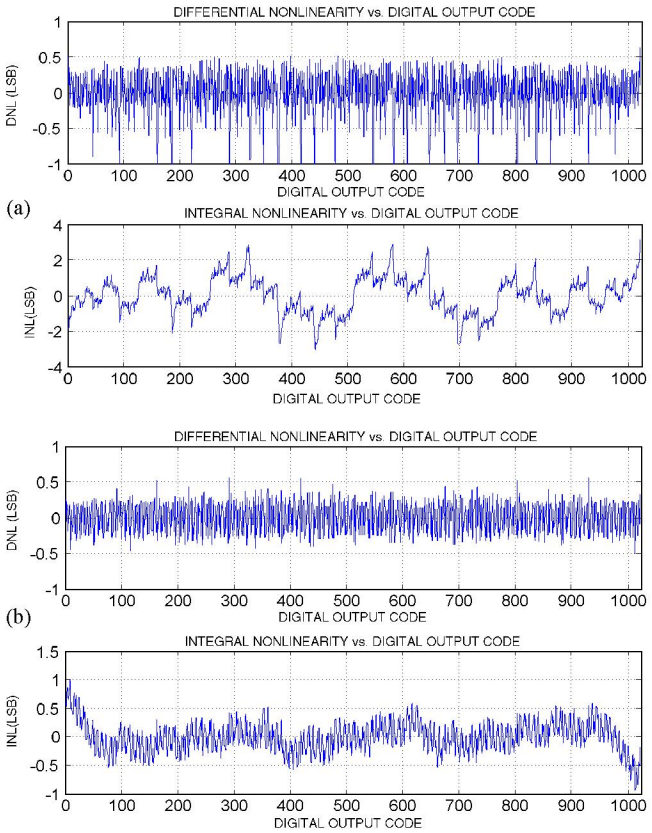

Fig. 3: Simulated INL and DNLL. (a) without gain-compensation; (b) with gain compensation.

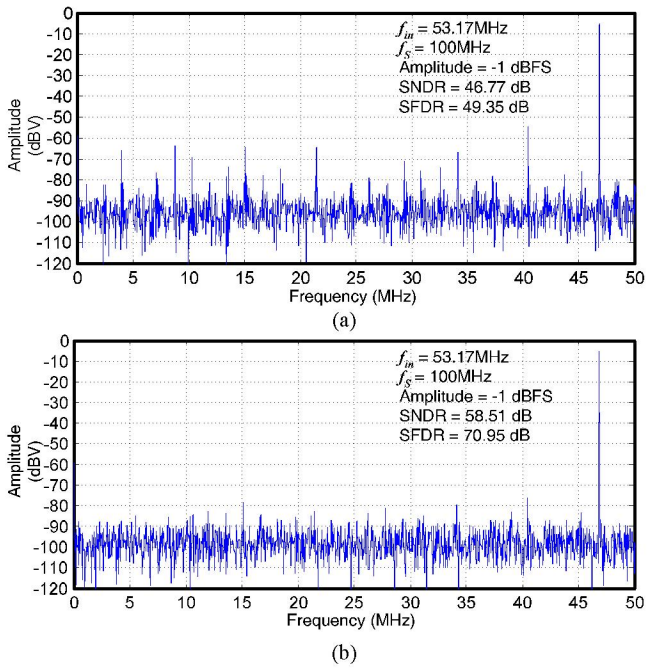

Fig. 4: Simulated FFT spectrum of the ADC. (a) without gain-compensation; (b) with gain compensation.

TABLE I. PERFORMANCE SUMMARY OF MAIN AND AUXILIARY AMPLIFIER IN 1ST STAGE MDAC

Performance	Main	Auxiliary
DC Gain	50 dB	51 dB
Feedback Factor β	0.24	
Unit-Gain Frequency	1.1GHz	640MHz
Phase Margin	79°	74°
Power Consumption (@ VDD=1.2V)	6.34mW	5.62mW

TABLE II. PERFORMANCE SUMMARY OF THE PIPELINED ADC

Performance	Without Compensation	With Compensation
Supply Voltage	1.2V	
Sampling Frequency	100 MS/s	
Full Scale Analog Input	1.2 Vpp differential	
DNL	+0.63/-1 LSB	+0.56/-0.5 LSB
INL	+3.12/-3.04 LSB	+1.0/-0.93 LSB
SNDR (@ fin=53.17 MHz)	46.77 dB	58.51 dB
SFDR (@ fin=53.17 MHz)	49.35 dB	70.95 dB
Power Consumption*	44 mW	68mW

* Excluding clock generator and biasing circuits

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REFERENCES

[1] Jen-Shiun Chiang and Ming-Da Chiang, "The design of a 1.5 V, 10-bit, 10 M samples/s low power pipelined analog-to-digital converter," in *Proc. of 2000 International Symposium on Circuits and Systems*, vol.1, pp. 443-446, May 2000.

[2] M.Waltari and K.A.I.Halonen, "1-V 9-bit pipelined switched-opamp ADC," *IEEE J. Solid-State Circuits*, vol.36, no.1, pp.129-134, Jan 2001.

[3] M. Keskin, U. Moon and G.C.Temes, "A 1-V 10-MHz clock-rate 13-bit CMOS ΔΣ modulator using unity-gain-reset op amps," *IEEE J. Solid-State Circuits*, vol.37, no.7, pp. 817-824, Jul 2002.

[4] V.S.L.Cheung, H.C.Luong and W.H.Ki, "A 1-V 10.7 MHz switched-opamp bandpass ΣΔ modulator using double-sampling finite-gain-compensation technique," *IEEE J. Solid-State Circuits*, vol.37, no.10, pp. 1215-1225, Oct 2002.

[5] D. Chang and U. Moon, "A 1.4-V 10-bit 25-MS/s pipelined ADC using opamp-reset switching technique," *IEEE J. Solid-State Circuits*, vol.38, no.8 pp. 1401- 1404, Aug 2003.

[6] Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "A novel very low-voltage SC-CMFB technique for fully-differential reset-opamp circuits," in Proc. of *2005 IEEE International Symposium on Circuits and Systems*, p. 1581-1584, May 2005.

[7] Sai-Weng Sin, Seng-Pan U, and R.P.Martins, "A novel low-voltage cross-coupled passive sampling branch for reset- and switched-opamp circuits," in Proc. of *2005 IEEE International Symposium on Circuits and Systems*, p. 1585-1588, May 2005.

[8] C.C. Enz and G.C.Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," in *Proc. of IEEE*, vol.84, no. 11, pp. 1584-1614, Nov 1996.

[9] Seng-Pan U, R.P.Martins and J.E.Franca, "Highly accurate mismatch-free SC delay circuits with reduced finite gain and offset sensitivity," in Proc. of *1999 IEEE International Symposium on Circuits and Systems*, vol. 2, p. 57-60, May 1999.

[10] H.Alzaher and M.Ismail, "A CMOS fully balanced differential difference amplifier and its applications," in *IEEE Trans. on Circuits and Systems II*, vol. 48, no. 6, pp. 614 – 620, Jun 2001.