Design and Test Strategy underlying a Low-Voltage Analog-Baseband IC for 802.11a/b/g WLAN SiP Receivers

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***Abstract* – The proliferation of multiple WLANs and the continuous scaling of CMOS have created the need for low-voltage multistandard WLAN receivers. Instead of approaching a complicated SoC, a 3D-stack SiP appears as a promising alternative to meet those requirements in conjunction with the obvious goals of low power and low cost. This paper, focused on the SiP implementation of a WLAN receiver, presents the design and test strategies underlying its analog-baseband portion to accomplish: low-voltage operation; 802.11a/b/g compliance; high routability in 3D stacking; and net-response testability of the functional blocks.**

I. Introduction

Cost minimization by means of a high-level of integration has been implemented through system-on-chip (SoC) and system-in-package (SiP) technologies. Entered in the nano-electronics era, the form of SoC is expected to deliver substantial improvements in cost, speed, power reduction, integration and density for digital circuits such as the microprocessors [1]. In sharp contrast, fabricating a mixed-signal SoC in nanoscale technologies is still in its infancy stage. One primary reason is a significant shrink of voltage headroom, which poses large constraints for analog and mixed-signal circuits design. Another reason is the multipurpose requirements of modern microsystems. Forming a new versatile SoC based on the existing SoCs requires a long design cycle to re-optimize the system performances and redo the fabrication. Besides, substrate crosstalk induced signal integrity will also obstruct the overall performance from reaching what their individuals can attain.

Alternatively, the 3D-stack SiP technology offers more flexibility. Dies fabricated in heterogeneous technologies and designed for different standards can be assembled as a multi-chip module (MCM) thought as a chip-to-chip interconnect inside a package, eliminating the substrate noise issue, saving lead time while reducing risk, and economizing on the increasingly costly mask sets required for manufacturing. Such a structure has demonstrated its effectiveness in the designs of memory and sensor designs [2], as well as in cellular transceivers [3].

This paper presents firstly the system design of the proposed low-voltage multistandard WLAN receiver in 3D-stack SiP. The simulation methodology, floor plan and test strategies exploited in its analog-baseband (BB) portion will follow, being decidedly different from other designs normally targeting on SoC and using a standard supply voltage, e.g. [4].

II. System Design

System Partition – The receiver architecture in 3D-stack SiP is shown in Fig. 1(a), and its corresponding block schematic is shown in Fig. 1(b). The system is pieced by heterogeneous best-fit technologies to compromise the form factor. High-frequency signals are kept on chip except those between the antenna and the radio chip. Since 802.11a, b and g are TDMA standards, the analog BB serves multiple standards through reconfiguration. The A/D interface (assuming 10-bit resolution) resides on the digital chip for 2 main reasons. First, a digital interface would require at least 20 more pins for communication between the two chips, as the receive chain generates in-phase (I) and quadrature (Q) signals. Second, the relatively large switching power in the A/D interface can induce substantial substrate noise that could disturb the receiver analog BB. The back-end chip includes the digital BB and MAC processor that are typically integrated on the same die [5]. For the power management unit, direct operation from a single low-voltage supply will ultimately yield the lowest possible power consumption, considering that DC-to-DC up/down converters consume significant amount of power (and area), and the leakage power mainly dominated by the quiescent and leakage currents in the nanoscale chips could be efficiently lowered by supply-voltage reduction.

Multistandard Compliance – Standard requirements constitute the basis for choosing the architecture. For the receiver (RX), 802.11b benefits from a zero-IF downconversion due to its spread-spectrum and wideband characteristics, the elimination of the DC offset by using a capacitive interconnect will not cause a heavy distortion as long as the frequency of the highpass pole is low enough, i.e., ~10 kHz. Conversely, although 802.11a and g are wideband, the OFDM technique will originate the removal of the problematic low-frequency noise. Without using an automatic frequency control, a slight frequency deviation in the frequency synthesizer (FS) will place the notch on the channel sub-carriers, rather than on the unwanted low-frequency disturbance area [6]. Such a problem can be facilitated by exploiting a low-IF approach with the selected IF equals to one-half of the channel spacing. Thus, the required image rejection can be relaxed due to the standard guideline, i.e., the image (1st adjacent channel) is maximally only 16 dB larger than the desired one. In addition, low IF allows the use of a more relaxed highpass pole (as high as 1.5 MHz) for the capacitive interconnect to meet the stringent response time required by 802.11a and g.

The proposed solution is a low-IF/zero-IF reconfigurable RX with a *two-step channel selection* [7], which not only synthesizes the beneficial features of low-IF and zero-IF, but also relaxes the FS's settling time and the local oscillator (LO)'s phase noise.

Multimode Analog BB – The analog BB is shown in Fig. 2. In RX mode, after amplification by the low-noise amplifier (LNA) and downconversion by the RF mixers, the signal will enter in the analog BB. The preselect filter and double-quadrature down-converter (DQDC) offer two modes: filtering and image-reject downconversion in low-IF mode (LIF), or simply channel-selection filtering with a halved bandwidth (BW) in zero-IF mode (ZIF). Thus, commonly used complex filters are unnecessary. The DQDC selects either the desired channel or its image (adjacent channel) to the BB, such that a *fine* channel selection is accomplished at the IF without using a secondary FS and LO. The radio FS is relaxed consequently to perform only *coarse* channel selection. The I/Q-modulation signals are generated precisely by

using quad series-switching (SS) mixers cooperating with a mixed-mode clock generator (CLKGEN). The lowpass filter (LPF) is BW-tunable for diverse channels, and the programmable-gain amplifier (PGA) allows the optimization of the signal swing. Several switchable DC-offset cancellation (DOC) loops are embedded in the LPF's and PGA's OpAmp to form a DOC scheme, through which the highpass poles are progressively switchable during preamble for fast settling [8]. The operation modes, channel selection, gain and bandwidth controls are implemented digitally.

Low-Voltage Implementation – Many BB blocks, such as amplifier, filter and IF mixer, can be built based on low-voltage inverting configurations. Figure 3 shows the proposed 8 functions. No input swing is required from the OpAmp while rail-to-rail output swing is deliverable. The DC level of the virtual ground is biased close to the ground rail for a NMOS switch to gain an enough overdrive voltage. All functions are super-positioned together to form multifunctional blocks with a single OpAmp. Those techniques were adopted in the design of a 1V PGA using a 3.3V 0.35μm CMOS process [8].

III. Simulation Methodology

The simulation methodology is summarized in Fig. 4. The abstract-level simulation was done in *MatLab/Simulink* with the provided toolboxes. Results from the models were translated to circuit-level specifications such as the *I/Q* mismatch, filter order, 3rd-order intercept point (IP3) and noise figure (NF), etc. The circuit-to-transistor-level designs were carried with *Cadence Composer*. DC operating points (e.g., input and output common modes) had been set before circuit architectures were chosen, on the ground that MOS differential pair and analog switches only work on the DC level closes to either one of the supply rails. Hardware breakpoints were assigned for measuring the functional blocks net responses. All the analog cells were full-custom optimized through *Cadence Parametric Analysis* and *Optimizer*, whereas the digital cells were based on standard cells with scaled-up physical sizes to compensate the increased delay of low-voltage operation (gate delay $\propto$ 1/supply). Constraint-driven optimization reduced the number of iterations in the design of paramount analog cells such as the OpAmp. The first verifications of analog and digital blocks were done in *Spectre* progressively from static (DC and AC) to dynamic (transient). The IF mixer was simulated after the other cells were completed since its switching behavior was the origin of substrate noise, as well as time-consuming in simulation. Iteration between the simulation and design stages continued, dependent upon system performance.

Layouts were completed in *Virtuoso*. The floor plan and pin assignments insured testability in verification and routability in 3D-stack SiP integration (more details in Section IV). DRC, LVS, density coverage, antenna effect cleared layouts were extracted to get the ubiquitous parasitic. Imbalanced parasitic at important nodes (e.g., OpAmp inputs) were equalized by repeating the processes of backannotation and extraction. Top-cell verifications in low-IF and zero-IF modes were executed separately in different workstations to save the simulation time and facilitate debugging. The effect of ground bounce was simulated (in transient) with the package model included in all I/Os, and with the multiple MOS capacitors connected between the ground and the AVDD, DVDD and common-mode voltages. Those MOS capacitors were used to determine the minimum amount of decoupling capacitance required for the supply noise to be neglectable.

Deliberately setting the input waveform and changing the circuit status speeded up the top-cell verification. For instances, DC, AC and noise analysis run in parallel involving only one-time netlisting and DC analysis, but determining the static behaviors simultaneously. Whereas a liberal transient simulation, with an input level that could get the largest output swing, and with the largest gain step applied in between, exhibits the worst measured settling time and overshoot. Monte-Carlo simulations (DC, AC and selected transient) were executed iteratively before tapout.

IV. 3D-Stack Considerations and Test Strategies

3D Floorplan – 3D stacking of multiple chips requires 3D floorplan to insure routability. Fig. 5(a) and (b) show, respectively, that the proposed 3D floor-plan can be optimized not only in the proposed transceiver in RX modes, but also in the transmitter (TX) mode (comprising 3 chips in each path, radio, analog BB and digital BB) for future full integration of the transceiver system. Without any cross bonding between chips, the analog BB chip bridges the radio to the digital BB one without complicated routings.

I/O Setup – Chip-to-chip bonding requires the concern of I/Os since each chip has ESD protection and may use different voltage levels in their pad rings. For instance, the inductance of the bondwire and the parasitic capacitance associated with the pads that will limit the bandwidth, and the potential difference of the pad rings that will limit both the common-mode voltage and signal swing. In the analog BB chip implementation, standard pads were employed since only low-frequency signals were transferred in and out the BB chip. The bypass settings in the 3.3V I/Os are shown in Fig. 6(a) and (b), respectively. Placing the switches after the resistor ensured high linearity and low-voltage workability. Two single-ended test buffers (BUFs) were employed for the differential outputs [Fig. 6(b)]. Inserting an inverter in the current mirror, the BUF can be switched off (on) with its gate voltage equal to 3.3V (bias voltage driven by current source I_b).

Although the pad-ring upper and lower voltage limits are set to 0V and 3.3V, respectively, simulation results showed that a THD <0.03% is achieved with a $1.2V_{pp}$ input at 0.1V DC level (Fig. 7). This implies that the signal swing can go beyond the pad-ring limits by a voltage level close to the forward-bias voltage of the protection diodes. Thus, unmatched pad-rings pose insignificant limits to chip-to-chip interconnect.

Testing Board – The chips for SiP integration must be individually verifiable while matching also the floor plan needed in the final 3D-stack SiP integration. Shown in Fig. 8 is the EMI-aware evaluation board for testing the overall and the functional-block net responses of the analog BB chip that was fabricated in a 0.35μm 4M2P 3.3V CMOS process. Decoupled voltage sources and regulated currents were used to breed the chip. The parts were placed in star connection with curved rout-and-connect to minimize EMI. The I/O networks are transformers and impedance matching parts for driving the 50-Ω testing ports. The on-chip switches are operated in the current mode, whereas those that are off-chip are jumpers.

Measurement – The experiment was conducted with in-house instruments as shown in Fig. 9. Based on the measurement procedures described in Fig. 10 and Table 1, the noise and gain (conversion gain for the IF mixers) responses of the functional blocks were obtained with only two sets of BUFs. The measured cases {1}-{3} examined the net responses of the I/O networks, whereas the {4}-{7} determined the responses of the chip in four different conditions: the pre-filter plus DQDC and LPF, the preselect filter plus LPF, the PGA and the overall. After simple

operations, the net responses of the functional blocks [{10}-{12}], and the overall responses in RX [{13}, {14}] were obtained, independent of the I/Os and BUFs. Fig. 11 (a) and (b) show the measured responses of the PGA and of the preselect filter with LPF, respectively, by using such a procedure.

V. Conclusions

The design and test techniques reinforced in a low-voltage WLAN SiP receiver were presented. Carefully partitioning the transceiver into multiple subsystems allowed the use of nanoscale technologies for digital chips, while the analog chips could be preserved at their best-fit technologies to facilitate the overall design and minimize cost. The analog baseband presented is the effectual cornerstone of building such a system. Right inserting the design techniques for low voltage, low power, low cost, 802.11a/b/g compliance, routability and testability in the design flow smoothed the progress at each stage, and produced the measured results on first silicon consistent to the simulation.

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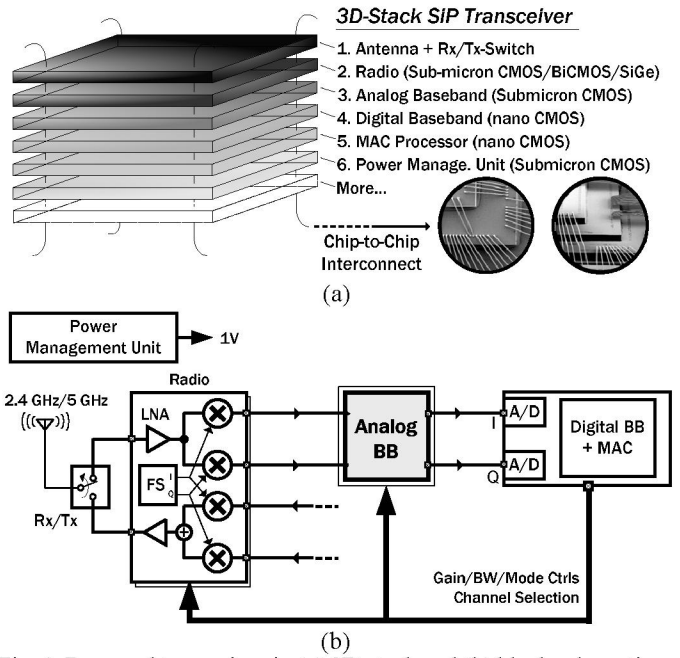


Fig. 1. Proposed transceiver in (a) 3D-stack and (b) block schematic.

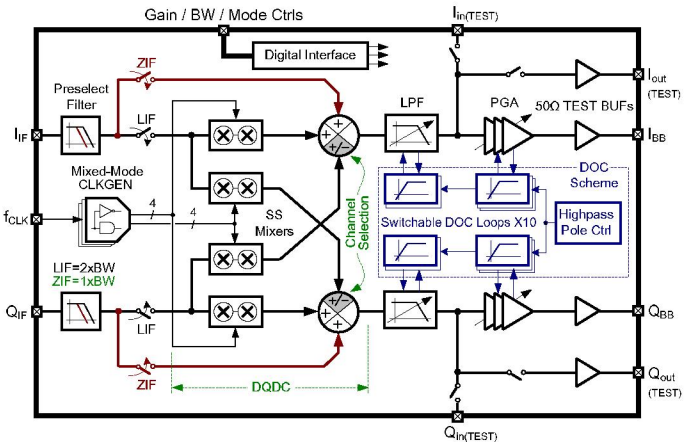


Fig. 2. Block schematic of the analog BB.

References

[1] S. Chou, "Integration and Innovation in the Nanoelectronics Era," in *IEEE ISSCC, Digest.*, pp.36-41, Feb. 2005.

[2] Nicky C. C. Lu, "Emerging Technology and Business Solutions for System Chips," in *IEEE ISSCC, Digest.*, pp.25-31, Feb. 2004.

[3] G. Uvieghara, *et al.*, "A Highly-Integrated 3G CDMA2000 1X Cellular Baseband Chip with GSM/AMPS/GPS/Bluetooth/ Multimedia Capabilities and ZIF RF Support," in *IEEE ISSCC, Digest.*, pp.422-423, Feb. 2004.

[4] Z. Xu, *et al.*, "A Compact Dual-Band Direct-Conversion CMOS Transceiver for 802.11a/b/g WLAN," in *IEEE ISSCC, Digest.*, pp.98-99, Feb. 2005.

[5] M. Bhardwaj, *et al.*, "A 180MS/s 162Mb/s Wideband Three-Channel Baseband and MAC Processor for 802.11a/b/g," in *IEEE ISSCC, Digest.*, pp.454-455, Feb. 2005.

[6] A. Behzad, "Wireless LAN Radio Design," presented in *IEEE ISSCC, Tutorial T2*, Feb. 2004.

[7] P.-I. Mak *et al.*, "Two-Step Channel Selection – A Novel Technique for Reconfigurable Multistandard Transceiver Front-Ends," *IEEE Trans. on CAS-I, Regular Paper*, vol. 52, No. 7, pp. 1302-1315, Jul. 2005.

[8] P.-I. Mak *et al.*, "A 1-V Transient-Free and DC-Offset-Canceled PGA with a 17.1-MHz Constant Bandwidth over 52-dB Control Range in 0.35-µm CMOS," in *Proc. of IEEE CICC*, pp. 649-652, Sept. 2005.

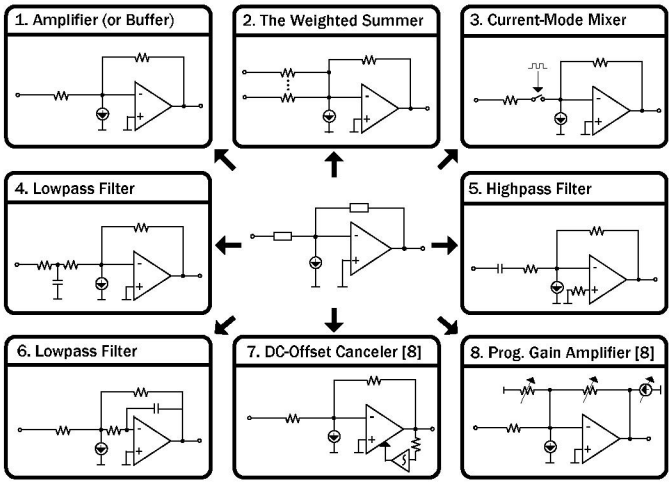


Fig. 3. BB functions based on OpAmp in inverting configurations.

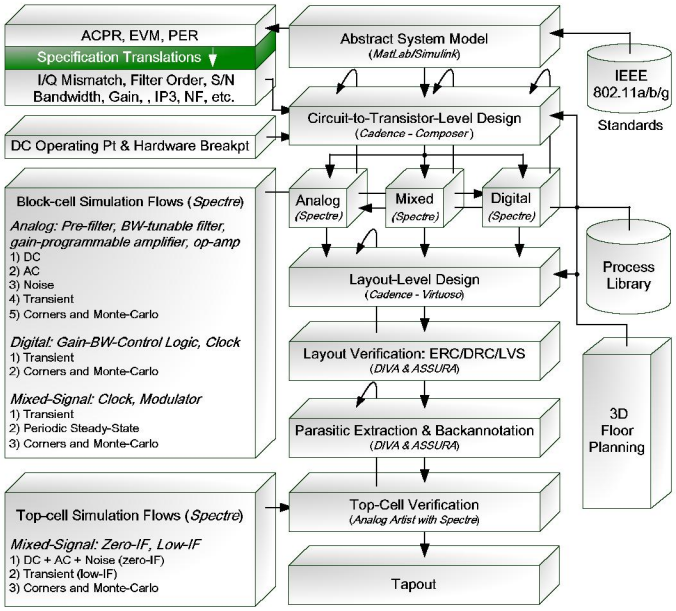
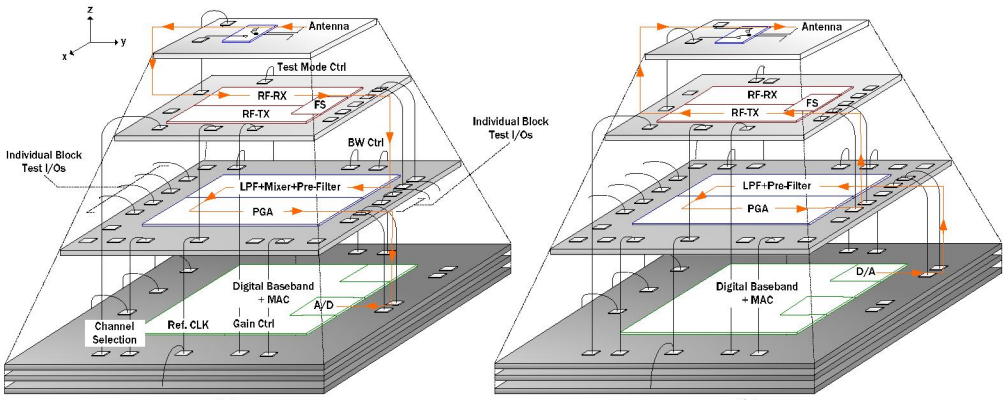


Fig. 4. Simulation methodology.



(a) (b)

Fig. 5. Simplified 3D floor plan and pin assignments. (a) RX. (b) TX.

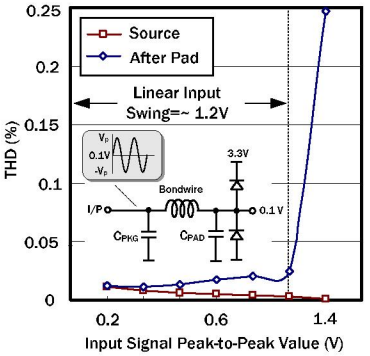
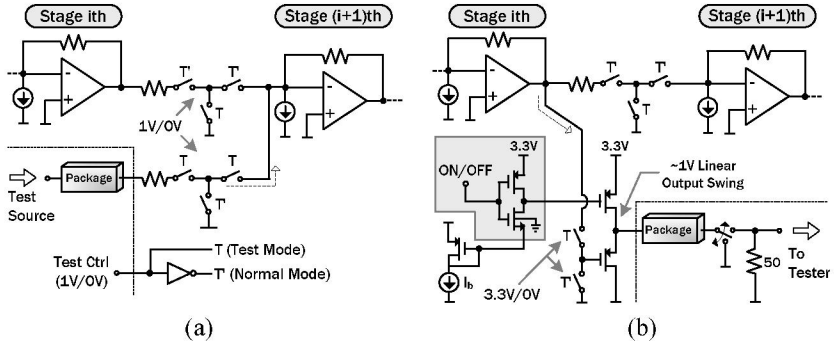


Fig. 7. Package linearity to input swing at 0.1V DC level.



(a) (b)

Fig. 6. I/O setup for (a) test-source injection and (b) response measurement.

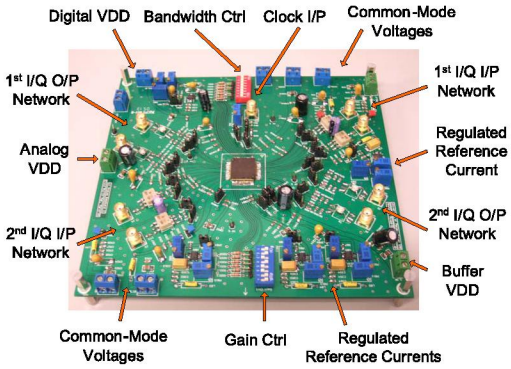


Fig. 8. Evaluation board for high testability.

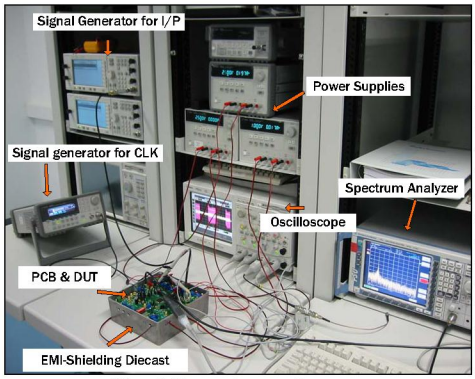


Fig. 9 Experimental setup.

Measured Cases		Off-Chip Switches					On-Chip Switches			
		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
$H_{I/P,1}(f) \cdot H_{O/P,2}(f)$	{1}	ON								
$H_{I/P,1}(f) \cdot H_{O/P,1}(f)$	{2}				ON					
$H_{I/P,2}(f) \cdot H_{O/P,2}(f)$	{3}					ON				
$H_{I/P,1}(f) \cdot H_{PF}(f) \cdot H_M(f) \cdot H_F(f) \cdot H_{B,1}(f) \cdot H_{O/P,1}(f)$	{4}			ON				ON		
$H_{I/P,1}(f) \cdot H_{PF}(f) \cdot H_F(f) \cdot H_{B,1}(f) \cdot H_{O/P,1}(f)$	{5}			ON				ON		ON
$H_{I/P,2}(f) \cdot H_P(f) \cdot H_{B,2}(f) \cdot H_{O/P,2}(f)$	{6}		ON				ON			
$H_{I/P,1}(f) \cdot H_{PF}(f) \cdot H_D(f) \cdot H_F(f) \cdot H_P(f) \cdot H_{B,2}(f) \cdot H_{O/P,2}(f)$	{7}		ON	ON					ON	

Operations				Net Responses	
{2} / {1}	→ get	$H_{O/P,1}(f) / H_{O/P,2}(f)$	{8}	Output-Network Ratio	
{3} / {1}		$H_{I/P,2}(f) / H_{I/P,1}(f)$	{9}	Input-Network Ratio	
{4} / {5}		$H_D(f)$	{10}	DQDC	
{9} · {7} / ({6} · {10})		$H_{PF}(f) \cdot H_F(f)$	{11}	Preselect Filter + LPF	
{8} · {7} / {4}		$H_P(f)$	{12}	PGA	[Assume $H_{B,1}(f)=H_{B,2}(f)$]
{10} · {11} · {12}		$H_{PF}(f) \cdot H_D(f) \cdot H_F(f) \cdot H_P(f)$	{13}	Preselect Filter + DQDC + LPF + PGA	[Low-IF Modes]
{11} · {12}		$H_{PF}(f) \cdot H_F(f) \cdot H_P(f)$	{14}	Preselect Filter + LPF + PGA	[Zero-IF Mode]

Table 1. Test procedure corresponds to Fig. 10.

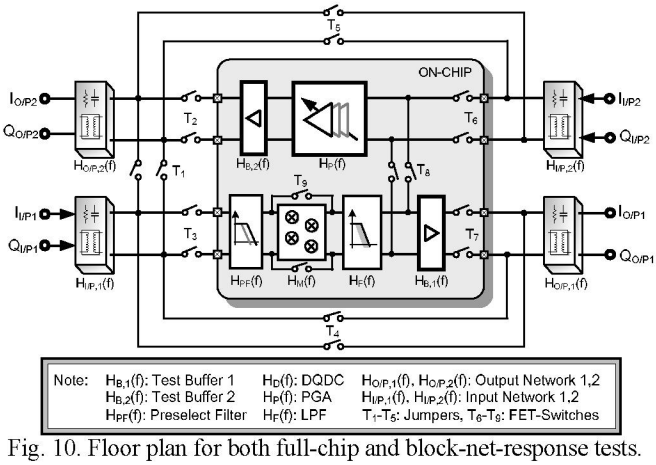
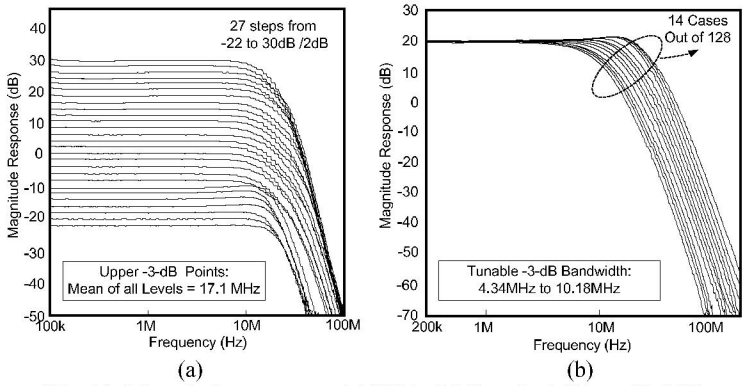


Fig. 10. Floor plan for both full-chip and block-net-response tests.



(a) (b)

Fig. 11. Magnitude responses. (a) PGA. (b) Preselect filter with LPF