A Dual-Mode Low-Distortion Sigma-Delta Modulator with Relaxing Comparator Accuracy

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Abstract **– A dual-mode single-loop multi-bit (3 bits) sigma-delta modulator (SDM) with reduced number of op-amps is proposed for satisfying the GSM/WCDMA standard. Such architecture is based in a simplified analog structure that not only features low distortion but also provides an aggressive and significantly enlarged noise shaping bandwidth with low over-sampling ratio (OSR). In addition, the resolution of comparators in the quantizer is relaxed to reduce the power consumption. Simulations in system- and transistor-level simulations prove a dynamic range of 88dB & 60dB in GSM & WCDMA respectively.**

I. INTRODUCTION

The major focus of modern RF receivers IC design has been on the increase of the adaptability and integration of multi-standard communication standards. Delta-Sigma Modulator has been one of the preferred solutions for integrated wireless applications since they provide some of the desired trade-offs between power consumption, over-sampling ratio (OSR) and dynamic range (SNR). Moreover, it provides the flexibility to satisfy the demanding performance for multi-standard applications by changing the order and the OSR of the delta-sigma ADC.

The stringent setting requirements of the analog building block especially the first integrator limit the performance and power consumption. Low-Distortion topology [1~2] can be used to relax the circuit imperfection that caused by nonlinear opamp gain and limited slew-rate. On the other hand, the passive summation network [1] is usually the preferred solution for implementation of the summation node. However, it increases the demanded performance of the quantizer. The SDM proposed in this paper relaxed the quantizer requirement. With flexibility in changing the order and OSR, it exhibits high-speed and low distortion, containing a high dynamic range performance that suitable for GSM or WCDMA applications. In section 2, the circuit architecture will be described, followed by its integrated circuit implementation on section 3. Section 4 will present the results of the simulation and finally in Section 5 the conclusions will be drawn.

II. SYSTEM ARCHITECTURE

A. Dual-Mode Adaptability

According with the requirements of GSM/WCDMA communication standards, different circuit topologies have been proposed [3-5] that are able to achieve an adequate performance. Figure 1a) and 1b) show the proposed architecture for WCDMA and GSM mode respectively and the corresponding transfer function given by equation (1) and (2). Low-Distortion topology has been employed to relax the op-amp specification. The order of the circuit change from 3rd and 2nd by disable the part of the feedforward signal path in the second integrator. It provides the flexibility for system level design. It is well suitable for power optimization under different communication standards.

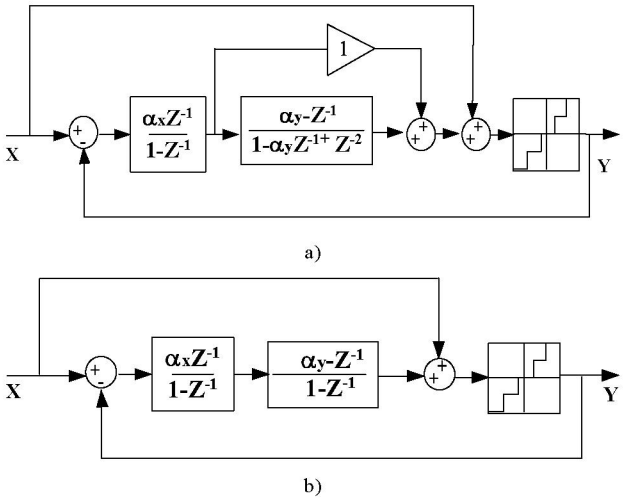

Figure 1: Proposed SDM architecture a) WCDMA mode b) GSM mode

WCDMA mode: STF = 1

$$NTF = \frac{(1-Z^{-1})(1-\alpha_y Z^{-1}+Z^{-2})}{1+(\alpha_x-1)Z^{-1}[(\alpha_y+1)-(\alpha_y+1)Z^{-1}+Z^{-2})]} \quad (1)$$

GSM mode: STF = 1

$$NTF = \frac{(1-Z^{-1})(1-\alpha_y Z^{-1}+Z^{-2})}{1+(\alpha_x\alpha_y-2)Z^{-1}+(1-\alpha_x)Z^{-2}} \quad (2)$$

B. Passive Sampling Summation Node

Active integrator can be used to implement the summation node [5]. Although the requirement of this amplifier can be relaxed by noise shaping, it also consumes an amount of the power and area. Hence, the passive summation network is chosen [6], as shown in figure 2 where a two-phase nonoverlapping clock is assumed. Such passive sampling network entails a factor of 3 drops in quantizer's input signal S(z). In order to maintain the same performance of the SDM, the reference voltage Vref must be scaled down from its nominal value. However, this is also scaled down (by the same factor) in the amount of the quantizer's step size and hence a comparator with higher resolution will be required. This implies the increase of quantizer's power consumption.

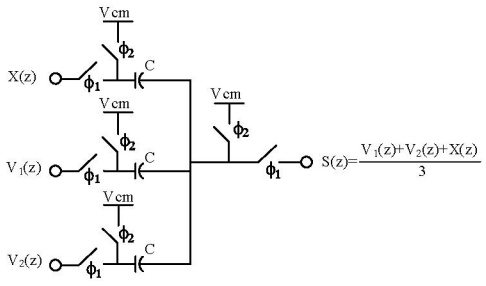

Figure 2: Switched Capacitor Passive Summation network

In multi-level quantization, the power consumption of the quantizer is also an important factor especially in high-speed applications. In principal, when the signal before the quantizer is scaled down by a factor, the gain of the first integrator can be increased to compensate the signal loss. In the proposed circuit, the first integrator gain can be increased by 3 to fully compensate the signal scaling. However, the saturation level of the integrator will limit the range of the integrator gain. Figure 3 shows the simulation results for the proposed circuit in WCDMA mode under various gains of the first integrator. It also shows that the gain cannot be changed arbitrarily otherwise the SNR will drop due to the saturation of the integrator. To obtain a trade-off between signal scaling and the achieved SNDR, the gain of the first integrator will be increased by 1.5 in the proposed circuit. Hence, the resolution of the quantizer will only be increased by two instead of three. With OSR=8/64, 3bits quantizer and setting α_y = 1.9 and α_x = 1, the system level simulation results show that the proposed structure achieves maximum SNDR of 60dB and 90dB with WCDMA and GSM modes respectively.

C. Switched – Capacitor (SC) Circuit

A fully differential switched-capacitor (SC) integrator is used in the proposed SDM. The first integrator is similar to a conventional SC integrator with multi-bit feedback. Due to the low distortion topology, the analogy requirements of the first op-amp such as the DC gain, GBW and SR can be relaxed. The second integrator and the corresponding timing diagram are shown in Figure 4. This second order integrator is implemented with a single op-amp [2]. Although the extra circuitry increases the capacitive loading, the noise shaping of the second integrator can relax the nonlinearity. In order to allow multi-standard operation, switch WC is added. When the switch WC is disabled, the extra circuitry is disable and the system changed from 2nd to 1st order. Under GSM mode, 2nd order SDM is enough to achieve the requirement. The proposed circuit is suitable for power optimization when system operates in different communication modes.

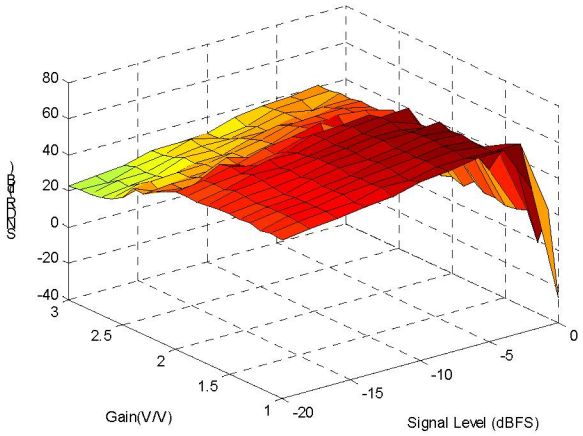

Figure 3: SNDR versus input amplitude

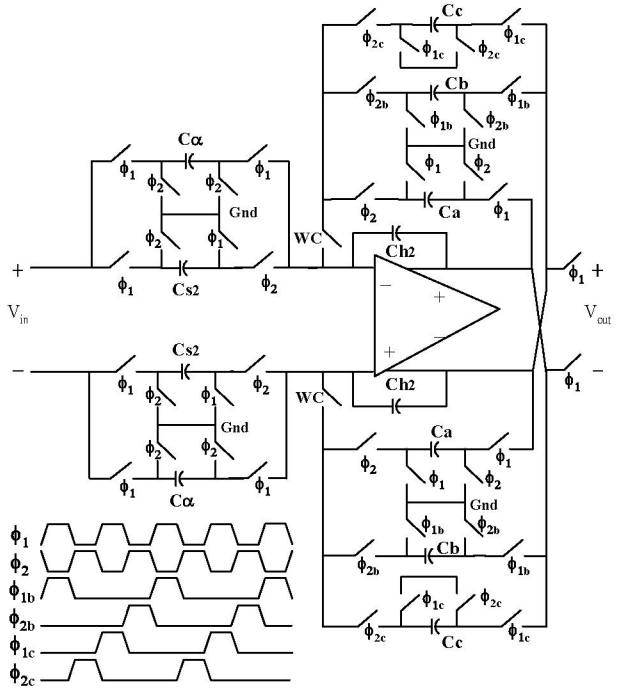

Figure 4: SNDR versus input amplitude.

III. CIRCUIT LEVEL IMPLEMENTATION

Op-amp is the dominant part of the SDM especially in the first integrator. A 2-stage OTA with rail-to-rail output is required to optimize the output swing. The supply voltage is 1.8 V and the process technology is 0.18μm. To further optimize the power consumption, a class AB push-pull second stage is used to allow a low static current and achieve high slew rate. A fully-differential 2-stage OTA with 70dB gain and 120MHz unity-gain bandwidth (GBW) was designed, with Miller compensation and the architecture is shown in Figure 5. In addition, figure 6 shows the 1-bit fully-differential comparators with 32mV of resolution that were designed to implement the 3-bits quantizer [7]. Moreover, in order to shape the DAC nonlinearity caused by mismatch of the feedback capacitor, a Pesudo Data Weighted Averaging (PDWA) technique [6] has been used.

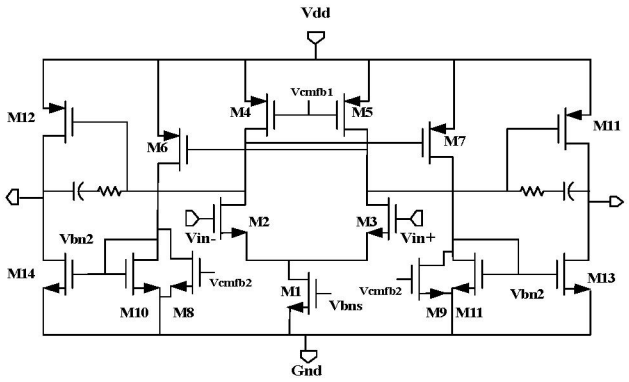

Figure 5: A 2-stage fully-differential Class AB OTA.

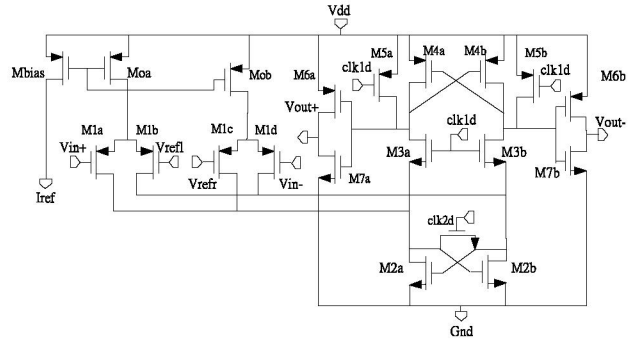

Figure 6: The comparator circuit schematic.

IV SIMULATION RESULTS

The behavioral simulation of the proposed SDM from Figure 8 was performed with the circuit parameters mentioned previously and with a sampling frequency of 32MHz with an OSR=8 for WCDMA. Each sampling capacitor has a value of 2.1pF in the first integrator and 1.4pF for the integrating capacitor. The variation of the design parameter α_y due to process variations will affect the overall circuit performance. Figure 7 shows the output spectrum for an input signal frequency of 0.5MHz with $0.6V_{pp}$. The achieved SNDR/SFDR are 60dB/69dB, respectively. The mismatch of the unit elements has also been analyzed by using a Gaussian distribution with a mean equal to the nominal value and standard derivation corresponding to the requirement of the accuracy. Figure 9 shows the statistical histogram of the 300-run simulation for SNDR with 7-bits accuracy for capacitance. Besides, the SDM achieves 88dB SNDR with fs=12.8MHz and OSR=64 for GSM MODE. In addition, the results satisfy the ADC requirement for WCDMA and GSM. 7-bits accuracy for the feedback capacitor ratio is required without significantly degrading the performance. Besides, a comparison of the existing SDMs for WCDMA and GSM with the novel proposed architecture is provided in Table 1, where it is shown that the proposed architecture obtains similar levels of accuracy when compared with others but with a simplified architecture.

V CONCLUSIONS

This paper has proposed a novel programmable low-distortion and opamp-reduced wideband multi-level SDM. Simulation results have shown that the proposed SDM is particularly adequate for dual-mode applications such as WCDMA and GSM. Moreover, the architecture can be extended to higher order to increase the SNDR for wider signal bandwidth. Comparing the proposed SDM with existing topologies targeted for dual-band, the proposed modulator not only reduces the number of opamps, relaxing the effect caused by the passive summation nodes but also satisfies more demanding communication standards with higher performance showing that this architecture is well-suited for low-power applications. Besides, chip area will also decrease with the reduction of the number of opamps.

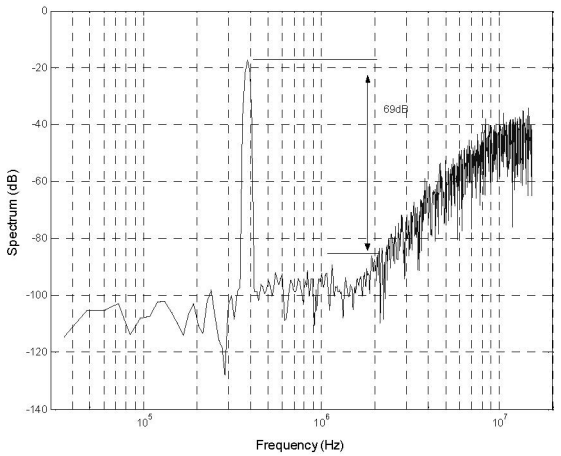

Figure 7: SNR vs DAC linearity for OSR = 8.

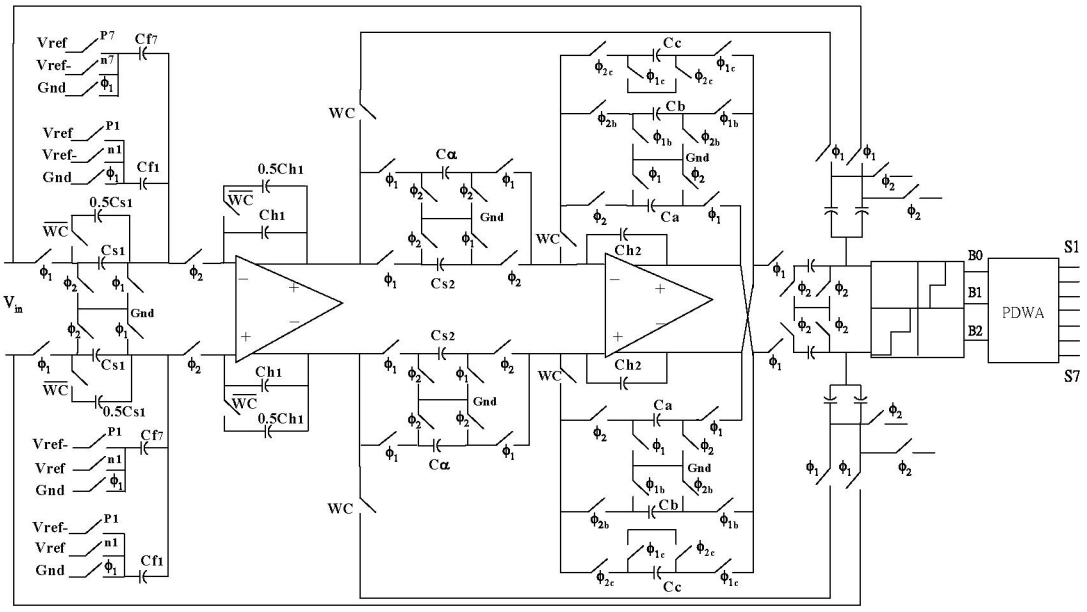

Figure 8: Circuit implementation of the proposed SDM.

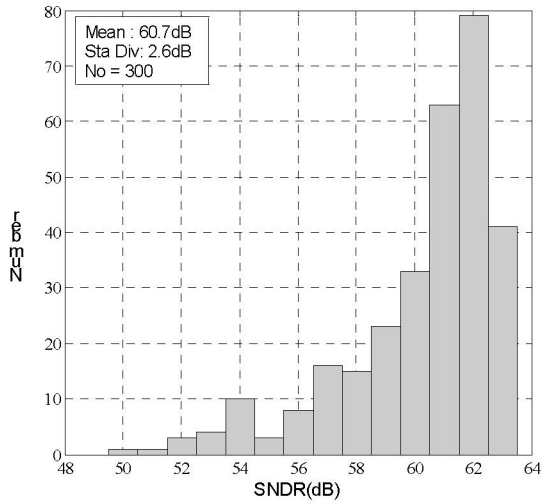

Figure 9: Histogram of 300-run Monte-Carlo simulation with capacitance variation for SNDR.

Table 1: Comparison among different Sigma Delta Modulators. (Ci-jBm: cascaded i-j converter where m denotes the number of bits in the quantizers. SnBm denotes n^{th}-order SDM with a m-bit quantizer.)

Refs	[3]	[4]	[5]	Proposed
OSR	10/195	12/65	8/156	8/64
Topology	C21B5	C20B2.3	C23B4	C20B3
Bandwidth (MHz)	1.92/0.1	2/0.1	1.92 /0.1	1.92/0.1
SNDR (dB)	64/81	50/79	72/82	60/88
Quantizer	5bits	2.3bits	4bits	3bits

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