A Novel Effective Bandpass Semi-MASH Sigma-Delta Modulator with Double-Sampling Mismatch-Free Resonator

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***Abstract*—This paper presents a novel high-order bandpass semi-MASH sigma-delta modulator (4-2+2-…-2+2mb) with $f_s/4$ center frequency. The proposed topology employs a semi-MASH technique with a 4-2^{L}mb topology to achieve an expandable and extendable high-order bandpass noise-shaping. To illustrate the novel architecture's behavior an 8xOSR 12-order 1.5-bit semi-MASH sigma-delta modulator is designed achieving 88 dB SNQR (signal-to-quantization-error ratio) at -1dB overloading point (90% of the modulator full-scale). A double-sampling mismatch-free single-opamp double-delay resonator is also proposed for the semi-MASH sub-stages to improve the overall design performance.**

I. Introduction

In modern wireless communication applications, the support of multiple operation modes represents usually a trend to obtain the success of a product. The adoption of multi-standards implies different types of modulation and channel bandwidths leading to highly flexible implementations. If signal digitization occurs in the baseband the analog circuitry complexity is higher with an important impact in the final cost. However, if the signal could be digitized closer to the antenna, then the multi-standard functionality including demodulation and channel-selection would be performed in the digital domain [1-6]. An optimum solution to fulfill this objective, at an intermediate-frequency (IF), implies digitizing the analog signal through a bandpass sigma-delta modulator, which will exhibit higher performance when compared with wideband Nyquist-rate ADCs. Since traditionally the bandwidth of IF signals is much smaller than the carrier frequency the bandpass sigma-delta modulator is an efficient architecture for such type of applications which benefits from its oversampling characteristic to achieve a high signal-to-noise-ratio [7]. But when the signal bandwidth increases, and for a fixed carrier frequency, the OSR value must be reduced which turns oversampling less attractive. Thus for wider bandwidth applications, high-order multi-bit sigma-delta modulators are naturally the best choice for an optimum system solution. MASH-type sigma-delta modulators such as 4-4^{L}mb and 4-2^{L}mb are usually utilized for the implementation of high-order noise-shaping modulators.. Recent trends of sigma-delta modulator research include the maximization of the SNQR through the spreading of NTF zero while achieving expandable architecture and minimizing the overloading point [8]. By exploring different trade-offs between these two topologies a semi-MASH sigma-delta modulator, recently proposed [9], can achieve a high-order expandable and extendable noise-shaping characteristic. The main idea behind this new architecture is the creation of a feedback path between the cascade modulator stages to obtain an aggressive noise-shaping with a minimum overloading region. In this paper, the semi-MASH technique is further enhanced and applied to bandpass sigma-delta modulation. In section II, the proposed bandpass semi-MASH architecture is thoroughly studied and a design example is presented to illustrate its behavior and compare it with different existing topologies. In section III a novel double-sampling mismatch-free technique will be proposed and explored for future application in the bandpass sigma-delta modulator. Finally, the conclusions will be drawn in section IV.

II. Architecture Study

The block diagram of the proposed expandable and extendable high-order bandpass semi-MASH sigma-delta modulator is shown in Figure 1 including the gains associated to different blocks. It is a combination of a bandpass version of 2-1^{L}mb [9] and semi-MASH technique. The analog part comprises a 4th-order bandpass sigma-delta modulator as the first stage followed by a chain of semi-MASH sub-stages. The first stage quantization gain is 4 to reduce the internal resonator swing and its noise transfer function (NTF) has two zeros at $f_s/4$. On the other hand, its quantizer error will be attenuated by a factor of 2 and also asymmetric coupling will be provide to the subsequent stage in order to minimize the overload region, introducing a systematic loss of 2, i.e., 1-bit loss into the overall noise attenuation. Each semi-MASH sub-stage consists of two 2nd-order bandpass sigma-delta modulators with a feedback sum in between. A quantization gain of 2 is introduced in each modulator to reduce the internal resonator swing.

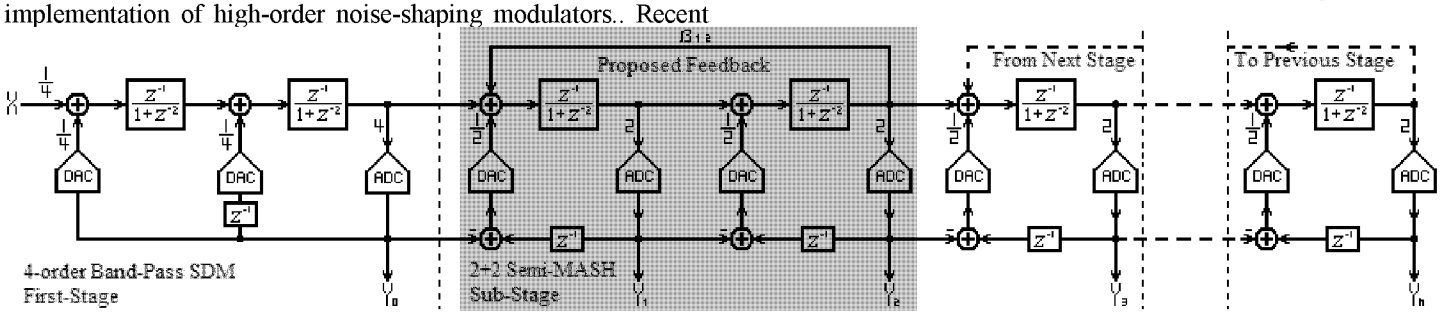

Figure 1. Generic (4+2×n)-th-order bandpass semi-MASH sigma-delta modulator with 4-2+2-…-2+2mb topology

$$Y = \sum_{0}^{n}(H_i \times Y_i) = X \times STF + E_n \times 2 \times NTF_n \cdots \quad (1)$$

$$STF = z^{-n} \cdots (2)$$

$$NTF_n\big|_{odd} = (1+z^{-2})^3 \times \prod_{1}^{(n-1)/2}(1+(2-\beta_{(2i-1)2i})z^{-2}+z^{-4}) \cdots (3)$$

$$NTF_n\big|_{even} = (1+z^{-2})^2 \times \prod_{1}^{n/2}(1+(2-\beta_{(2i-1)2i})z^{-2}+z^{-4}) \cdots (4)$$

$$H_0 = z^{-n} \times (1+(1+z^{-2})^2) \cdots (5)$$

$$H_i\big|_{even} = 2 \times z^{-(n-i)} \times (1+z^{-2})^2 \times (1+(1-\beta_{(n-1)n})z^{-2}) \times \prod_{1}^{i/2-1}(1+(2-\beta_{(2i-1)2i})z^{-2}+z^{-4}) \cdots (6)$$

$$H_i\big|_{odd} = 2 \times z^{-(n-i)} \times (1+z^{-2})^2 \times \prod_{1}^{(i-1)/2}(1+(2-\beta_{(2i-1)2i})z^{-2}+z^{-4}) \cdots (7)$$

$$f\theta_i = 0.25\,fs \pm \frac{fs}{4\pi}\cos^{-1}\left(1-\frac{\beta_{(2i-1)2i}}{2}\right) \cdots (8)$$

In the proposed architecture, the feedback within the sub-stage can spread the two NTF zeros away from *fs/4* though appropriate control and using the adequate error cancellation logic. If perfect cancellation occurs, the signal (STF) and noise (NTF) transfer functions of the proposed semi-MASH can be obtained as presented from (1) ~ (4), where the digital cancellation logic, used to eliminate the internal quantizer error can be expressed by (5) ~ (7). The location of the NTF zero location is given by (8) and if n is odd, one additional NTF zero occurs at *fs/4* as express in (3).

Based on the above architecture and corresponding equations an 8xOSR 12th-order (4+2×4) 1.5-bit band-pass semi-MASH sigma-delta modulator has been designed to demonstrate the superior behavior of the proposed structure. The digital cancellation logic can be obtained from the expressions (9) ~ (13). Figure 2 shows the SNQR versus feedback factors β weights (β_{12} and β_{34}) for -1 dBFS input signal level. To maximize the SNQR and minimize the coefficient spread, a gain weight of 1/9 is selected for both β_{12} and β_{34}. Totally 6 NTF zeroes (3 double-zeros) will exist which are located at [0.25-0.0267, 0.25, 0.25+0.0267]×*fs*.

$$H_0 = z^{-4} \times (1+(1+z^{-2})^2) \cdots (9) \qquad H_1 = 2 \times z^{-3} \times (1+z^{-2})^2 \cdots (10)$$

$$H_2 = 2 \times z^{-2} \times (1+z^{-2})^2 \times (1+(1-\beta_{12})z^{-2}) \cdots (11)$$

$$H_3 = 2 \times z^{-1} \times (1+z^{-2})^2 \times (1+(2-\beta_{12})z^{-2}+z^{-4}) \cdots (12)$$

$$H_4 = 2 \times (1+(1-\beta_{34})z^{-2}) \times (1+(2-\beta_{12})z^{-2}+z^{-4}) \times (1+z^{-2})^2 \cdots (13)$$

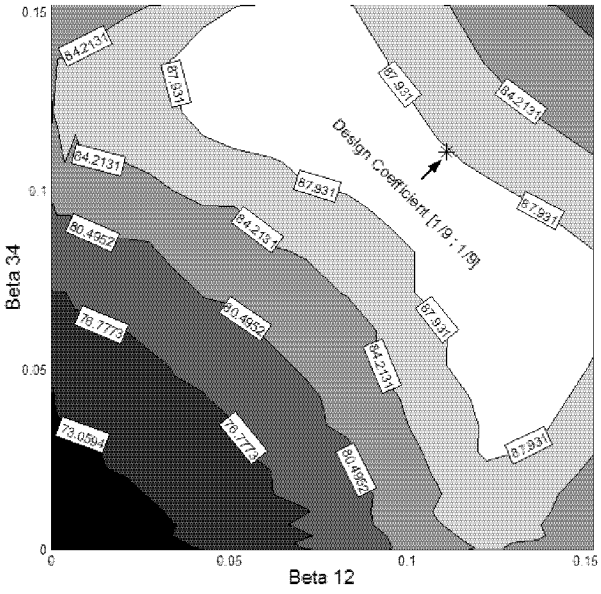

Figure 2. SNQR vs. Feedback Beta weight.

Figure 3 shows the power spectrum density (PSD) of the modulator's output including a detailed zoom view around fs/4 for a -1 dBFS sine wave (and relative to the reference voltage). SNQR of 88 dB and a SFDR of 107 dB are achieved. Figure 4 shows the histogram of the outputs of all resonators relative to the reference voltage, which are all within the quantizer full-scale in order to avoid overloading the modulator stage. Figure 5 shows the 3D plot of the SNQR versus the input signal level and the PSD within the bandwidth. The SNR curve shows that -1dBFS overloading point is achieved and 90% of the modulator full scale can be used. The output PSD shows that the proposed topology will not be affected by stability since the input signal level is less than -1 dBFS. Comparing the results of this semi-MASH architecture with a 4-2^Lmb topology, a more aggressive noise shaping is obtained, on the other hand, comparing it to 4-4^Lmb topology, the overload region is now smaller and the systematic loss is avoided due to scaling down the inter-stage quantizer error coupling gain.

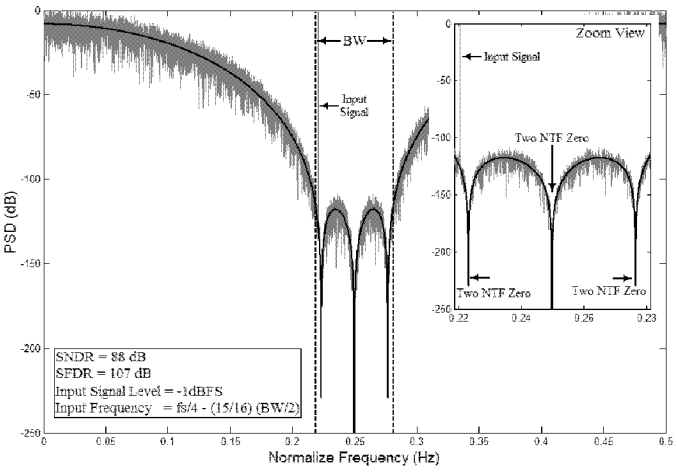

Figure 3. PSD of modulator output.

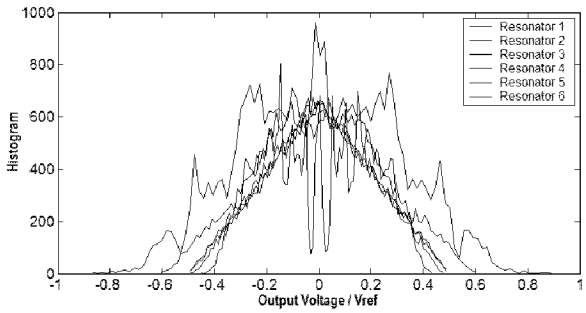

Figure 4. Histogram of all resonator output

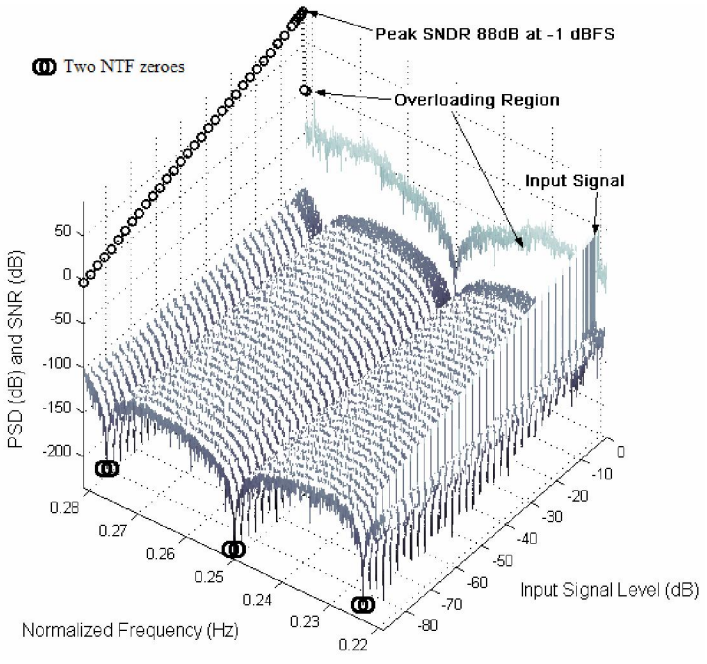

Figure 5. SNQR vs. loop order with different topology for 8xOSR.

Figure 6 shows the SNQR curves and a detailed zoom view for different MASH topologies, with Table I showing their performances summary for 8xOSR. The gray dotted line (a~b) are 12^{th}-order 4-2^4mb MASH with all NTF zeros forced to DC with (a) having 1-bit internal quantizer and -5 dB overloading point (OL) and (b) having 1.5 bit internal quantizer with -1 dB overloading point. Since a 3-level DAC is inherently linear in differential implementation, comparing it to 1-bit internal quantizer, it will be more effective to use a 1.5 bit internal quantizer in order to minimize the overload region. Then, (c) represents a 12^{th}-order semi-MASH with all β gains equal to 1/9, resulting in a larger 17 dB SNQR gain when compared to (a); (d~f) are obtained from 8^{th}-, 10^{th}- and 12^{th}- order Semi-MASH architectures with 1.5-bit internal quantizers, when led to -1dB constant overload point. In the case of the proposed topology (f) it achieves 88dB SNQR with a gain of 18dB SNQR over the traditional 4-2^Lmb topology (b). In a final comparison with 4-2^Lmb and 4-4^Lmb topologies, the proposed semi-MASH maximizes SNQR while minimizing simultaneously the overload region, leading to extendable and expandable bandpass sigma-delta modulator architecture.

Just like most of MASH-type sigma-delta modulators, the inter-stage quantization error leakage is the main drawback that might damage the overall performance. There are three main paths contributing to mismatch leakages: the resonator's feed-forward path gains, the DAC's linearity and the feedback factor β's. Since all resonator's gains of the semi-MASH sub-stage are set to unity, the mismatch in the signal path can be avoided by applying a mismatch-free technique, which will be presented next. The 4^{th}-order bandpass sigma-delta modulator used as first stage contributes for the suppression of all mismatches leakages through a 4^{th}-order band-pass noise shaping. Figure 7 shows the histogram of SNR of -1 dBFS input with different capacitor ratio mismatch standard deviation of the DAC's and the feedback factor β's with 100 Monte-Carlo simulations. Worst case 78-dB SNR is achieved for 0.1% standard deviation in capacitor ratio. Dynamic element matching and calibration technique [10] could be applied to suppression the mismatch leakage. A band-pass DEM technique [5-6] can also be applied to the DAC, which will be equivalent to apply a high-order noise-shaping (first-stage with a 4th-order noise shaping and a band-pass DEM noise-shaping) for the suppression of the DAC's linearity leakages more effectively.

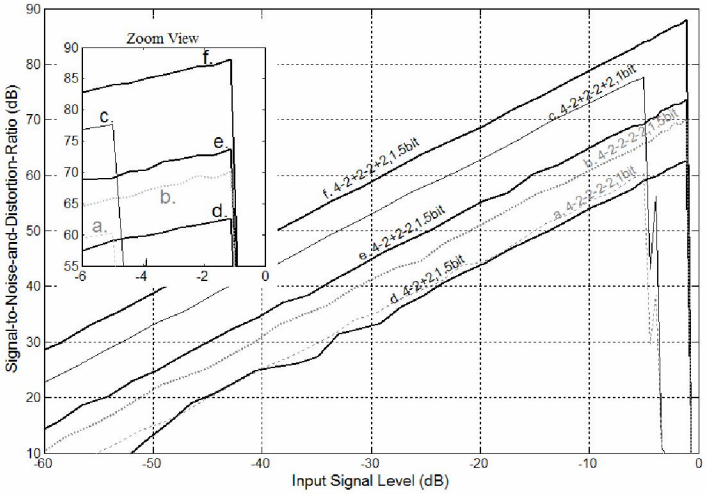

Figure 6. SNQR vs. loop order with different topology for 8xOSR

TABLE I PERFORMANCE SUMMARY FOR DIFFERENCE TOPOLOGY

Topology	SNQR	OL
a. 4-2-2-2-2 MASH; 1-bit	60 dB	-5 dB
b. 4-2-2-2-2 MASH; 1.5-bit	70 dB	-1 dB
c. 4-2+2-2+2 semi-MASH; 1-bit	77 dB	-5 dB
d. 4-2+2 semi-MASH; 1.5-bit	62 dB	-1 dB
e. 4-2+2-2 semi-MASH; 1.5-bit	73 dB	-1 dB
f. 4-2+2-2+2 semi-MASH; 1.5-bit	88 dB	-1 dB

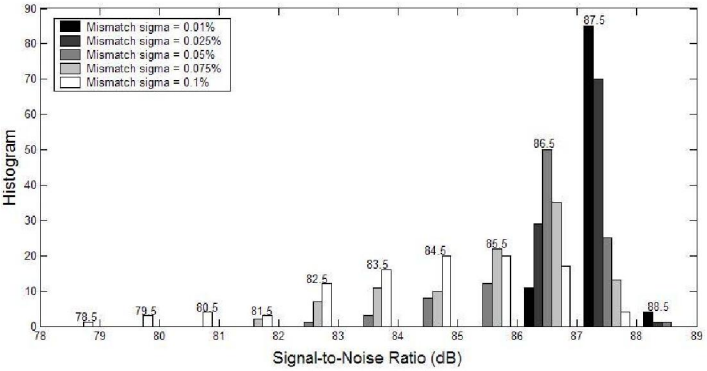

Figure 7. SNQR vs. weight mismatch standard deviation

III. DOUBLE-SAMPLING MISMATCH-FREE RESONATOR

A mismatch-free technique based on an exchange capacitor has also been developed for the switched-capacitor delay circuit [11]. Since in the proposed topology, all the resonators gains of the semi-MASH sub-stages are equal to unity, this technique can be applied to the resonator to avoid inter-stage quantization error leakage. Furthermore, double-sampling can also be applied to increase the effective sampling frequency. Figure 8 shows the proposed double-sampling mismatch-free single-opamp double-delay resonator.

There, several operations can be found that include sampling, output, store and charging, and which will be executed by the exchange of 4 capacitors (C_A, C_B, C_C, C_D) circularly in the 4 phases (a, b, c, d). In phase a, the input will be sampled by C_A. Then, C_A will connect to the output in phase b and the charge in Cc will charge the output capacitor. Also, the charge in Cc is stored in phase a, which will be the output in phase d. This operation will be continuous executed by the 4 capacitors (C_A, C_B, C_C, C_D) circularly in the 4 phase (a, b, c, d). There is no charge-transfer though this feed-forward path, implying that there will be no capacitor mismatch affecting the resonator gain that is equal to 1. This operation can be summarized (14) to (16). Figure-9 shows the resonator simulated magnitude response versus different DC gains. This technique will be further developed and applied to the semi-MASH architecture previously introduced in order to optimize its performance in subsequent work.

$$C_A \times Y[n] = C_A \times X[n-1] - C_C \times Y[n-2] \quad \ldots (14)$$

$$C_A \times Y(z) = C_A \times X(z) \times z^{-1} - C_C \times Y(z) \times z^{-2} \quad \ldots (15)$$

$$\frac{Y(z)}{X(z)} = \frac{z^{-1}}{1+\frac{C_C}{C_A}z^{-2}} \quad \Rightarrow \quad \left.\frac{Y(z)}{X(z)}\right|_{CA=CC} = \frac{z^{-1}}{1+z^{-2}} \quad \ldots (16)$$

IV. Conclusions

This paper presented an expandable architecture for an extendable high-order bandpass modulator which has employed a semi-MASH technique (4-2+2-…-2+2mb). Significant advantages are obtained in terms of the SNQR, SFDR and overloading region by spreading NTF zeros and using 3-level internal quantizers. The idea of introducing inter-stage feedback has also been combined to existing 4-2^Lmb bandpass sigma-delta topology. A 12th-order 1.5-bit semi-MASH bandpass sigma-delta modulator was then designed to illustrate the novel architecture's efficiency. The design achieved 88dB SNQR with a -1dB overloading point and it also implements the most effective high-order noise-shaping ever developed when compared with previous different topologies. A double-sampling mismatch-free single-opamp double-delay resonator was also proposed for the semi-MASH sub-stage resonator to further enhance the new architecture performance in future work.

Acknowledgment

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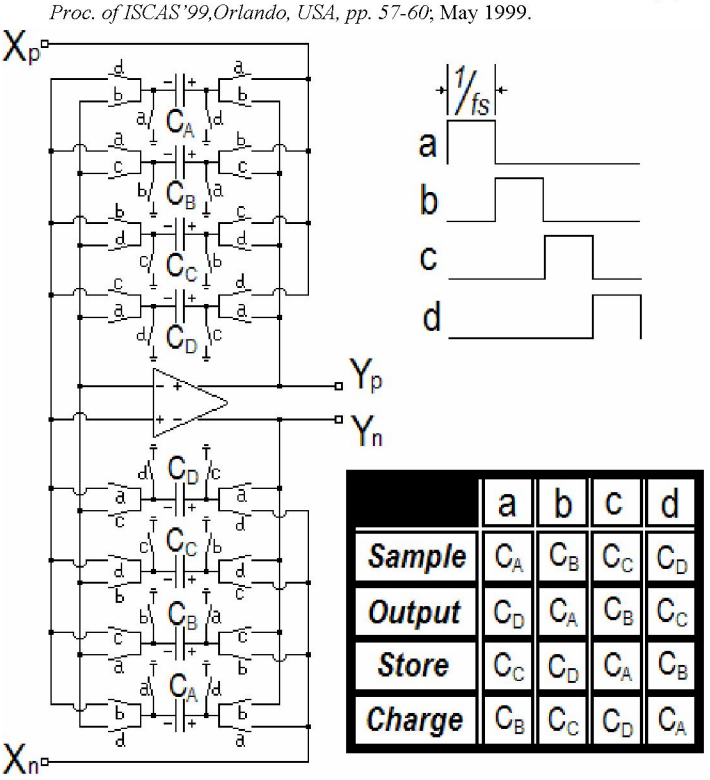

	a	b	c	d
Sample	C_A	C_B	C_C	C_D
Output	C_D	C_A	C_B	C_C
Store	C_C	C_D	C_A	C_B
Charge	C_B	C_C	C_D	C_A

Figure 8. The proposed double-sampling mismatch-free resonator

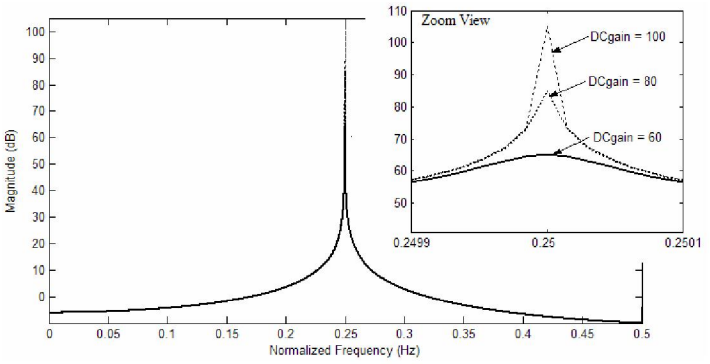

Figure 9. Resonator magnitude responde for different DC gains