ARCHITECTURE COMPILATION OF MULTISTAGE IIR SWITCHED-CAPACITOR DECIMATORS

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Abstract

An interactive architecture compiler has been developed for the design of multistage IIR Switched-Capacitor (SC) decimators with optimum implementation. The approach is based on the cascade of N-th order IIR SC decimator building blocks as a means of obtaining minimum order structures for high selectivity applications with very large factors of sampling rate reduction. The strategy for reducing the sampling rate is determined in conjunction with the pole-zero pairing in order to achieve the required baseband and anti-aliasing amplitude responses using a minimum number of switching waveforms, to relax the speed requirements of the operational amplifiers and also to reduce the capacitance spread and total capacitor area. A design example is presented of an SC bandpass decimator which is suitable for a voiceband analogue interface system and attractive for CMOS integrated circuit implementation.

1. Introduction

Among the many SC filter design methods that have reached a considerable level of maturity [1,2], SC biquadratic structures suitable for cascaded biquad designs [3] are widely preferred because of their moderate sensitivity characteristics and design flexibility for meeting most of the filtering specifications found in practical applications. Methods which allow designers to quickly compute the exact capacitance ratios for these structures to realise a predetermined set of design specifications are also available. Several research groups have developed "SC silicon compilers" which automatically select a filter structure based upon the design specifications, size all components (operational amplifiers (OA's), capacitors and analogue switches, etc.), and generate a circuit layout which can then be submitted for fabrication. However, the problems of pole-zero pairing, maximisation of the dynamic range, and minimisation of the speed requirements of the OA's, capacitance spread and total capacitor area still prevail.

Recently, discrete-time signal processing concepts have been applied to the development of multirate SC circuits and systems [4-7] which are the most appropriate for applications requiring high factors of sampling rate reduction and high selectivity

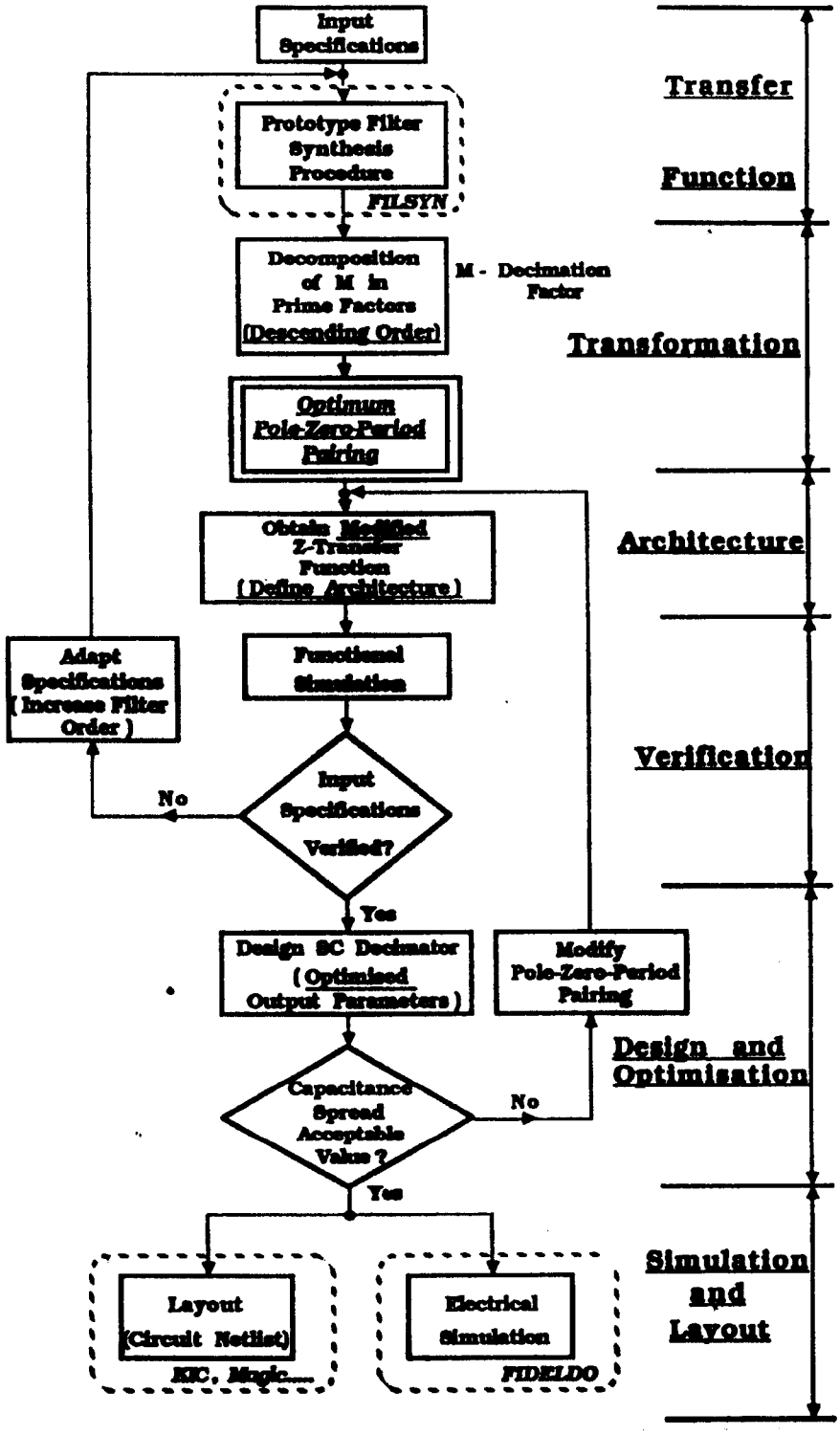

Fig.4 : General structure of the automated methodology for designing multistage IIR SC decimators.

filtering. For such applications a novel methodology has been developed for the design of multistage IIR SC decimators with optimum implementation [8], employing the cascade of only IIR SC decimator building blocks [6,7]. The strategy for reducing the sampling rate is determined in conjunction with the pole-zero pairing to achieve relaxed speed requirements for the OA's together with reduced capacitance spread and total capacitor area.

It is generally a goal of the SC circuit designer to optimise circuit performance while simultaneously minimising silicon area. Unfortunately, this is such a challenging problem that most designers submit non-optimum and sub-optimum designs to fabrication. In this paper we present a novel interactive architecture compiler for the design of multistage IIR SC decimators with optimum implementation. This compiler allows the selection of alternative topologies in order to meet a desired frequency response specification. The computer optimised synthesis procedure is based on the cascade of N-th order IIR SC decimator building blocks in order to obtain minimum order structures for applications with high selectivity and high decimation factors. To achieve the required baseband and anti-aliasing amplitude responses using a minimum number of switching waveforms and relaxed speed requirements of the OA's, an automated pole-zero-period pairing design procedure is carried-out which can be seen as an additional degree of freedom available to the designer for optimising the circuit performance. Once the optimum sequence of decimation and pole-zero pairing have been determined, an optimisation of each single stage is carried-out in order to improve signal handling capability and minimise capacitance spread and total capacitor area. A design example is given of an SC bandpass decimator that is appropriate for a voiceband analogue interface system and which can virtually eliminate costly on-chip active-RC prefilters.

2. General Design Automation Methodology

The general structure of the automated methodology for designing a multistage IIR SC decimator is presented in Fig.1. Basically, the automated design procedure comprises **i)** the definition of the prototype filter **transfer function** that meets the specified baseband and anti-aliasing filtering characteristics, **ii)** the **transformation** of the transfer function for the required decimation factor [9], **iii)** the definition of a decimator **architecture** using a cascade of N-th order building blocks, **iv)** the **verification** of the input specifications carried-out by means of a functional simulation of the modified transfer function of the circuit, **v)** the **design and optimisation** of the SC decimator yielding the determination of the capacitance values, the maximisation of the dynamic range and minimisation of the capacitance spread and total capacitor area, and **vi)** the generation of two output interface files, one for mixed-mode **simulation** of the final SC decimator circuit and the other, which contains a netlist of the circuit, for the **layout** realization.

3. Strategy for Pole-Zero-Period Pairing

The main problem of the above design methodology consists of the selection of a particular sequence for decimation and which should be determined in conjunction with the assignment of poles and zeroes to each SC decimator building block and by taking into account the corresponding frequency-translated aliasing responses. This make it possible not only to obtain the desired baseband specifications, as in traditional cascade filter design methods, but also the specified anti-aliasing filtering response. The optimum sequence of decimation and corresponding pole-zero pairing makes use of the following design criteria:

i) Decompose M in prime factors by descending order, in order to minimise the speed requirements of the OA's,

ii) Associate the larger values of the pole and zero frequencies to the lower values of T_i ($T_i=1/F_{si}$, being F_{si} the sampling frequency of the ith block in the cascade), i.e. minimise F_{si}/F_{pi} and F_{si}/F_{zi}, in order to minimise capacitance spread and total capacitor area,

iii) Implement first lowpass decimator stages with low selectivity poles, i.e. low Q_p, and wide transition bands in order to reject the alias frequency components at higher frequency, and also to increase the attenuation of the input high frequency noise,

iv) Implement high selectivity lowpass decimator stages, as well as bandpass decimator stages, at the heart of the cascade structure in order to increase the attenuation of those aliasing frequency components closer to the passband, and also to maximise the dynamic range of the overall decimator,

v) Implement all highpass decimator stages at the end of the cascade structure, since they only contribute to the definition of the lower stopband of the baseband response.

The automated design procedure is carried-out for all decimator stages until the resulting amplitude response meets the target specifications, both in the baseband and in the aliasing band.

4. Multistage IIR SC Decimators Architecture

The basic building blocks for the implementation of multistage IIR SC decimators are illustrated in Fig.2 [6,7], consisting of a single SC network with input sampling rate MF_s and whose output sampling rate F_s determines the speed requirements of the OA's. Fig.2-a and 2-b, respectively, show first and second order building blocks, while in Fig.2-c an N-th order building block is presented. In general, such building blocks can be divided into two major parts, namely one high selectivity recursive network primarily responsible for the implementation of the denominator polynomial function and one low selectivity polyphase network determining the numerator polynomial function. The recursive network can realize an arbitrary combination of real and complex conjugate poles. The polyphase network, on the other hand, is formed by a varying number of

simple SC branches depending both on the sampling rate decimation factor M and on the complexity of the numerator polynomial function. After the implementation of the pole-zero-period pairing strategy, the final multistage architecture can be obtained by the cascade connection of any number of such building blocks.

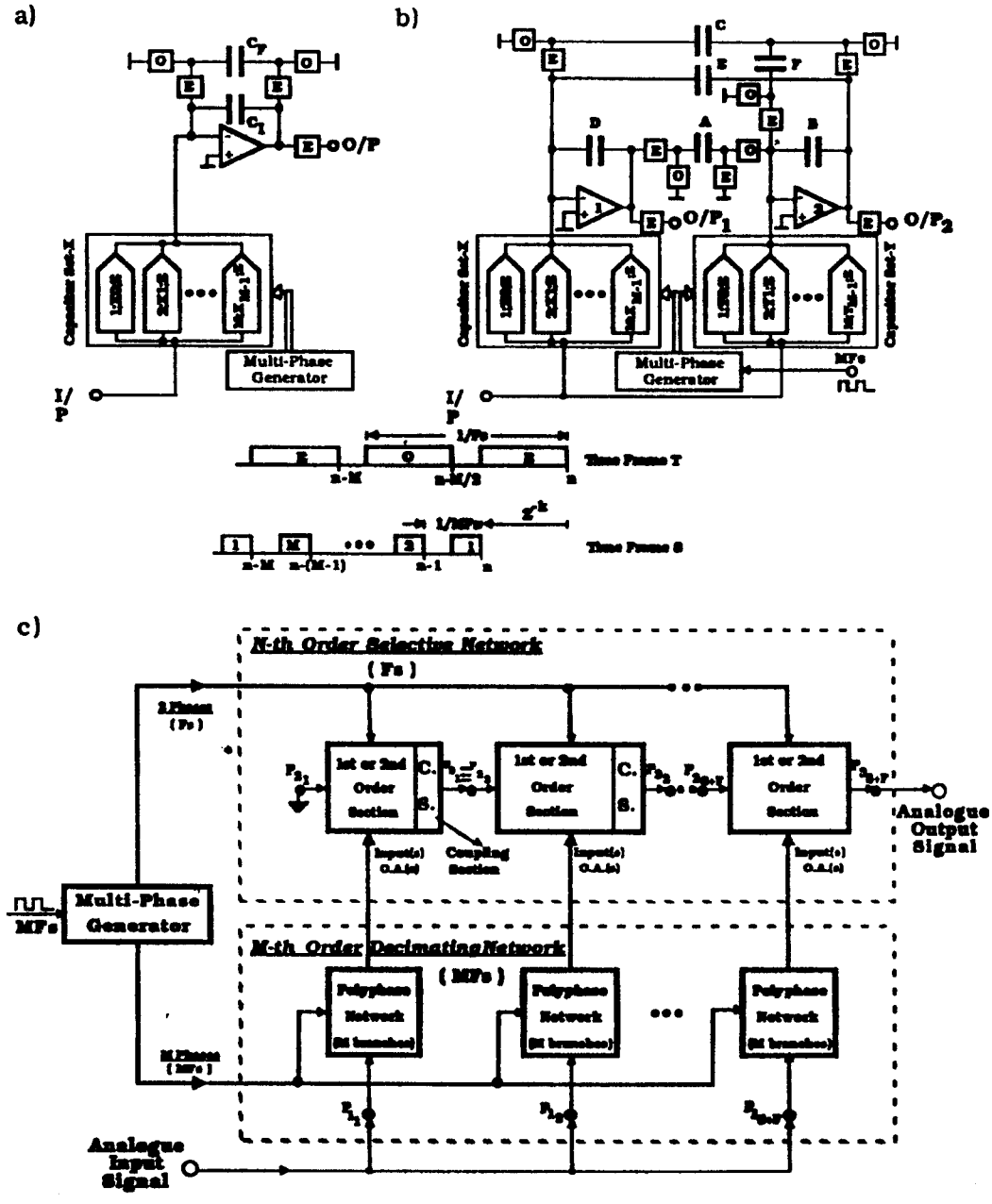

Fig.2: Basic IIR SC decimator building blocks.
a) 1st. order. b) 2nd. order. c) N-th order.

5. Menu Structured Environment

To simplify the design of a multistage IIR SC decimator a highly interactive menu structured environment is developed to render more user friendly the interface between non skilled users and the general design automated methodology presented before. Fig. 3 shows the most important menus used in the definition of an optimum multistage design. The automated design can be divided into two major parts, one mainly responsible for the input specifications (with an interface to FILSYN [11]) and the other one implementing the different steps of the automated design methodology. The final results validated by the functional verification lead to interface files, both for electrical and functional simulation and for the layout realization.

6. Design Example

In order to demonstrate the above methodology we shall consider here the design of an IIR SC bandpass decimator which is appropriate for a voiceband analogue interface system. For an input sampling rate above 1MHz only a mere first order prefilter is required and this can be realised by a simple off-chip RC section. Despite this high input sampling rate, the decimator will be designed to allow comfortable settling times for the OA's determined by switching frequencies well below 1MHz.

The complete architecture of the SC bandpass decimator is illustrated in Fig.4-a. A high selectivity 12th. order SC bandpass decimator with a factor M=40 of sampling rate reduction is designed to meet the baseband specifications together with a minimum 55dB rejection of the aliasing frequency components up to $40F_S/2$ and the corresponding repetitions above $40F_S/2$. In front of this bandpass decimator we place a simple 2nd. order lowpass decimator to increase the input sampling rate up to $120F_S$ and, at the same time, guarantee the required 65dB rejection of the aliasing frequency components over the entire frequency range from baseband to $120F_S/2$ and the corresponding repetitions above $120F_S/2$. The resulting capacitance spread after design optimisation is 48, the total capacitor area under 530 capacitor units and the minimum time for the amplifiers to settle is 5.2μs.

Fig.5-a and Fig.5-b, respectively, illustrate the ideal amplitude baseband responses of the SC lowpass and bandpass decimators, i.e. from DC to $120F_S/2$ and from DC to F_S. The complete response of the overall SC bandpass decimator in the frequency band from DC to $120F_S/2$, is shown in Fig.5-c giving the required 65dB minimum rejection of the unwanted aliasing frequency components.

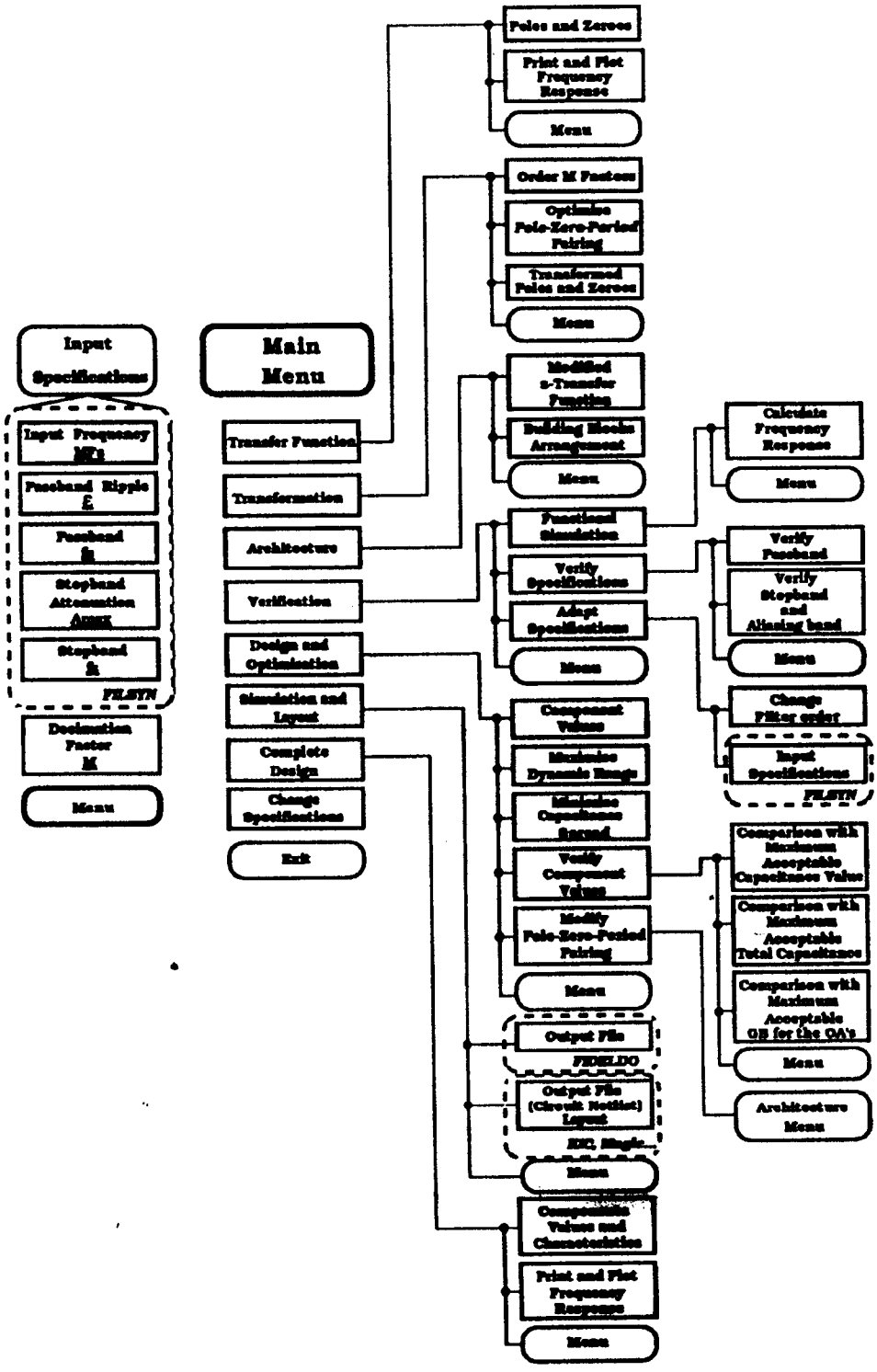

Fig.3 : Menu-structured environment of the computer-aided tool.

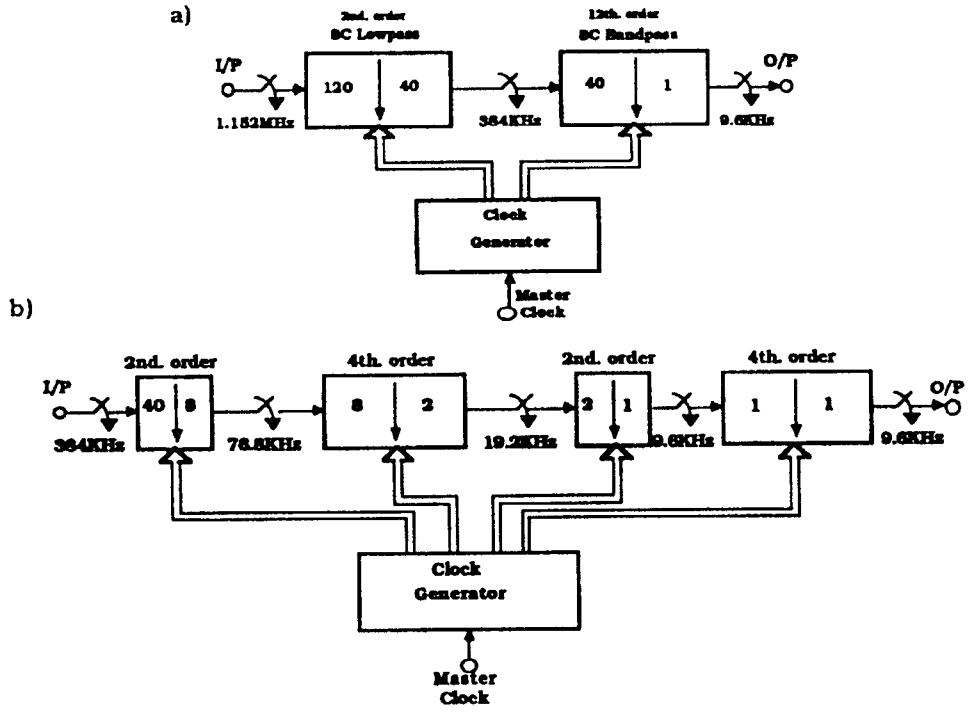

Fig.4 : Multistage IIR SC bandpass decimator system (M=120).
a) Overall architecture. b) SC bandpass decimator.

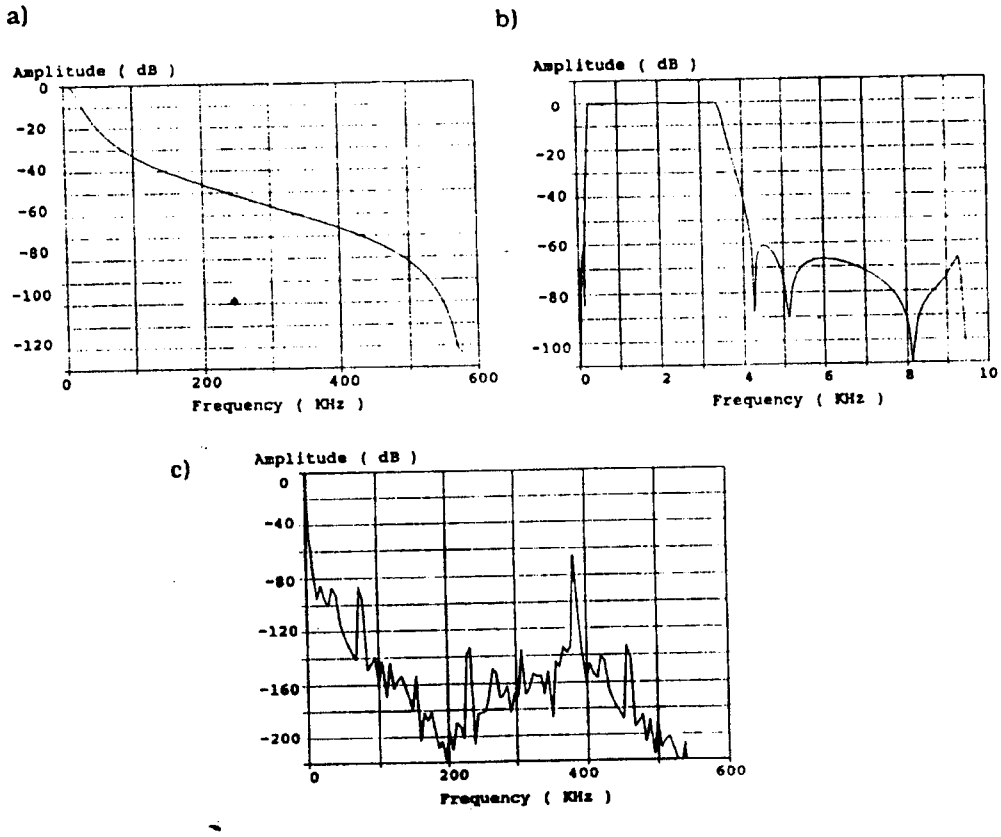

Fig. 5 : Multistage IIR SC bandpass decimator system amplitude response.
a) Lowpass decimator. b) Bandpass decimator. c) Overall multistage decimator.

7. Conclusions

This paper described an interactive architecture compiler which produces optimum designs of multistage IIR SC decimators. This is based on the cascade of only IIR SC decimator building blocks in order to obtain minimum order structures for high selectivity filtering requirements with large factors of sampling rate reduction. In such structures the strategy for pole-zero-pairing is determined to achieve relaxed speed requirements for the OA's, to minimise silicon area and to maximise signal handling capability. A user friendly menu structured environment has also been developed to simplify the complex system design. Finally, the proposed design approach has been employed for designing an SC bandpass decimator which virtually eliminates the need for costly on-chip continuous-time filters in voiceband analogue interface systems, thus making it attractive for the implementation of high performance integrated circuits.

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[2] - **P.E.Allen, D.R.Holberg,** *"CMOS Analog Circuit Design"*, Holt, Rinehart and Winston, New York, U.S.A., 1987.

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[8] - **R.P.Martins, J.E.Franca,** "Optimum Implementation of a Multistage IIR SC Bandpass Decimator for a voiceband Analogue Interface System", *Proceedings International Symposium on Circuits and Systems 1988*, Helsinky, Finland, pp.1661-1664, June 1988.

[9] - **R.E.Crochiere L.R.Rabiner,** *"Multirate Digital Signal Processing"*, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1983.

[10] - **FIDELDO (Rel.-3.0),** "User and Installation Manual", CNET/ANACAD-France, 1988.

[11] - **G.Szentirmai,** "S/FILSYN Quick Reference Manual", April 1983.

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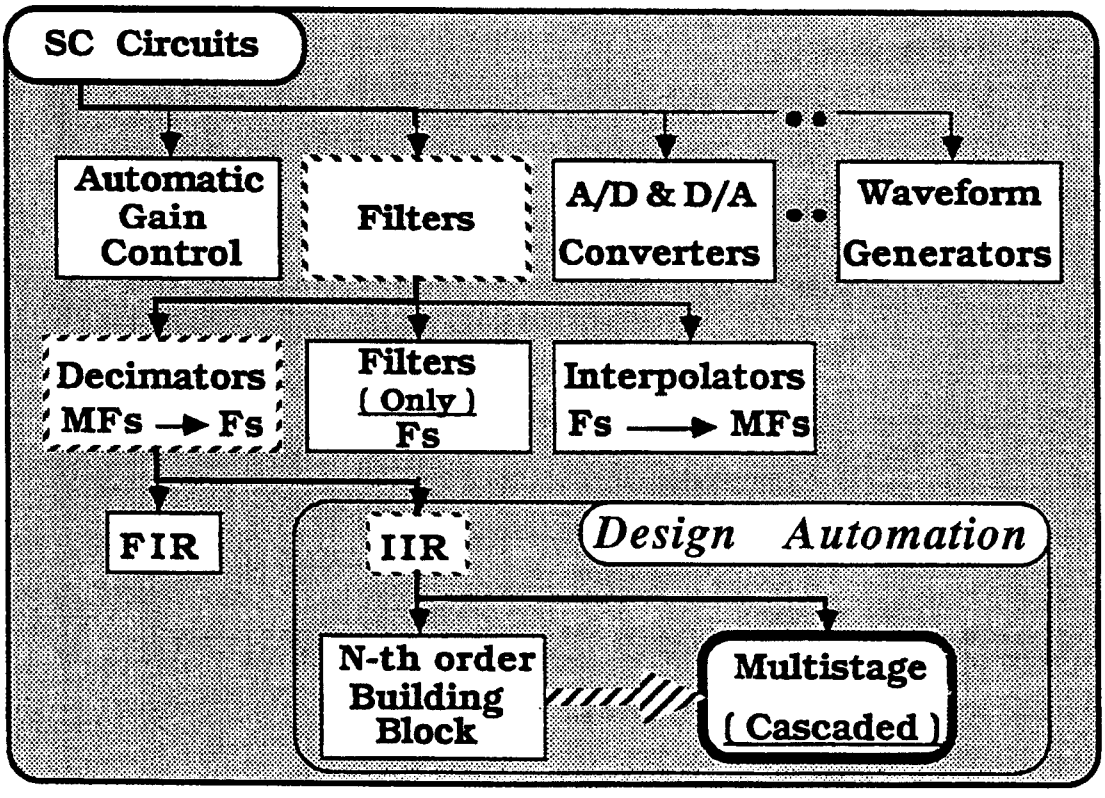
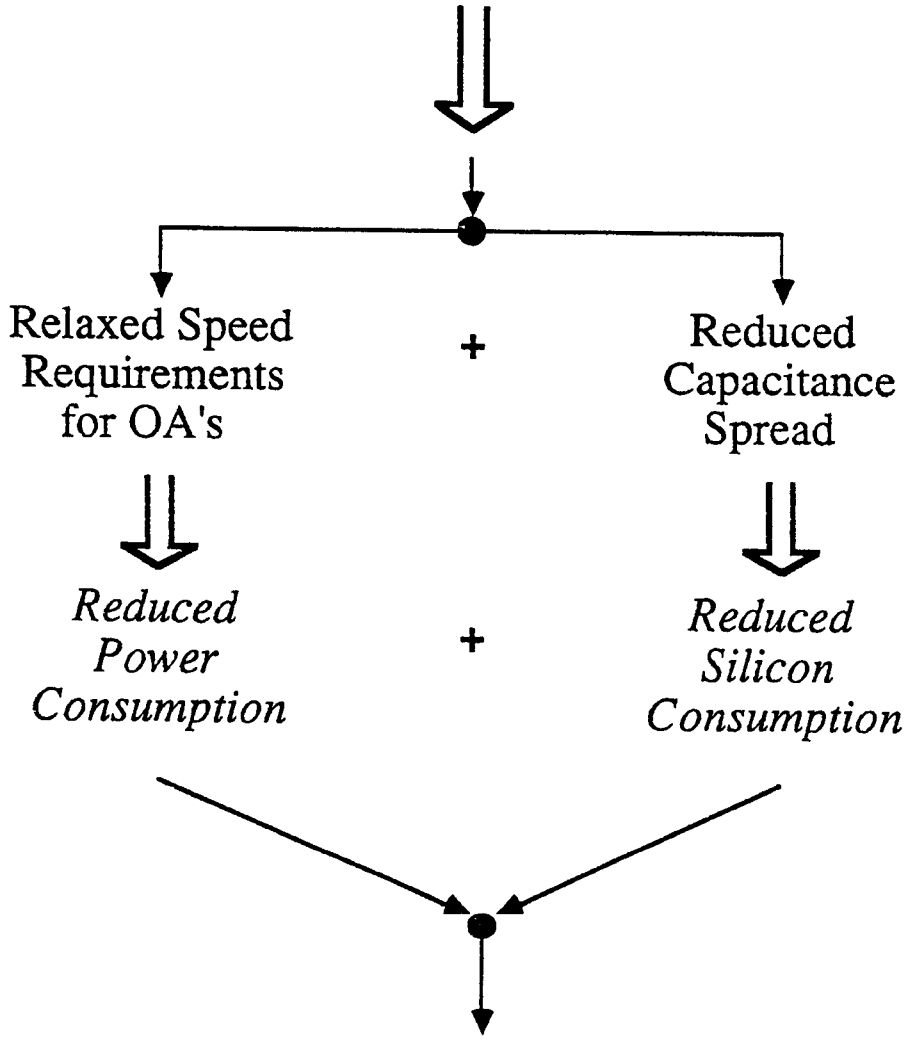


Advantages

- Reduce sampling frequency from infinity (continuous-time) to ADC sampling frequency
- Provide required anti-aliasing and baseband specifications
- Minimum silicon and power consumption
- Ideally no on-chip continuous-time filters

- **Design Strategy**

Sampling Rate Reduction + Pole-Zero Pairing



Optimised Circuit Performance

Introduction

- **Interactive Architecture Compiler**

Architecture ⟶ Cascade N-th order IIR SC Decimator building blocks

(Multistage order = No. Stages x N)

- **Novel Interactive Architecture Compiler with Automated :**

Pole-Zero-Period Pairing Procedure

Capacitor Values Design

File Generation for Layout and Simulation

allows :

Interactive Topology choice

is adequate for :

High selectivity and high sampling rate reduction applications

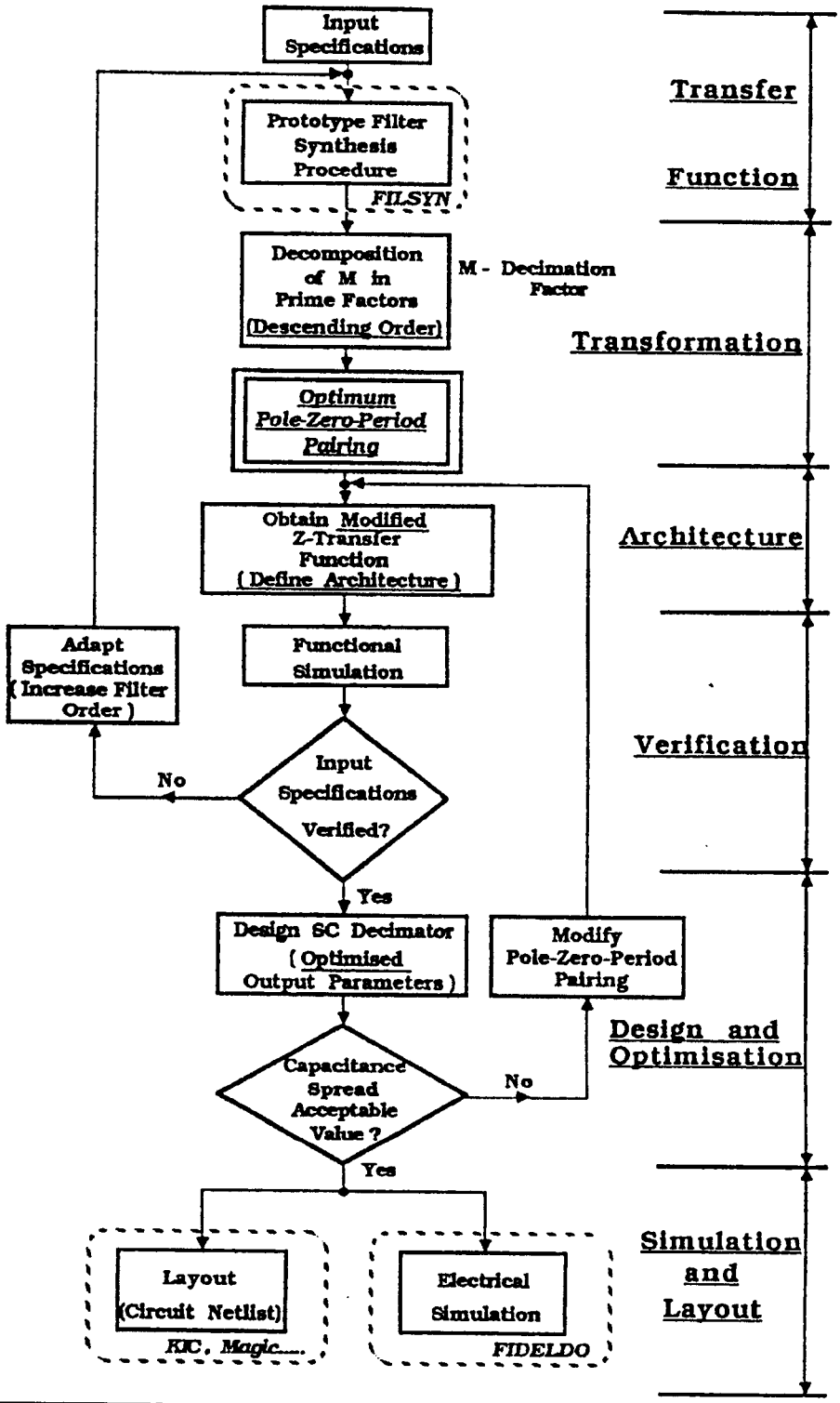
and optimises :

OA's Speed Requirements

Capacitance Spread

Signal Handling Capability

Anti-aliasing Frequency Response


Input Specifications
Prototype Filter Synthesis Procedure
FILSYN
Decomposition of M in Prime Factors (Descending Order)
M - Decimation Factor
Optimum Pole-Zero-Period Pairing
Obtain Modified Z-Transfer Function (Define Architecture)
Adapt Specifications (Increase Filter Order)
Functional Simulation
No
Input Specifications Verified?
Yes
Design SC Decimator (Optimised Output Parameters)
Modify Pole-Zero-Period Pairing
Capacitance Spread Acceptable Value ?
No
Yes
Layout (Circuit Netlist)
KIC, Magic.....
Electrical Simulation
FIDELDO
Transfer Function
Transformation
Architecture
Verification
Design and Optimisation
Simulation and Layout

- **Design Methodology**
  - **Original z-Transfer Function**
    Poles and Zeroes at MFs
  - **Modified z-Transfer Function**
    Poles and Zeroes at ≠s MiFs

- **Pole-Zero-Period Coupling**

i) M decomposed in prime factors by descending order ⟹ Low speed OA's

ii) Larger values of pole and zero frequencies associated to lower values of Ti ⟹ Minimise Capacitance Spread

iii) Implement 1st. lowpass decimator stages with low selectivity poles ⟹ Reject High Frequency Alias Components

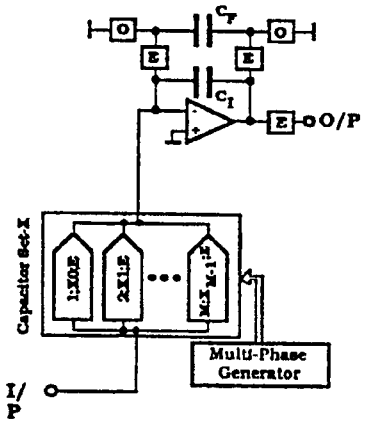
iv) Implement high selectivity poles and bandpass decimator stages at the heart of the cascade ⟹ Increase attenuation Alias Components Close to Passband

v) Implement highpass decimator stages at the end of the cascade ⟹ Only contribute to lower stopband

Alternative topologies in cascading IIR SC decimator building blocks

- **IIR SC Decimator Building Blocks :**

a)



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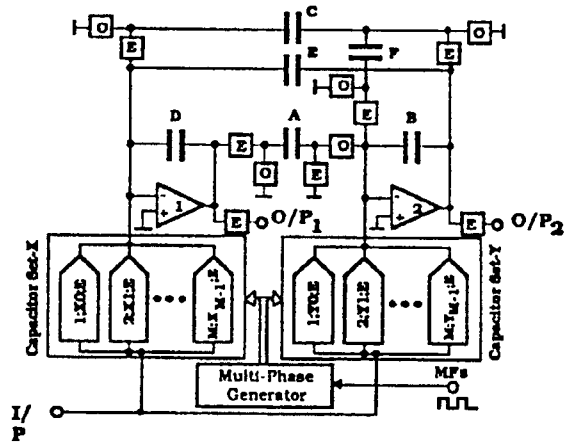
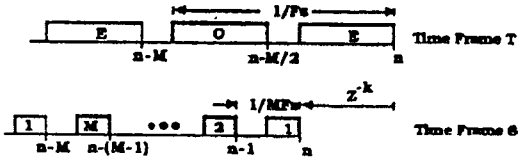
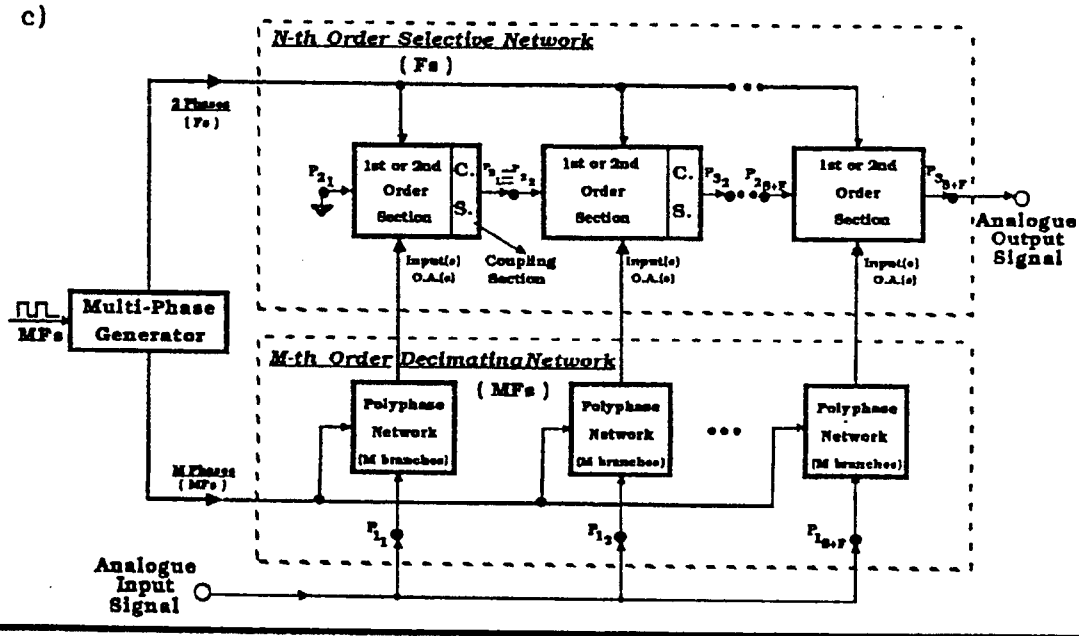
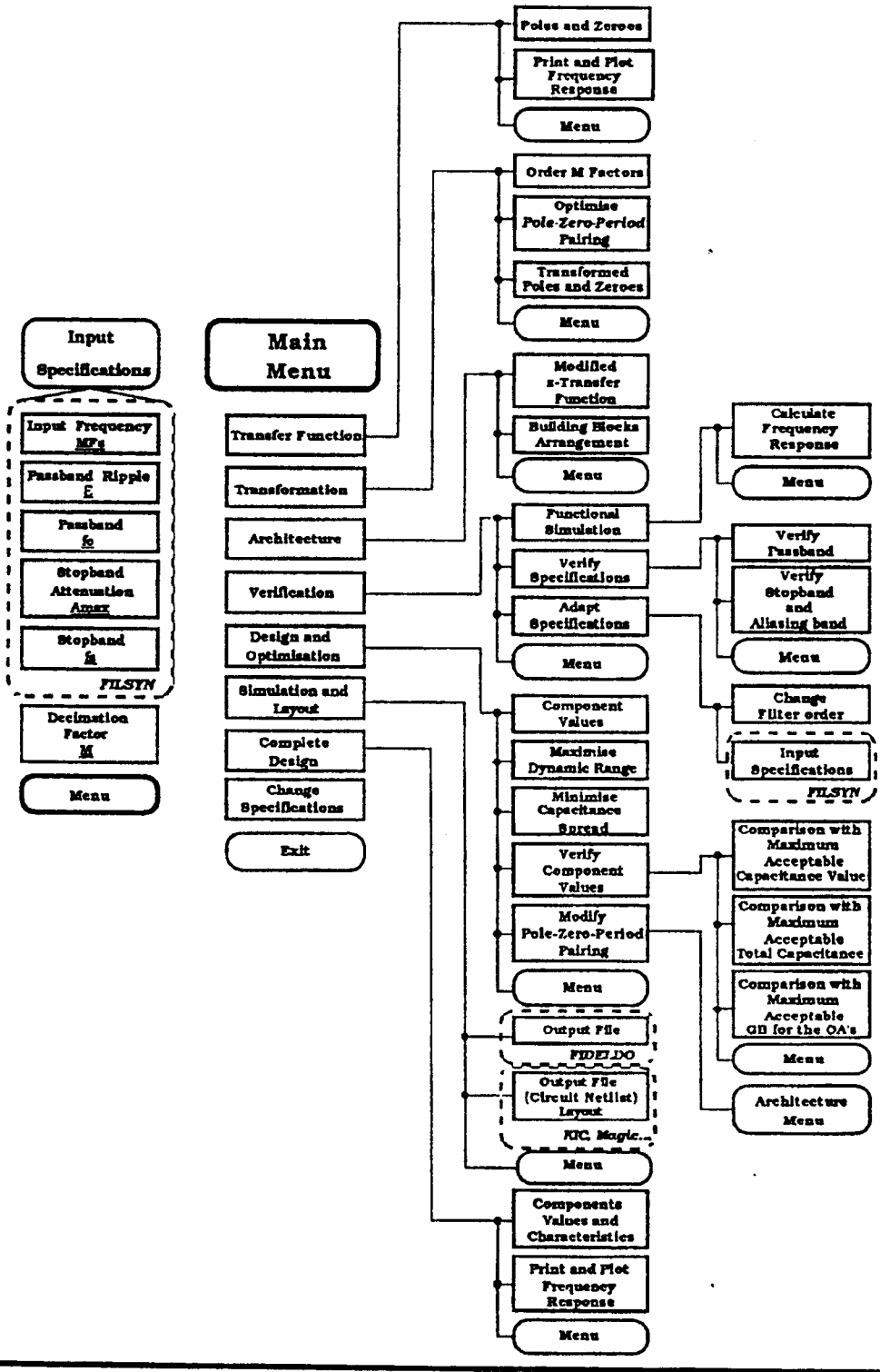




c)

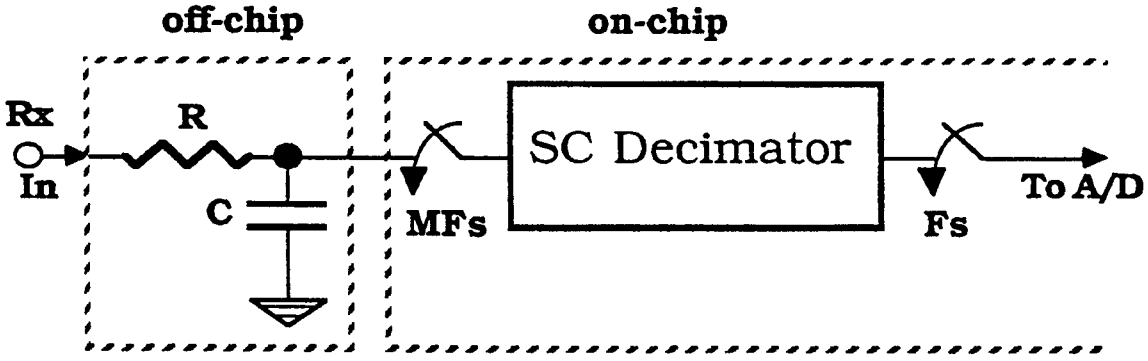


Menu Structured Environment



Design Example

- **Design Strategy**



- Fs / fmax ≅ 3
- MFs / fmax ≅ 3 M

⇓

- For a 1st. order off-chip RC lowpass filter

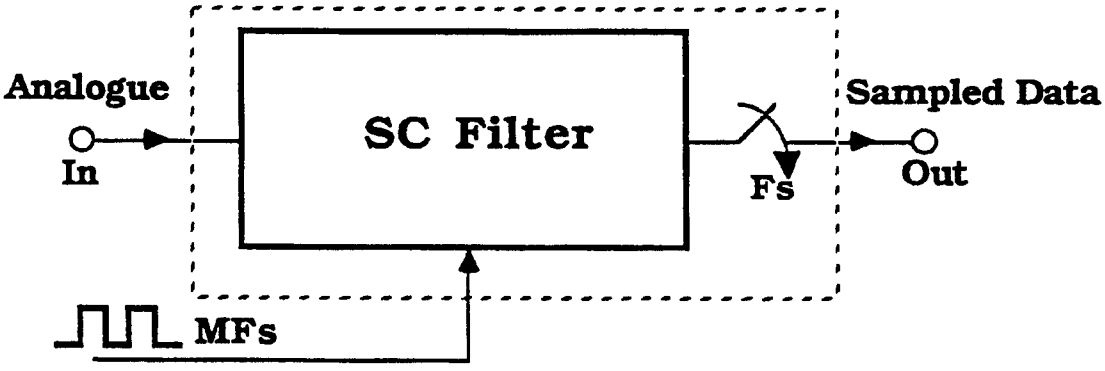
⇓

- $M_{min} \cong 120$

Design Example

- **Traditional Implementation**

IIR Single Stage Non - Optimum SC Implementation



Unacceptably Large Capacitance spread

⇓

Large Silicon Consumption

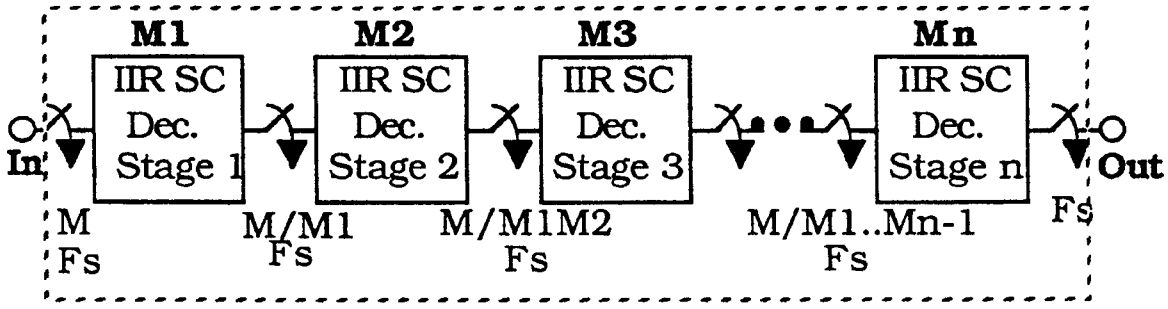
High Speed Operational Amplifiers

⇓

High Power Consumption

Design Example

- **Optimum Multistage Implementation**



Response DC to MFs/2

- Advantages
  - **Reduces capacitance spread**
  - **Reduces total capacitor area**
  - **Allows low speed OA's**

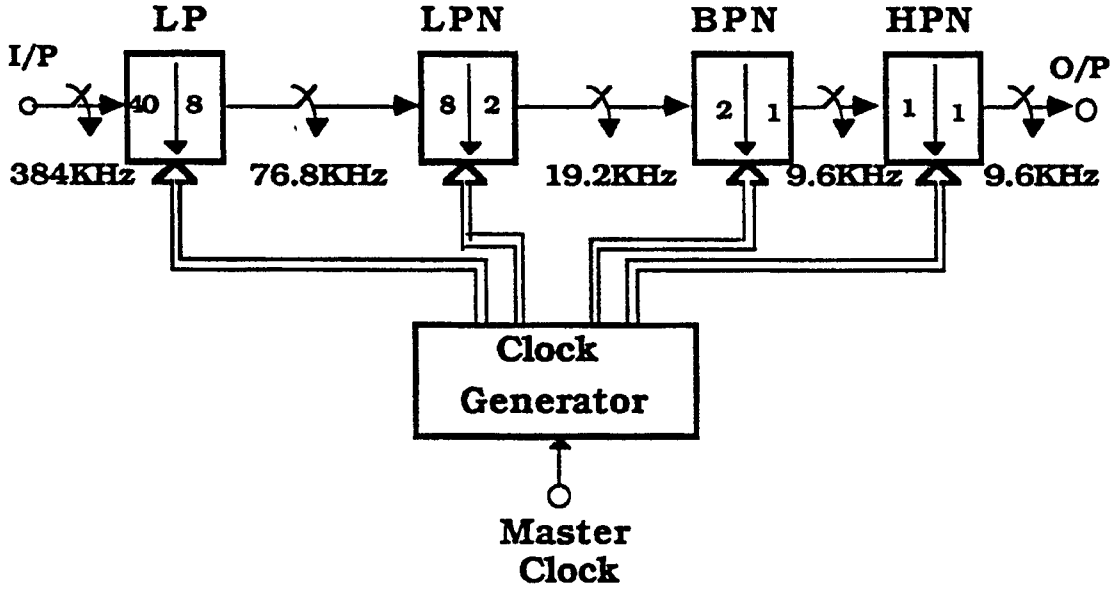
This approach requires :

- **Optimum Nth. order building blocks for implementation (** *Franca, Martins* **)**
- **Synthesis of Z-Transfer Function following an optimized procedure for Pole-Zero-Period coupling**

Design Example

- **IIR SC Bandpass Decimator**

(12 th. order)



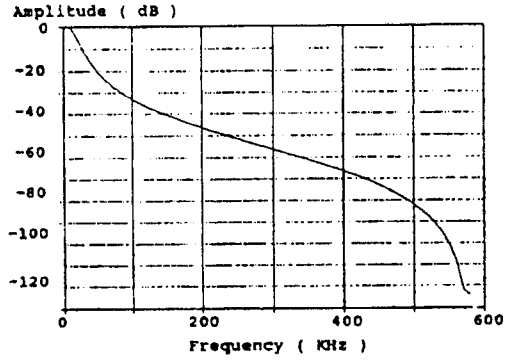
- **Capacitance Values**

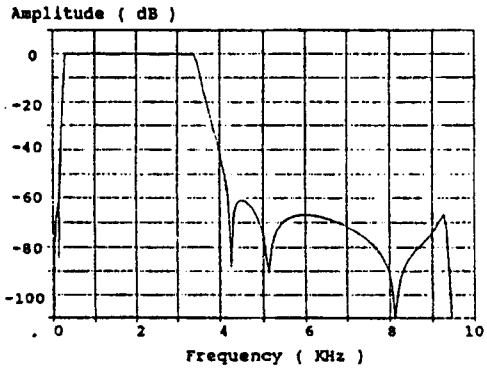
Approach	Spread	Total Area
Tradit.	840	5200
New	48	530

Design Example

- **Results**

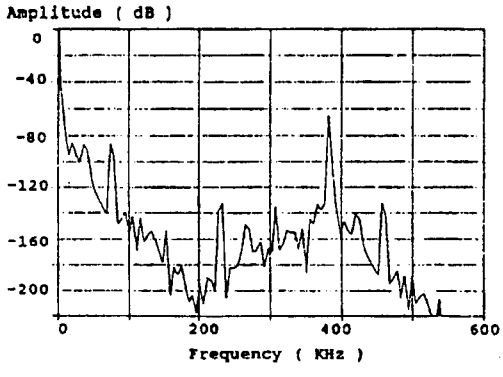
IIR SC Lowpass Decimator
(DC - 120 Fs/2)





IIR SC Bandpass Decimator
(DC - Fs)

Overall IIR SC Decimator
(DC - 120Fs/2)



Conclusions

- Novel interactive compiler of multistage IIR SC decimators is presented which allows the design of :

  - **Minimum order structures for high selectivity filtering**
  - **Large sampling rate reduction factors**
  - **Relaxed speed requirements for the OA's**
  - **Reduced capacitance spread and total capacitor area**
  - **Elimination of on-chip continuous-time filters**
  - **Integrated Circuit Implementation**

with a:

Complete Automated Design Procedure

from

Specifications

to

Simulation and Layout